

**MANIPAL SCHOOL OF INFORMATION SCIENCES**

**(A Constituent unit of MAHE, Manipal)**

**ASSIGNMENT – 1**

**DIGITAL SYSTEMS AND VLSI DESIGN LAB**

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| **Reg. Number** | **Name** | **Branch** |
| **241038005** | **Chaitanya S Rao** | **VLSI** |

**Submitted to**

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**11/11/2024**

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**Question**

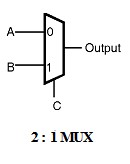
1. Design a 2:1 MUX using transmission gates.
2. Design a 4:1 MUX making use of the symbols of 2:1 MUX designed above.
3. Simulate the behaviour of this design.

Draw the layout for the above design and verify its correctness by spice extraction, LVS, RC extraction and simulation.

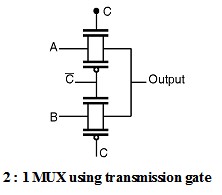
**2:1 MUX using transmission gates:**

**Theory:**

A 2:1 multiplexer is shown in Figure below. This gate selects either input A or B on the basis of the value of the control signal 'C'. When control signal C is logic low the output is equal to the input A and when control signal C is logic high the output is equal to the input B. A 2:1 multiplexer can be implemented using transmission gates. Figure below shows the connection diagram of the 2:1 multiplexer using transmission gates. The 2:1 MUX selects either A or B depending upon the control signal C. When the control signal C is high then the upper transmission gate is ON and it passes A through it so that output = A.



When the control signal C is low then the upper transmission gate turns OFF and it will not allow A to pass through it, at the same time the lower transmission gate is 'ON' and it allows B to pass through it so the output = B.



**Schematic diagram:** The circuit schematic of the 2:1 MUX Using Transmission Gate is as shown below,

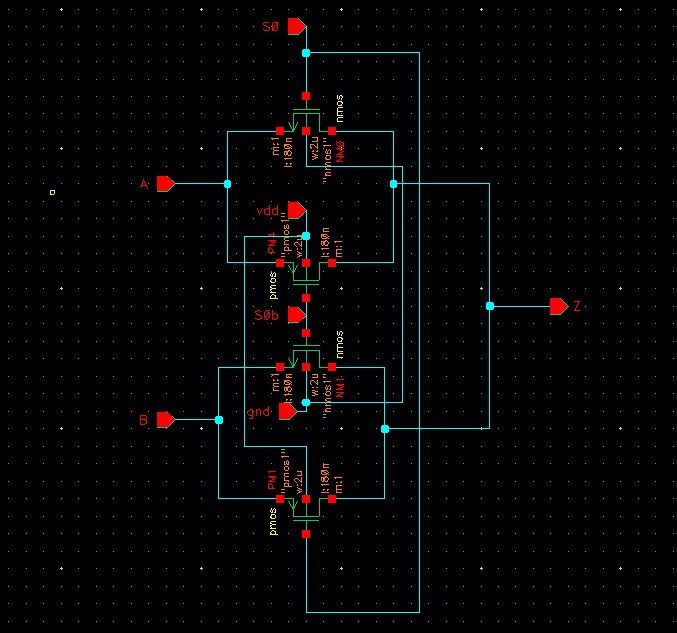


Figure 1: 2:1 MUX Using Transmission Gate

**Simulation Results:**

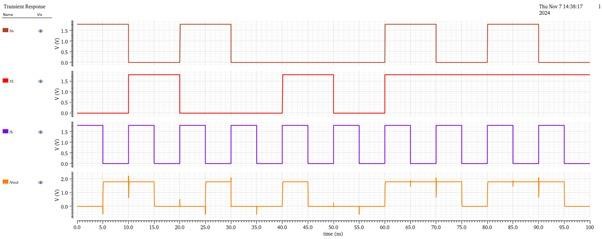


Figure 2: Simulation results of 2:1 MUX

**Symbol:**

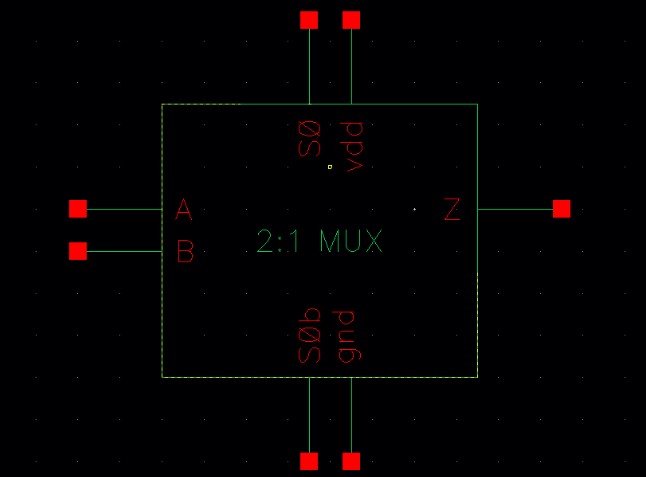


Figure 3: symbol of 2:1 MUX Using Transmission Gate

**Layout:**

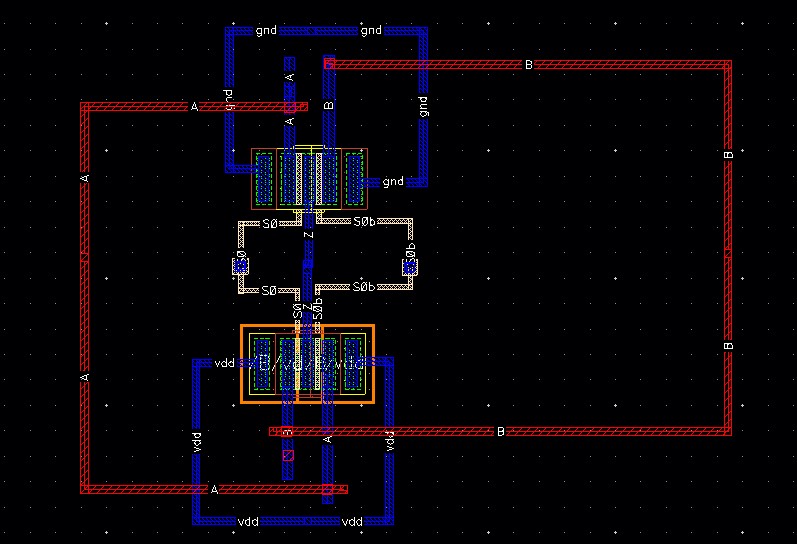


Figure 4: Layout of 2:1 MUX Using Transmission Gate **Results:**

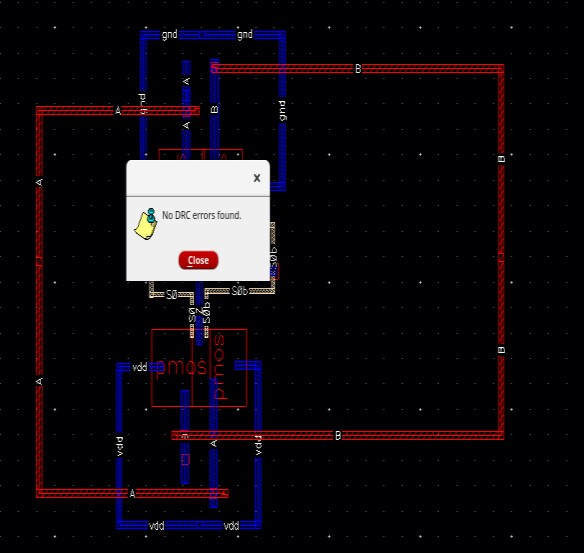


Figure 5: No DRC error in 2:1 mux

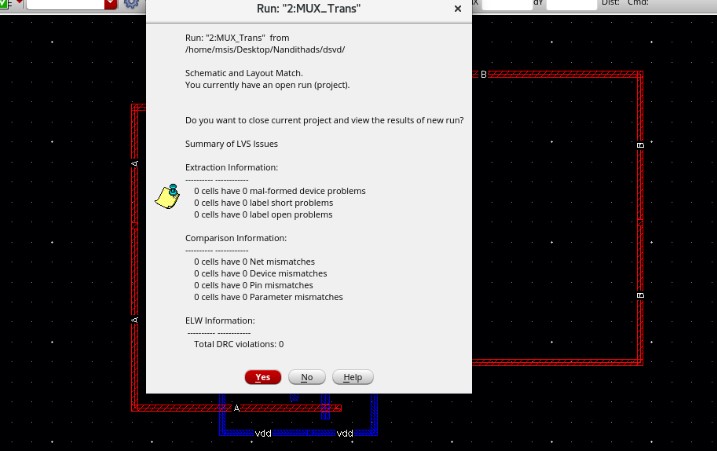


Figure 6:No LVS error in 2:1 MUX

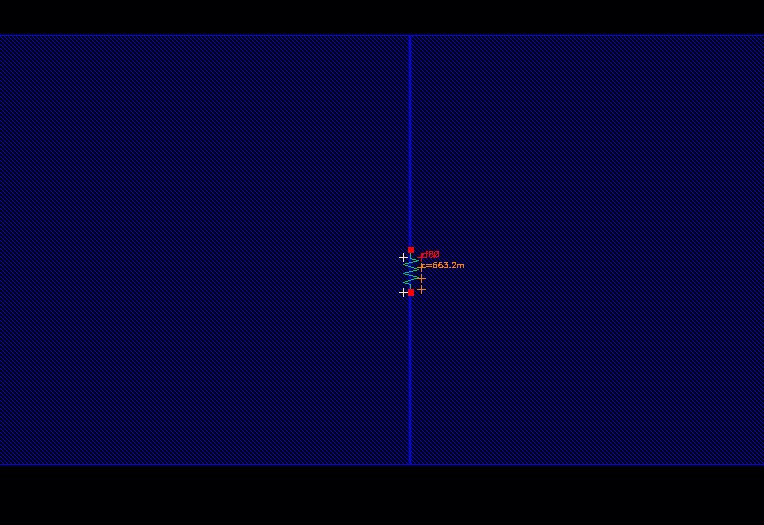


Figure 7: Extracted R in 2:1 MUX

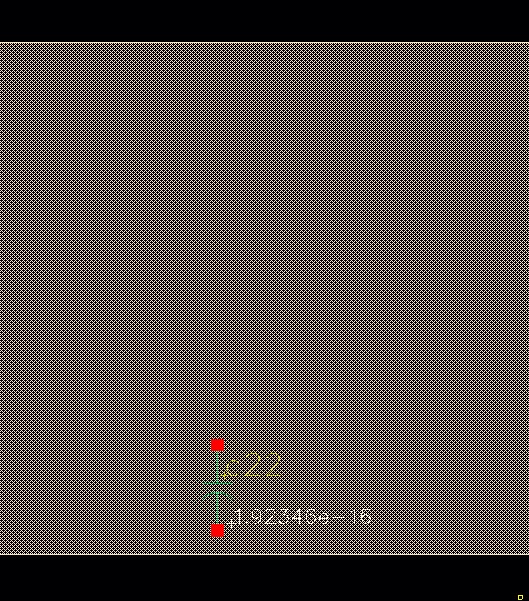
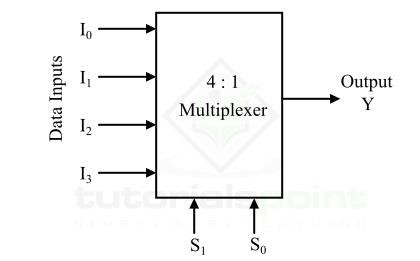


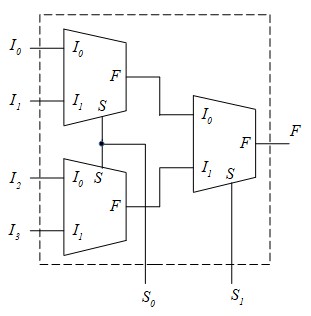
Figure 8:Extracted C in 2:1 MUX

**4:1 MUX using 2:1 MUX:**

4×1 Multiplexer has four data inputs I3, I2, I1 & I0, two selection lines S1 & S0 and one output Y. The block diagram of 4×1 Multiplexer is shown in the following figure.



Three 2: 1 MUX are required to implement 4 : 1 MUX.



**Schematic diagram:** The circuit schematic of the 4:1 MUX Using Transmission Gate is as shown below,

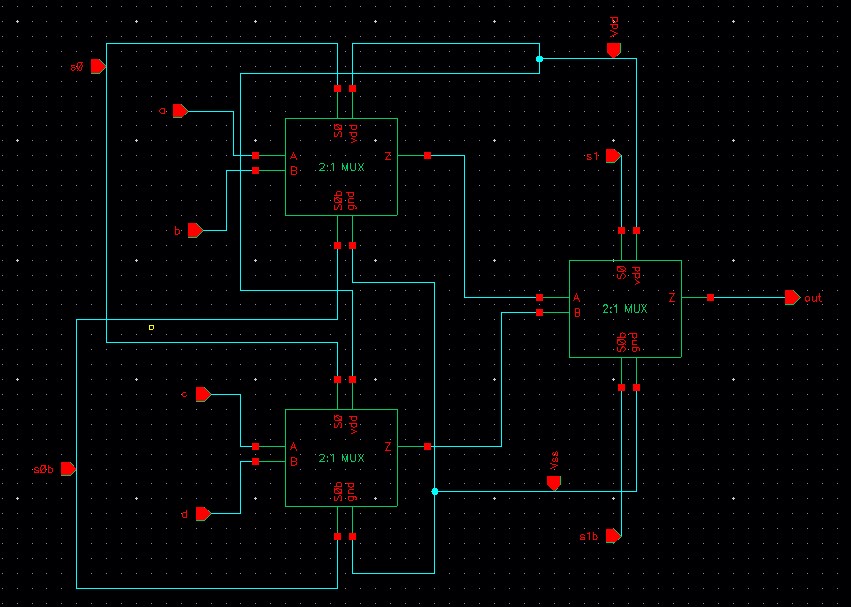


Figure 9: Schematic of 4:1 MUX using 2:1 MUX

**Simulation Results:**

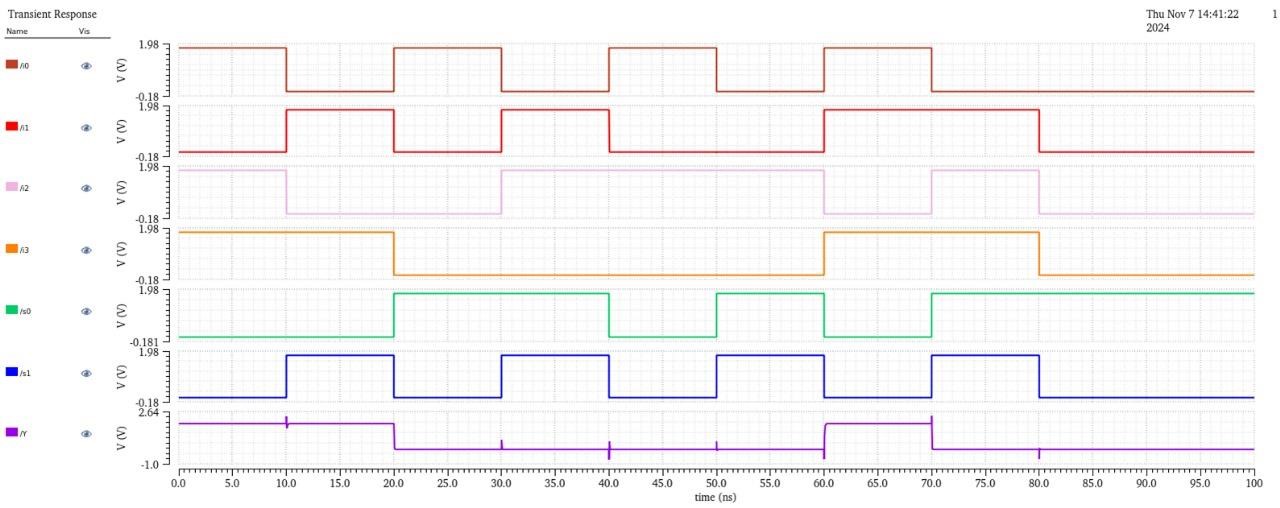


Figure 10: Simulation results of 4:1 MUX

**Layout:**

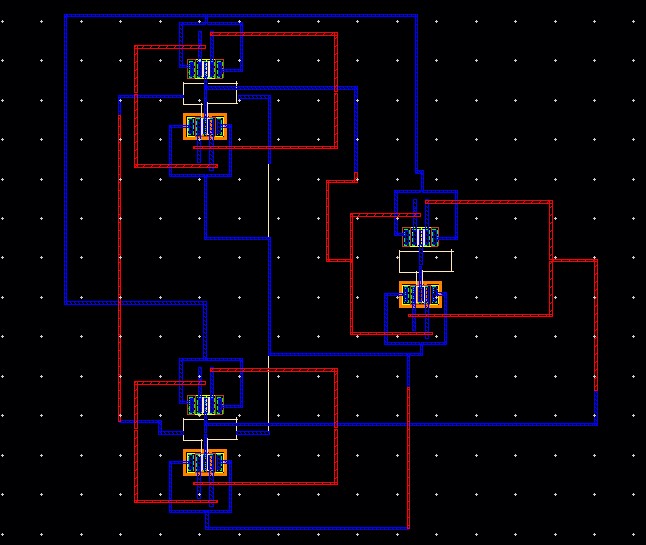


Figure 11: Layout of 4:1 MUX Using Transmission Gate

**Results:**

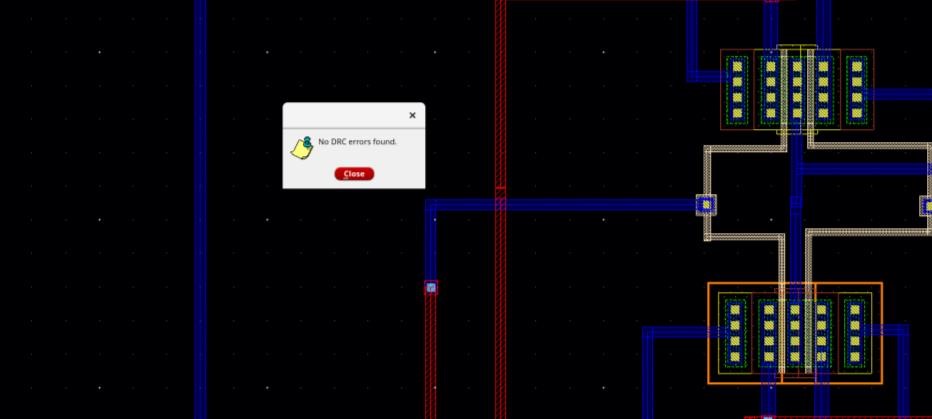


Figure 12: No DRC error in 4:1 mux

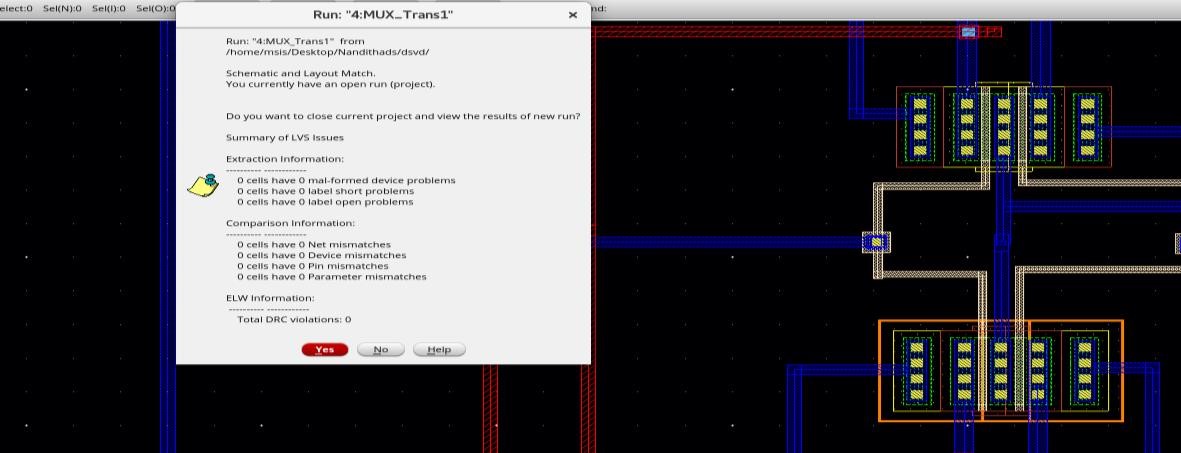


Figure 13: No LVS error in 4:1 MUX

