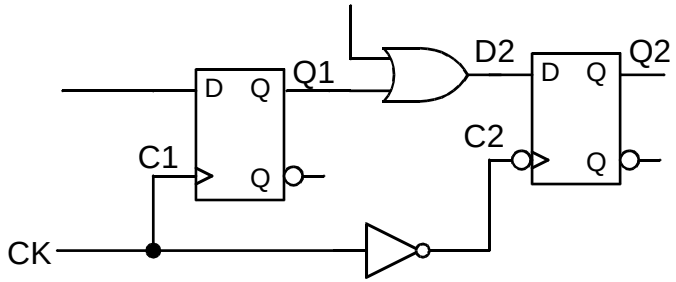
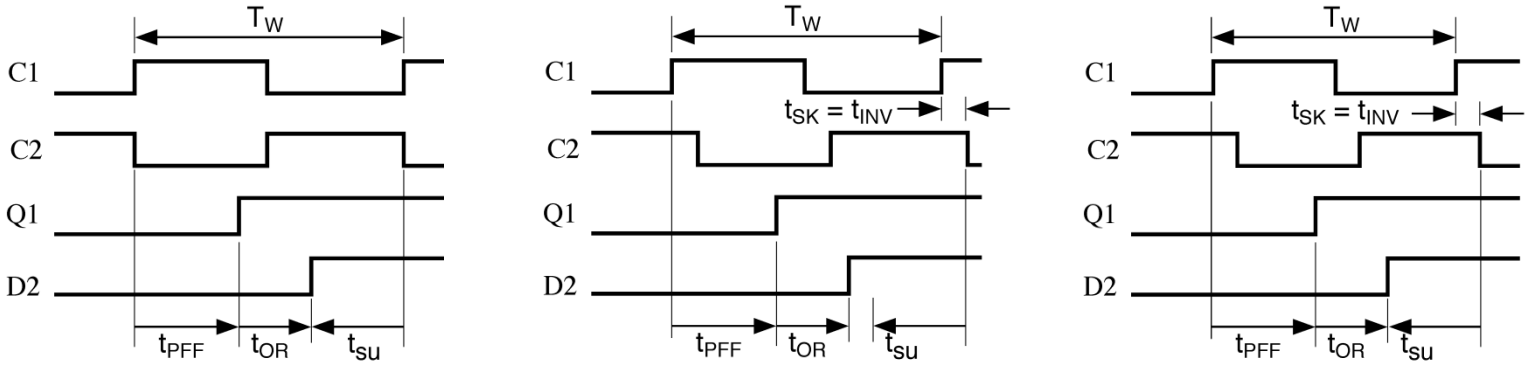
- Clock Skew
  - If a clock edge does not arrive at different flip-flops at exactly the same time, then the clock is said to be *skewed* between these flip-flops.
  - The difference between the times of arrival at the flip-flops is said to be the amount of *clock skew*.
  - Clock skew is due to different delays on different paths from the clock generator to the various flip-flops.
    - Different length wires (wires have delay)
    - Gates (buffers) on the paths
    - Flip-Flops that clock on different edges (need to invert clock for some flip-flops)
    - Gating the clock to control loading of registers

- Example (Effect of clock skew on clock rate)
  - Clock C2 skewed after C1

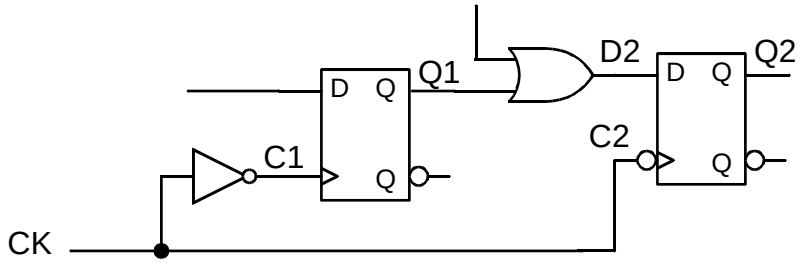


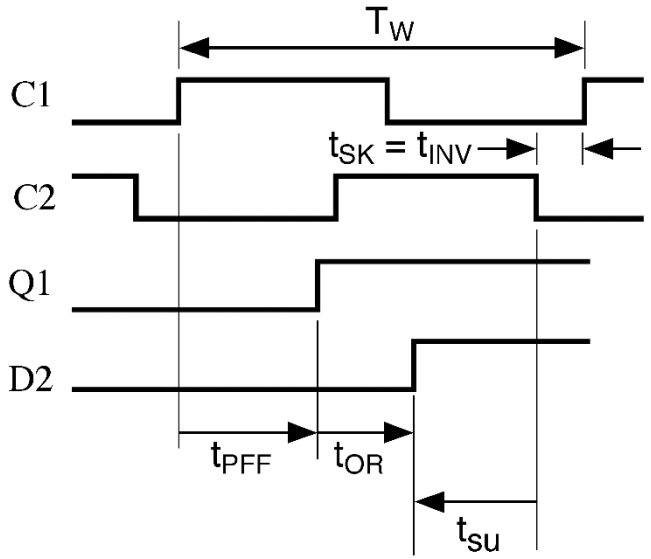


$T_W \geq \max T_{PFF} + \max t_{OR} + t_{su}$
(if clock not skewed, i.e., $t_{INV} = 0$)

$T_W \geq \max T_{PFF} + \max t_{OR} + t_{su} - \min t_{INV}$
(if clock skewed, i.e., $t_{INV} > 0$)

- Clock C1 skewed after C2

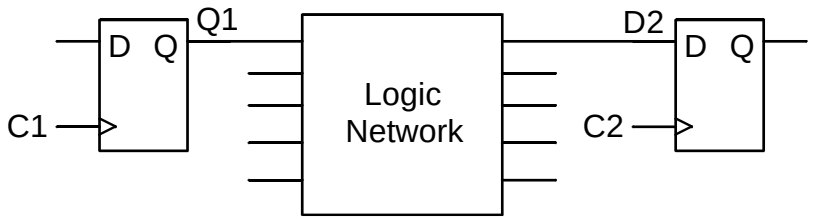


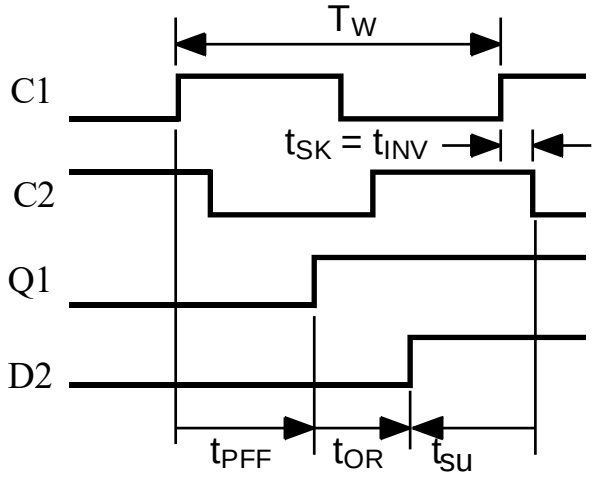


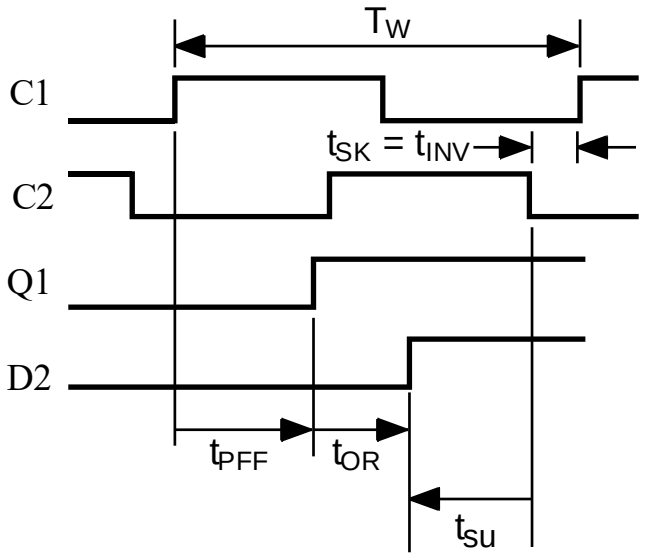
$T_W \geq \max T_{PFF} + \max t_{OR} + t_{su}$
(if clock not skewed, i.e., $t_{INV} = 0$)

$T_W \geq \max T_{PFF} + \max t_{OR} + t_{su} + \max t_{INV}$
(if clock skewed, i.e., $t_{INV} > 0$)

- Summary of maximum clock frequency calculations





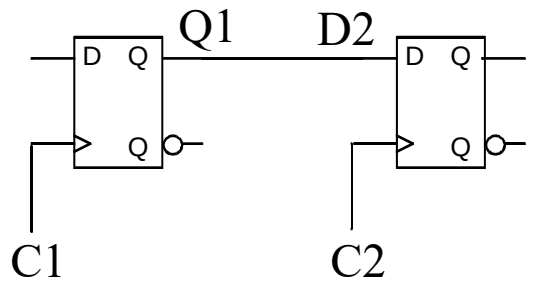


C2 skewed after C1: $T_W \geq \max T_{PFF} + \max t_{NET} + t_{su} - \min t_{INV}$

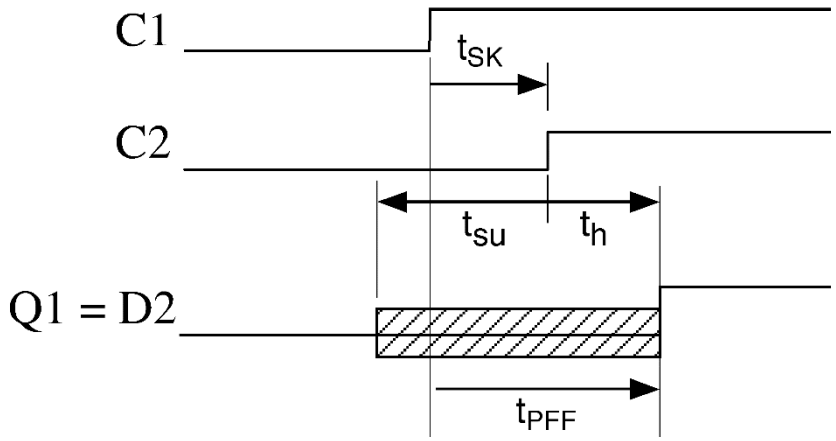
C2 skewed before C1: $T_W \geq \max T_{PFF} + \max t_{NET} + t_{su} + \max t_{INV}$

Maximum Allowable Clock Skew

- How much skew between C1 and C2 can be tolerated in the following circuit?



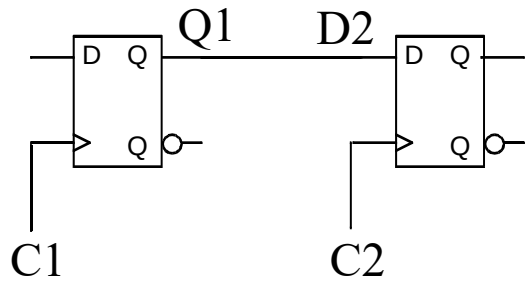
  - Case 1: C2 delayed after C1

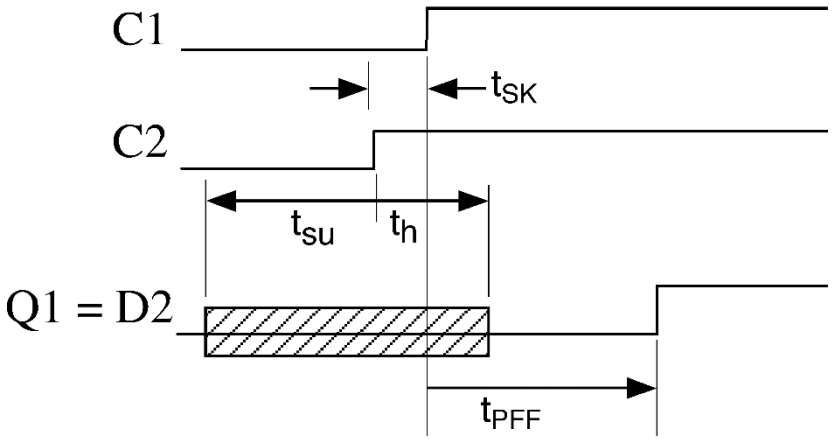


$$t_{PFF} > t_h + t_{SK}$$

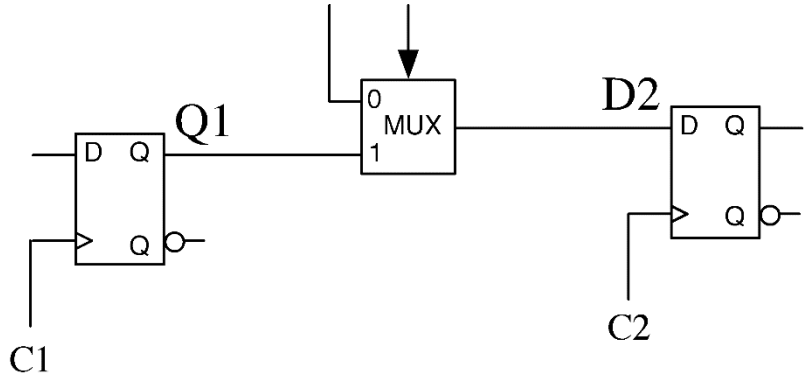
$$t_{SK} < \min t_{PFF} - t_h$$

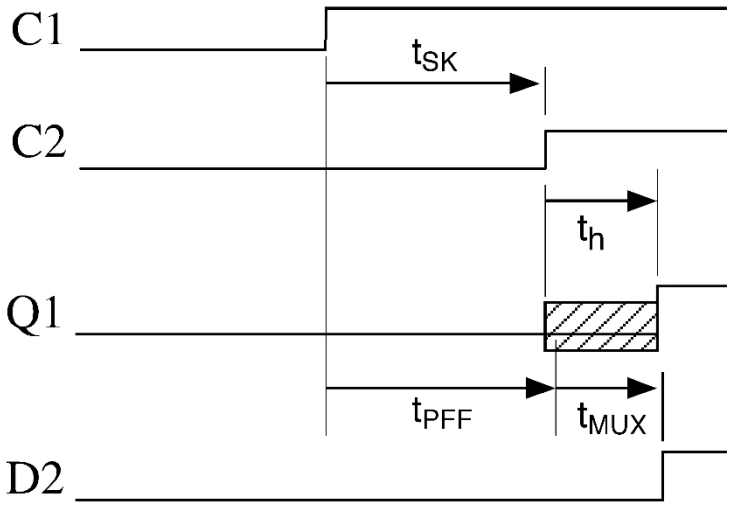
- Case 2: C1 delayed from C2





- How does additional delay between the flip-flops affect the skew calculations?

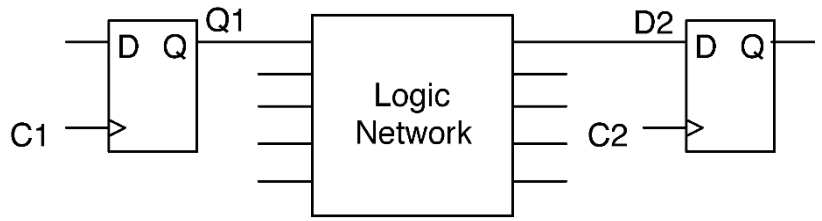


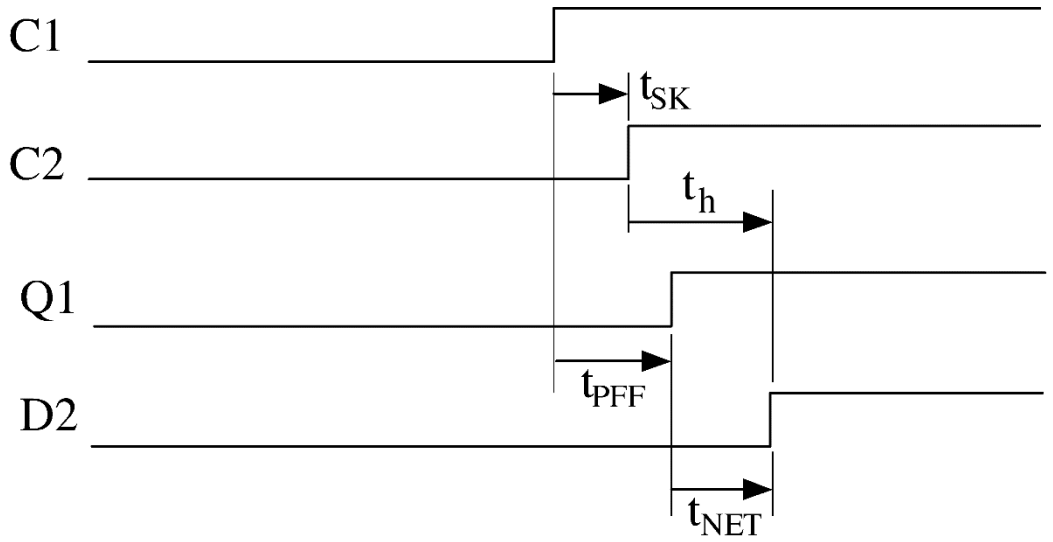


$$t_{SK} \leq \min t_{PFF} - t_h$$

$$t_{sk} \leq \min t_{PFF} + \min t_{MUX} - t_h$$

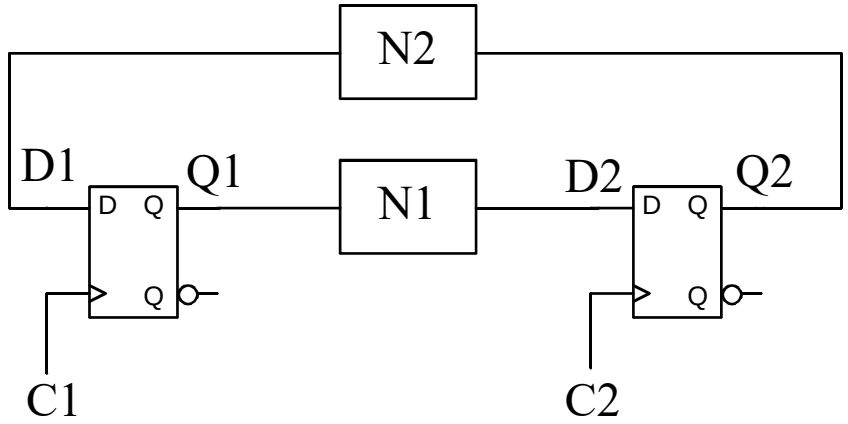
- Summary of allowable clock skew calculations

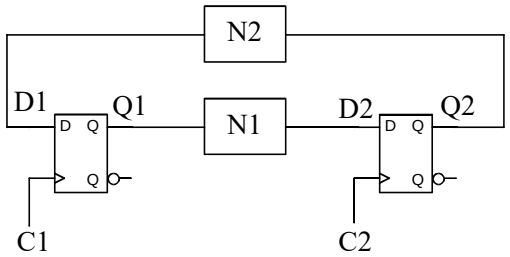




$$t_{SK} + t_h \leq t_{PFF} + t_{NET}$$
$$t_{SK} \leq \min t_{PFF} + \min t_{NET} - t_h$$

- Example: What is the minimum clock period for the following circuit under the assumption that the clock C2 is skewed after C1 (i.e., C2 is delayed from C1)?





- First calculate the maximum allowable clock skew.

$$t_{SK} < \min t_{PFF} + \min t_{N1} - t_h$$

- Next calculate the minimum clock period due to the path from Q1 to D2.

$$T_W > \max t_{PFF} + \max t_{N1} + t_{su} - \min t_{SK}$$

- Finally calculate the minimum clock period due to the path from Q2 to D1

$$T_W > \max t_{PFF} + \max t_{N2} + t_{su} + \max t_{SK}$$

$$T_W > \max t_{PFF} + \max t_{N2} + t_{su} + (\min t_{PFF} + \min t_{N1} - t_h)$$

$$T_W > \max t_{PFF} + \min t_{PFF} + \max t_{N2} + \min t_{N1} + t_{su} - t_h$$

Exercises

1. **Draw a divide by 2 circuit using D FF. What is the maximum clock frequency at which you can operate the circuit, given that Setup and hold times of the FF are 5 ns and 2 ns respectively. The propagation delay of the FF is 10 ns ?**

- Setup time = 5ns
- Hold time = 2ns
- reg to reg delay is :

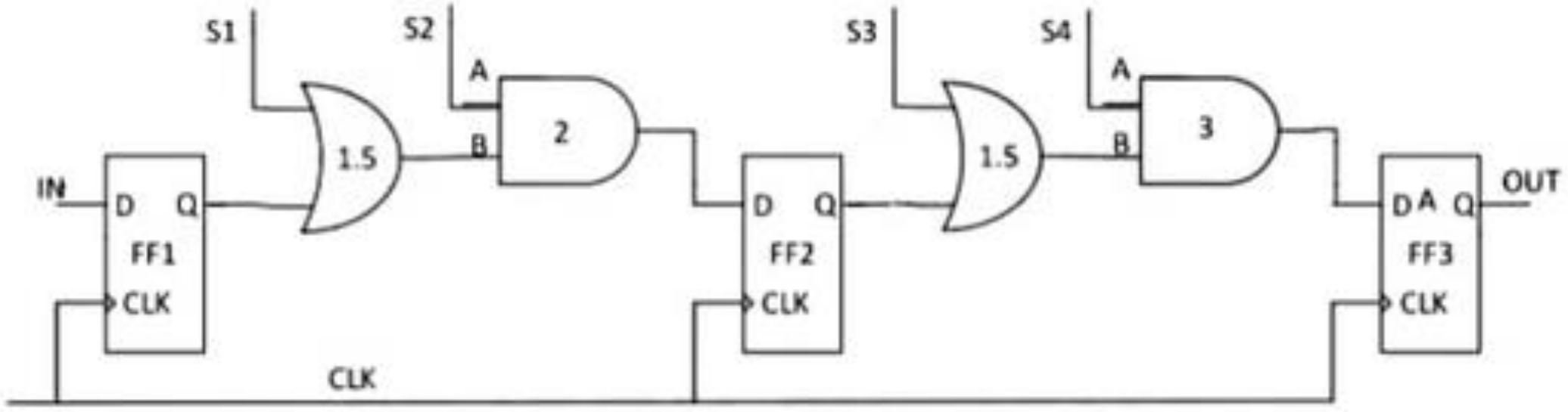
  = tcq+setup time

  = 10+5 => 15ns

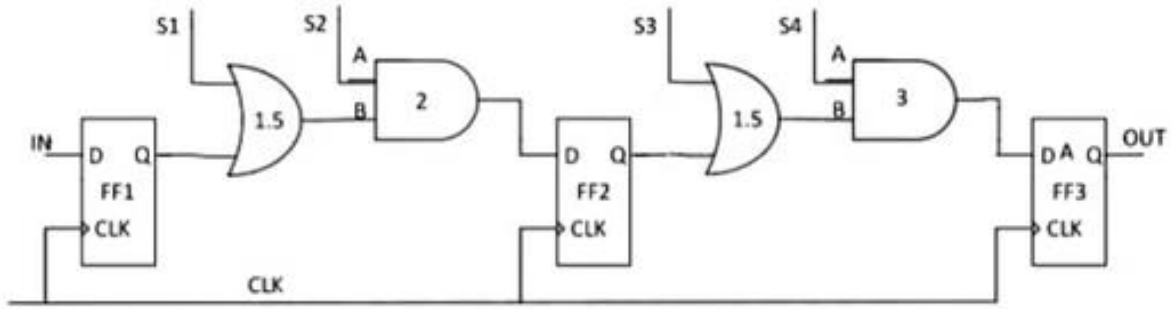
  = 1/15 => 66.67MHz

Assignments - STA

- For each of the flip-flops, the CLK to Q delay is 1ns, and setup time requirement is 0.5ns. The hold time requirement at each flip-flop is 0.25ns.
- Assume that the numbers indicated within each gate are the propagation delays of the gates in ns.
- Obtain max possible clock frequency for which the circuit will function properly ?



For each of the flip-flops, the CLK to Q delay is 1ns, and setup time requirement is 0.5ns. The hold time requirement at each flip-flop is 0.25ns. Assume that the numbers indicated within each gate are the propagation delays of the gates in ns. Obtain what will be the max possible clock frequency for which the circuit will function properly ?



Step 1 : FF1 TO FF2 (Reg2Reg Delay)

= Tc2q+1.5+2+Tsetup
= 1+1.5+2+0.5
= 5ns

Step 2 : FF2 TO FF3 (Reg2Reg Delay)

= Tc2q+1.5+3+Tsetup

= 1+1.5+3+0.5

= 6ns

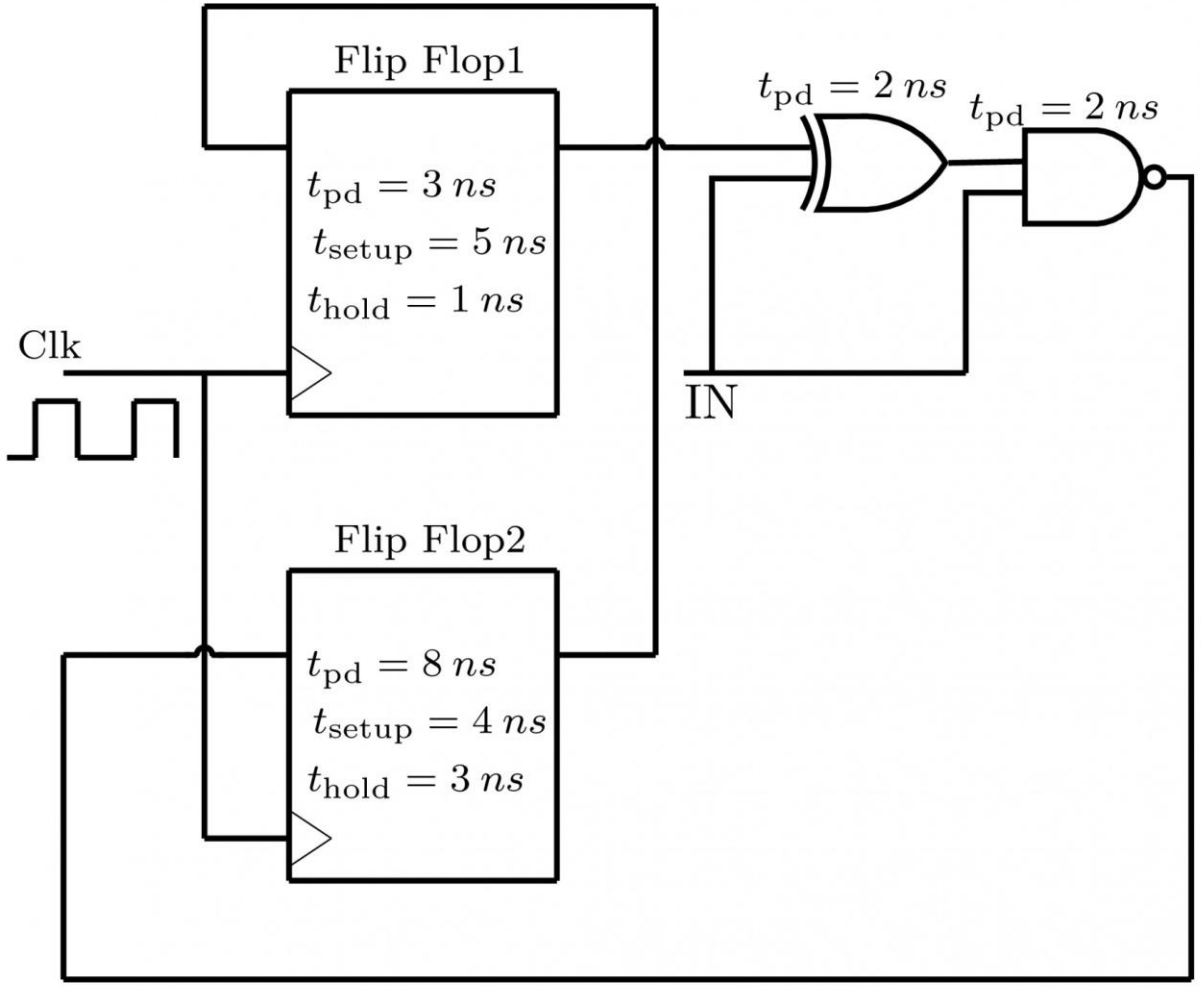
Max Possible Clock Frequency = 1/Max(Reg2Reg_delay)

= 1/Max(5,6)

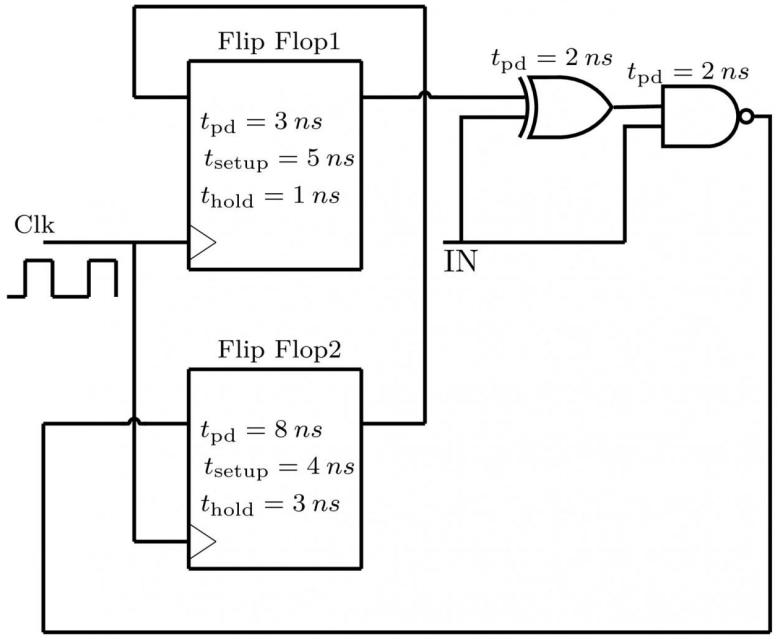
= 1/6

= 16.67MHz

3. **What is the total delay of the circuit given below ? (Tpd_ff1 =3ns , Tsetup_ff1 =5ns ,thold_ff1 =1ns ,Tpd_ff2 =8ns , Tsetup_ff1 =4ns ,thold_ff1 =3ns**



What is the total delay of the circuit given below ? (Tpd_ff1 =3ns , Tsetup_ff1 =5ns ,thold_ff1 =1ns ,Tpd_ff2 =8ns , Tsetup_ff1 =4ns ,thold_ff1 =3ns



Path 1: FF1 to FF2

delay = Tpd_ff1+Tpd_exor+Tpd_nand+Tsetup_ff2

= 3+2+2+4

= 11ns

Path 2: FF2 to FF1

delay = Tpd_ff2+Tsetup_ff1

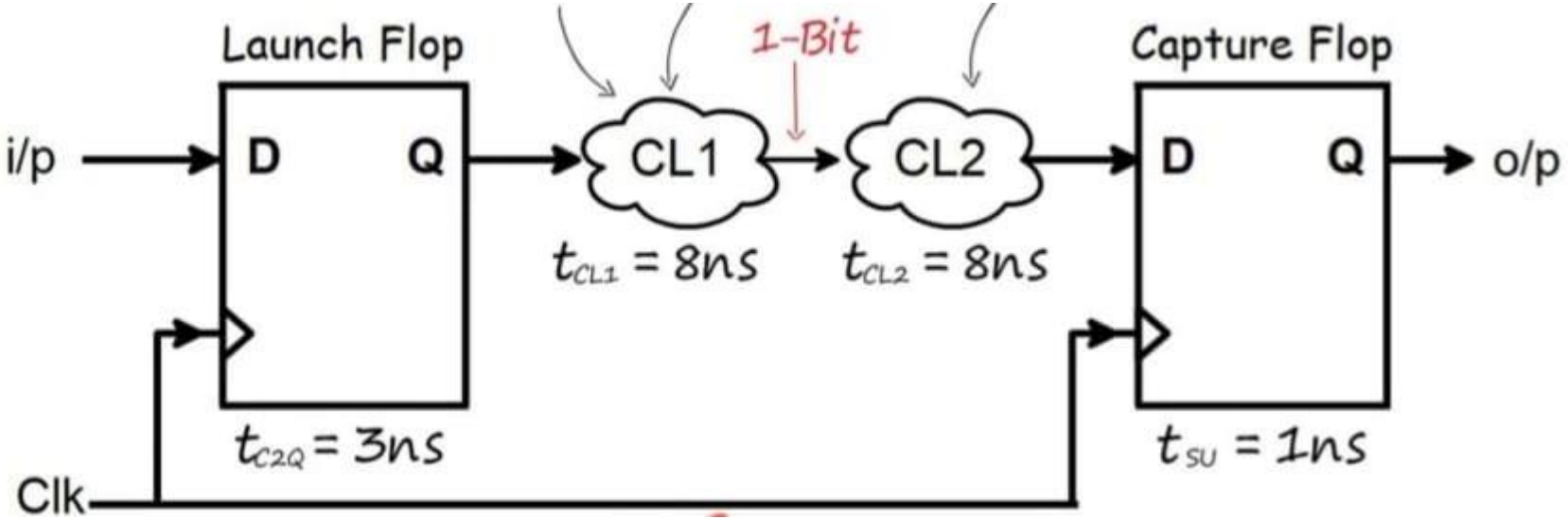
= 8+5

= 13ns

Delay = max(path1,path2)

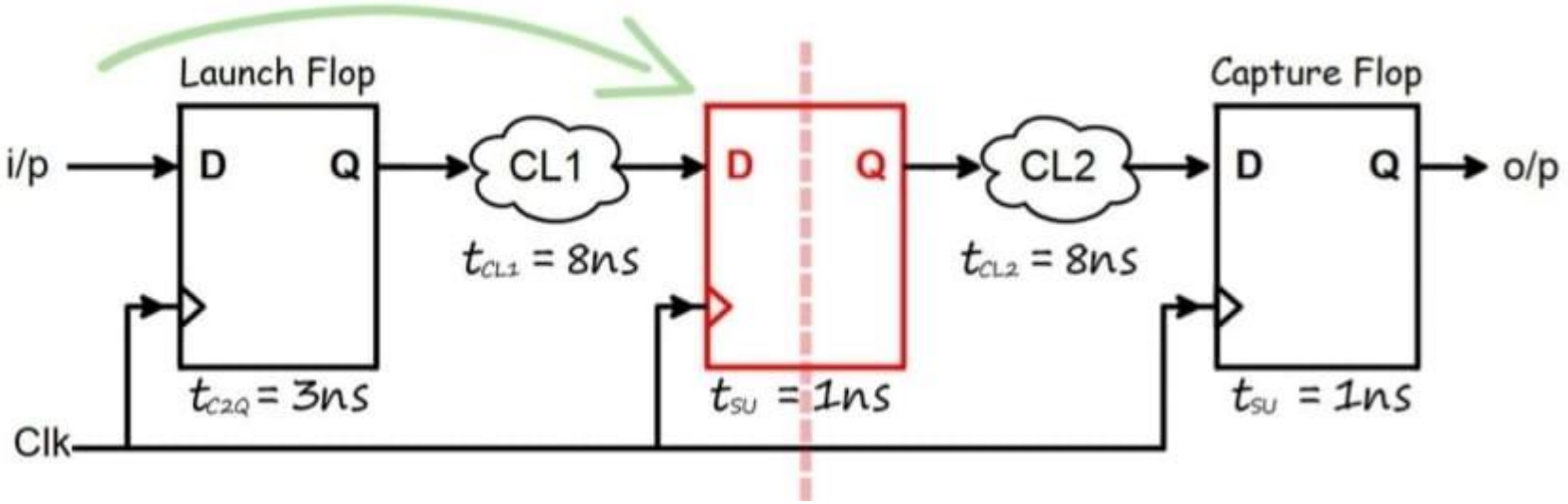
= 13ns

4. Calculate the minimum time period and maximum clock frequency at which the given circuit can operate ?



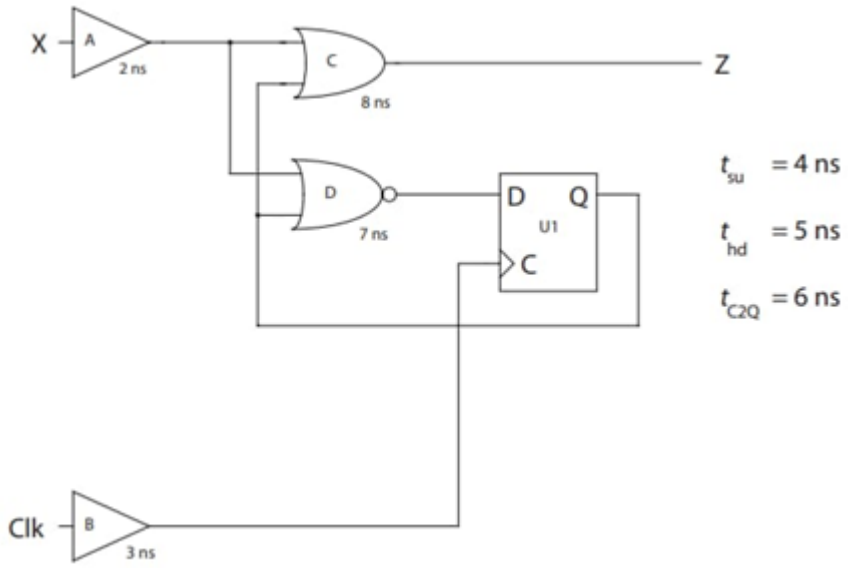
Consider, Tc2q+Tcl1+tcl2
3+8+8 < Tmin-1
19 < Tmin-1
Tmin =20ns
Fmax = 1/20
= 50MHz

5. **Can you operate the given circuit at some frequency higher than the max frequency you've calculated. If yes, then what modifications are required in** the **design ?**



Tc2q+Tcl1< Tmin-Tsetup
3+8 < Tmin -1
Tmin = 12ns
Fmax = 1/12
= 83.33MHz

6. Find out Hold Slack for the given Circuit below ?

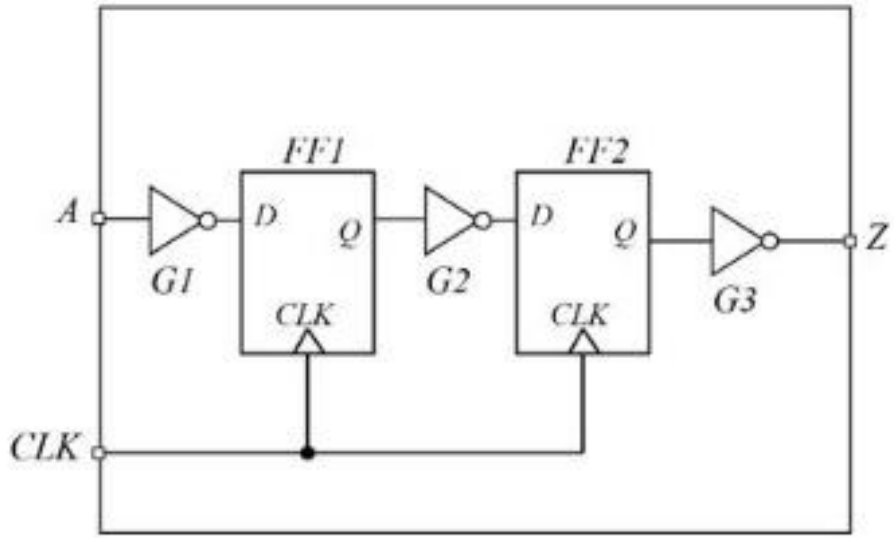


- Hold slack = Arrival time - Required time
- Arrival Time = Tclk_q+T_comb
  = 6+7 = 13ns

- Required Time = Thold+Tskew
  = 5+0, Assume Tskew is 0ns
  = 5ns
- Hold slack = 13-5 =8ns

7. **Setup time=45 ps, hold time=10 ps, and CLK-to-Q delay=20 ps. The delay of each inverter is 50 ps. Ignore the wire delay.**

- **Assume that the period of the clock is 1000 ps. What is the setup slack at the timing end-point FF2/D?**



Setup Slack = Required time - Arrival time

Required time = Tclk-Tsetup+Tskew

= 1000-45+0

= 955ps

Arrival Time = Tclk_q+Tcomb

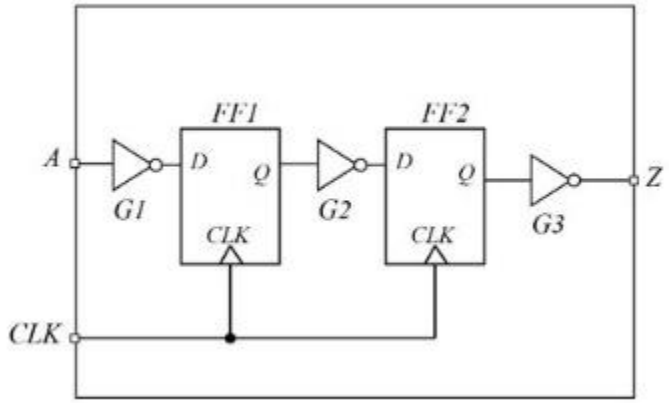
= 20+50

= 70ps

Setup Slack = 955 - 70 = 885ps

8. **Find the hold slack at the timing end-point FF2/D?The following attributes are valid for the flip-flops FF1 and FF2: setup time=45 ps, hold time=10 ps, and CLK-to-Q delay=20 ps.**

- **The delay of each inverter is 50 ps. Ignore the wire delay?**



Hold Slack = Arrival time - Required time

Arrival Time = Tclk_q+Tcomb

= 20 +50 = 70ps

Required Time = Thold+Tskew

= 10+0 = 10ps

Hold Slack = 70 - 10 =60ps