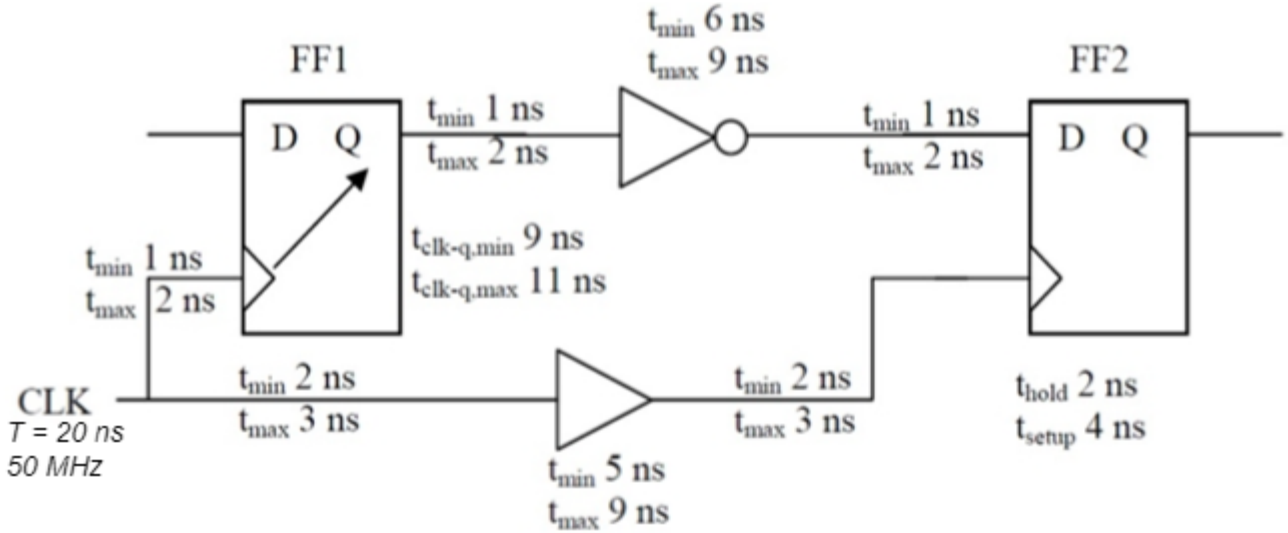
Example: Setup

Calculate Maximum Frequency



- Setup Slack = -1 ns

Setup slack: mln delay along clock path – max delay along data path = 25 – 26 = -1 ns

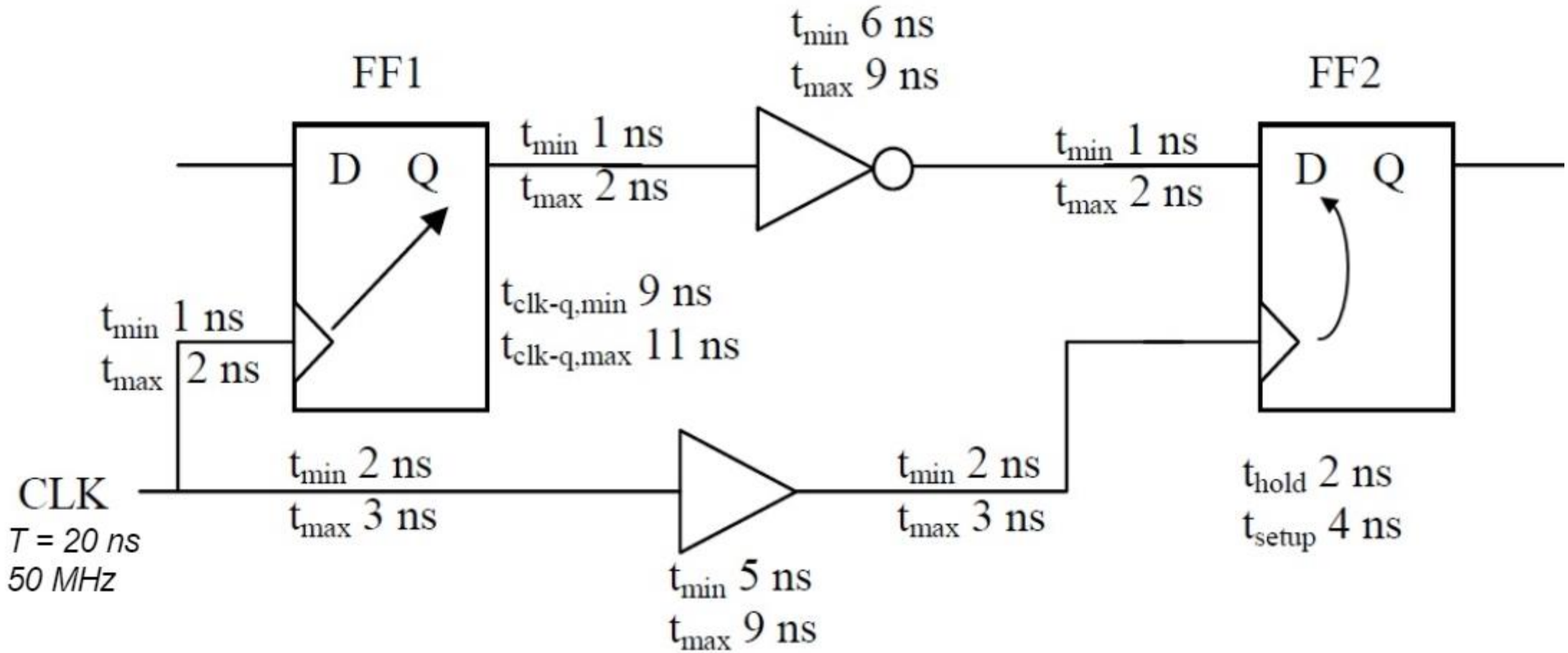
- Make the period 1 ns longer, 20+1 = new period = 21 ns

- $T_{min} = DAT_{max} + t_{su} - t_{clk,min} = 26+4-9=21$ ns

  = Data Arrival Time + setup time of destination reg – clock delay to destination reg

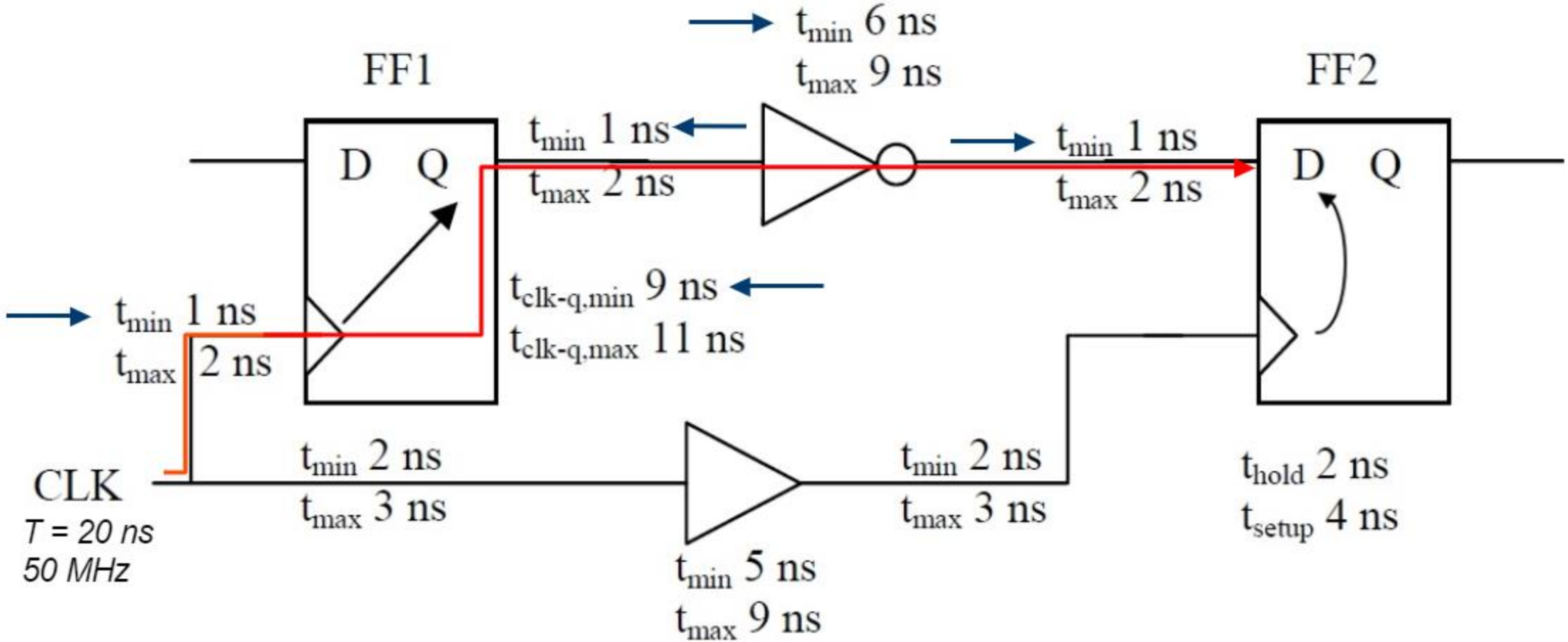
- $f_{max} = 1/T_{min} = 1/21 = 47.6$ MHz

Example: Hold



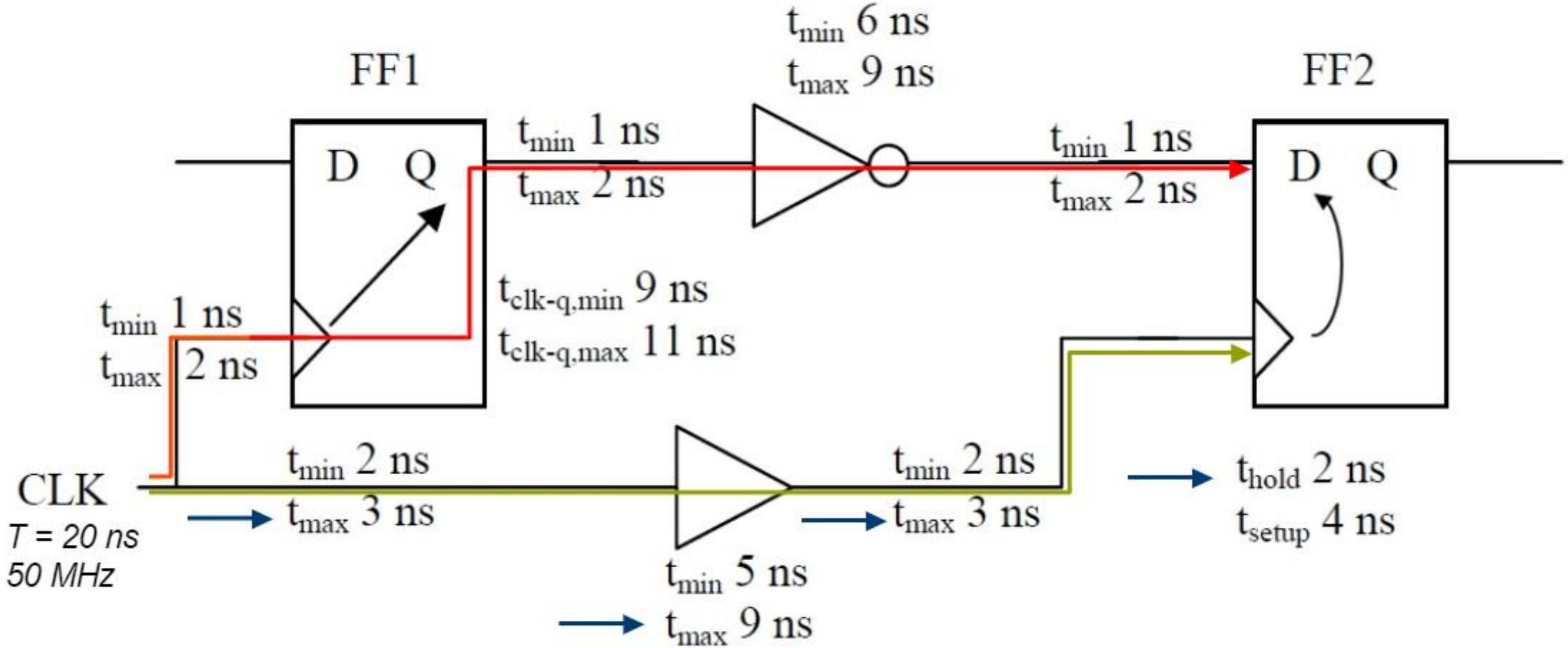
Hold slack: min delay along data path (min data arrival time) – max delay along clock path (max data required time) =

Example: Hold



Hold slack: min delay along data path – max delay along clock path = (1+9+1+6+1) –
(min data arrival time) (max data required time)

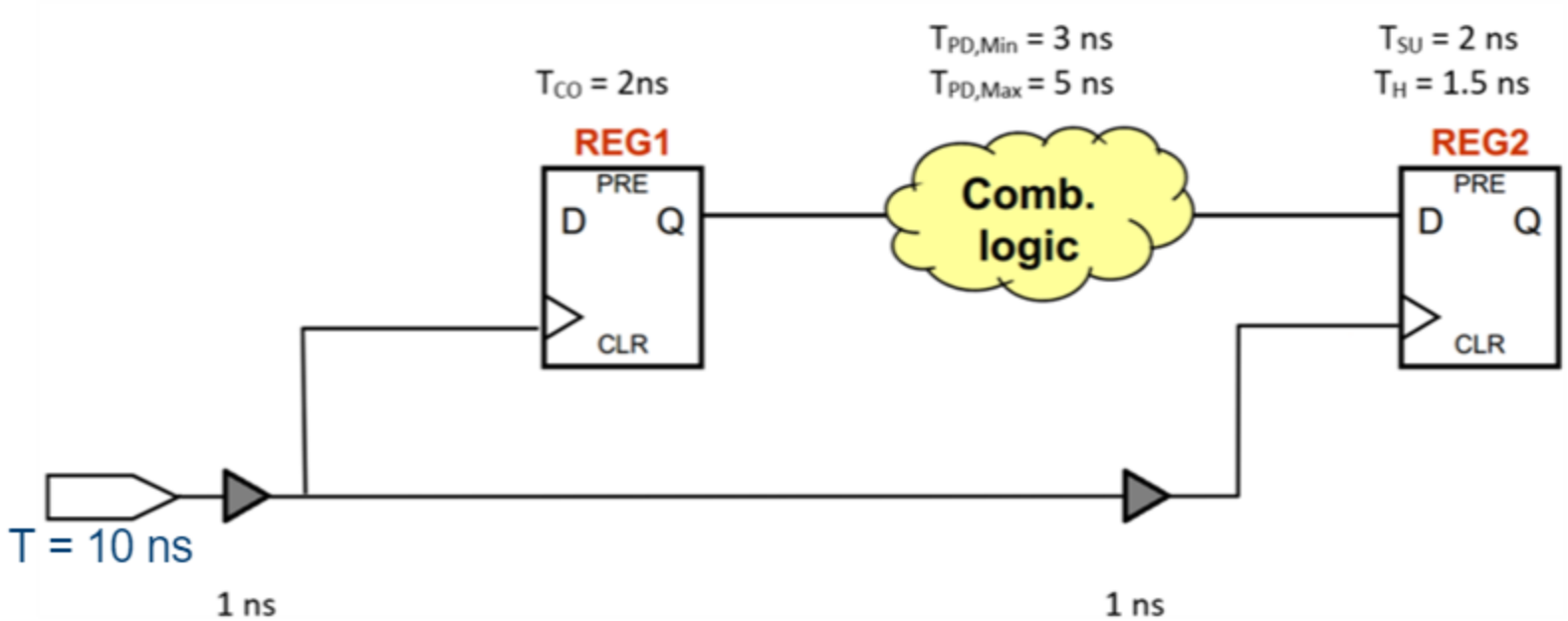
Example: Hold



Hold slack: min delay along data path – max delay along clock path = (1+9+1+6+1) – (3+9+3+2) = 18-17 = 1 ns
(min data arrival time) (max data required time)

Problem

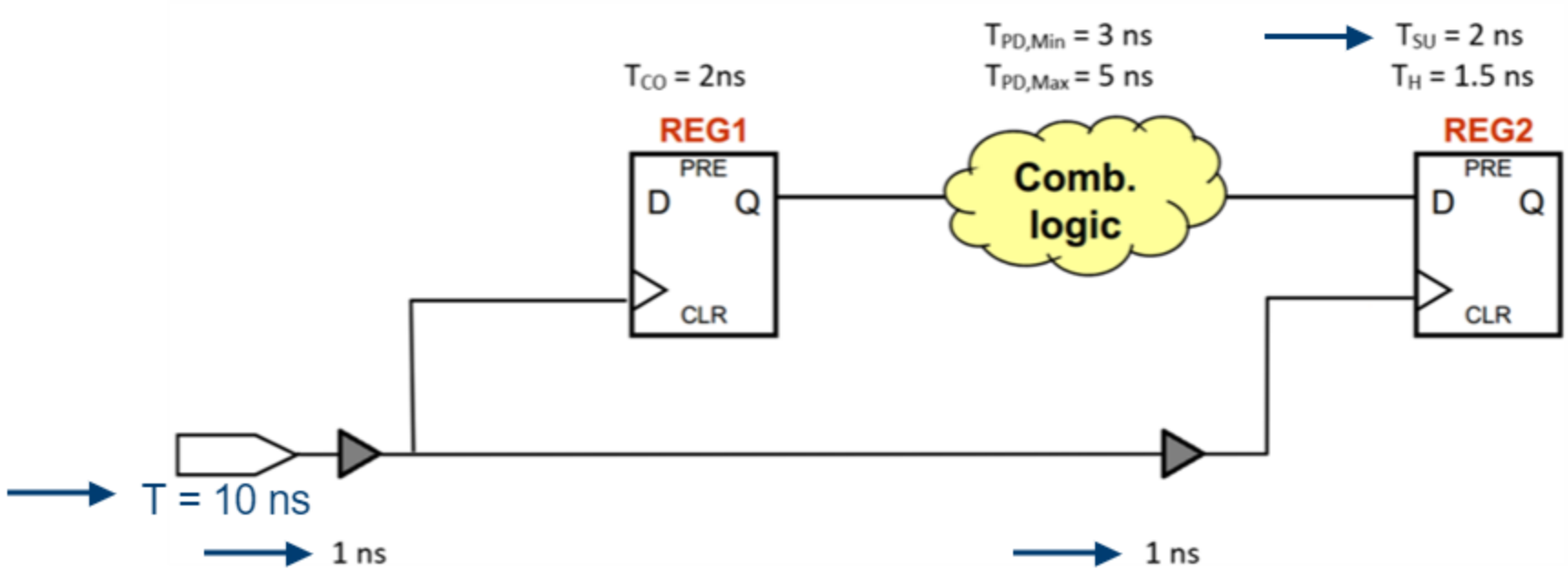
Exercise 1(a)



Setup Slack = min DRT – max DAT =

Solution

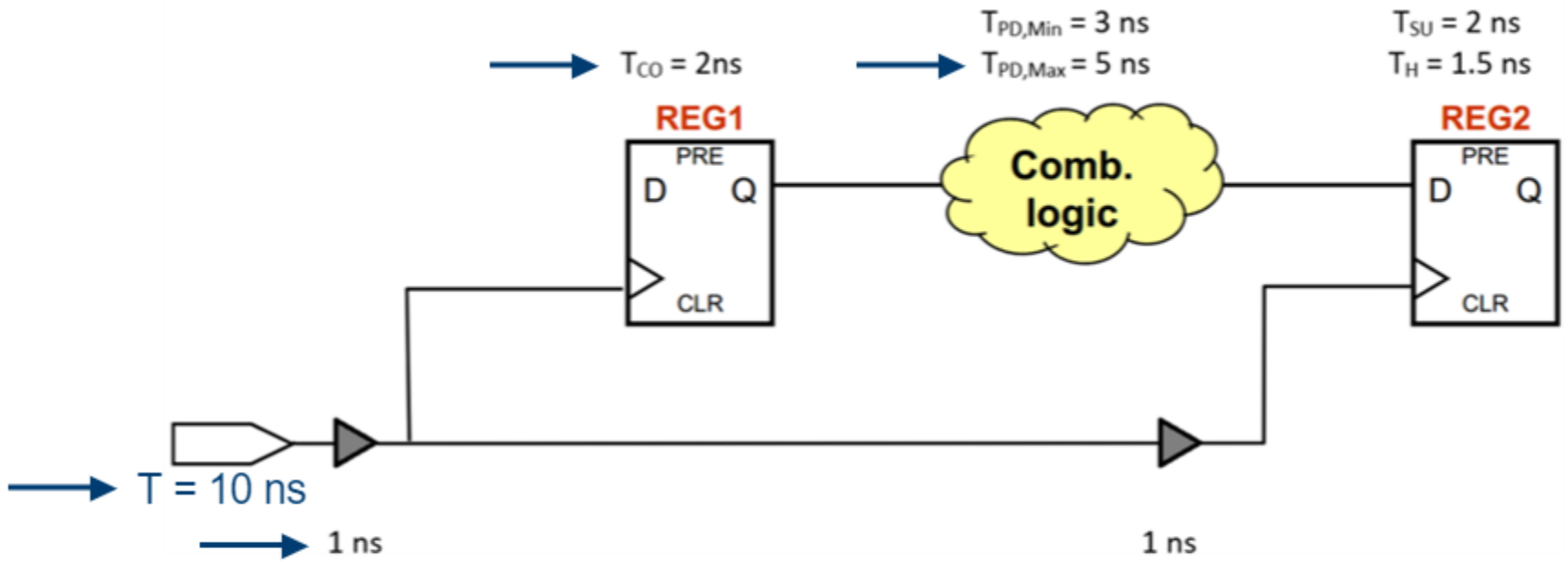
Exercise 1(a)



Setup Slack = min DRT – max DAT = (10 + 1 + 1 - 2)

Solution

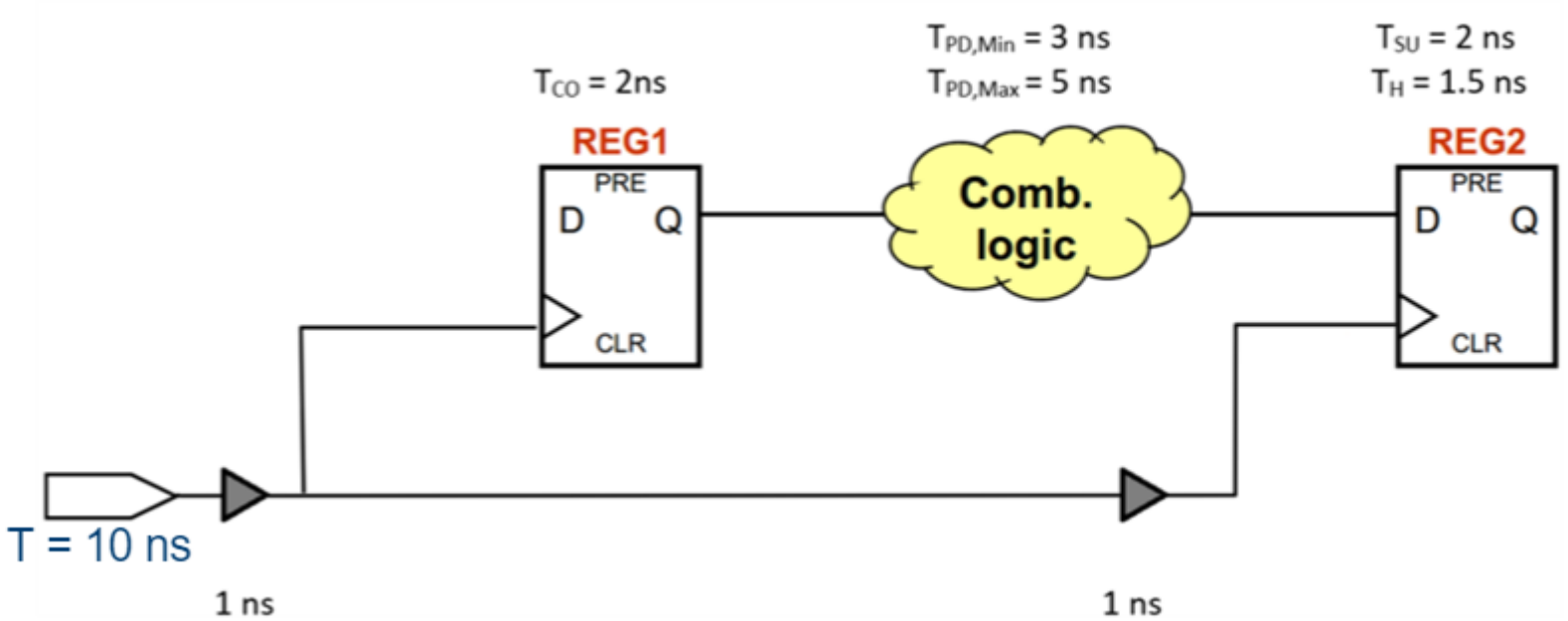
Exercise 1(a)



Setup Slack = min DRT – max DAT = (10 + 1 + 1 - 2) – (1 + 2 + 5) = 2 ns

Solution

Exercise 1(a)

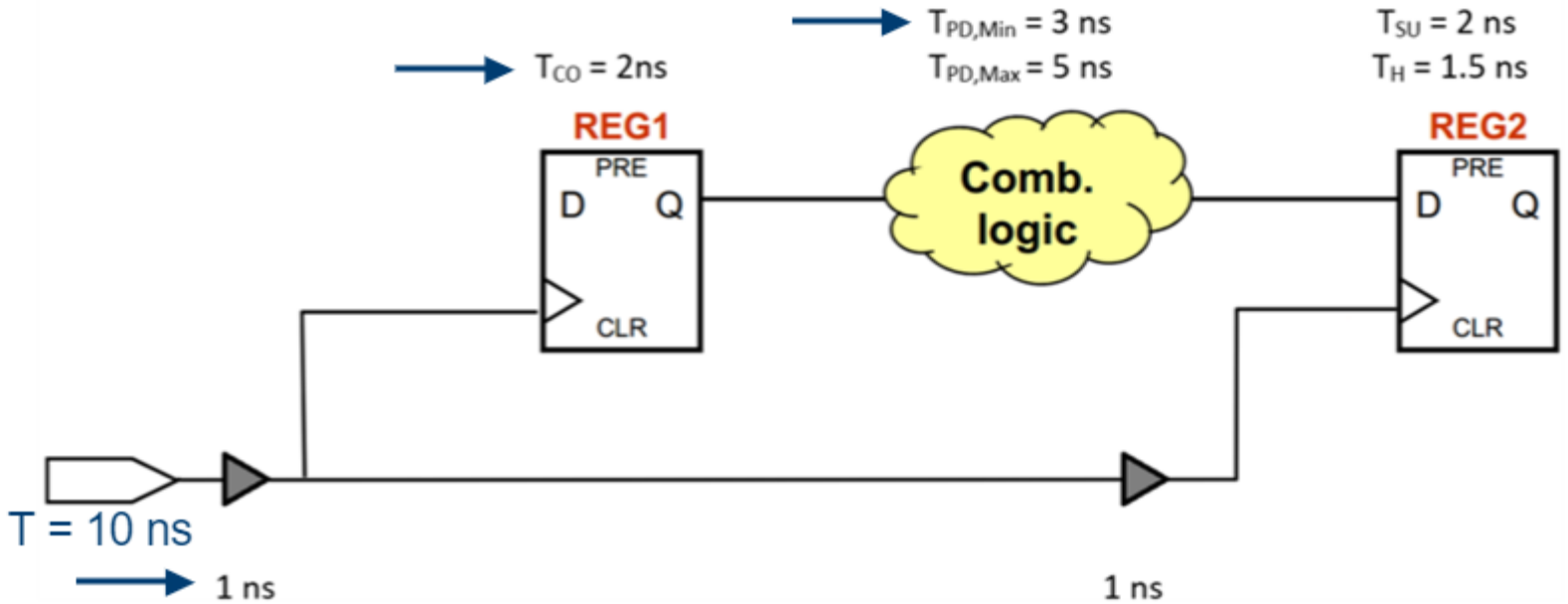


Setup Slack = min DRT – max DAT = (10 + 1 + 1 - 2) – (1 + 2 + 5) = 2 ns

Hold Slack = min DAT – max DRT =

Solution

Exercise 1(a)

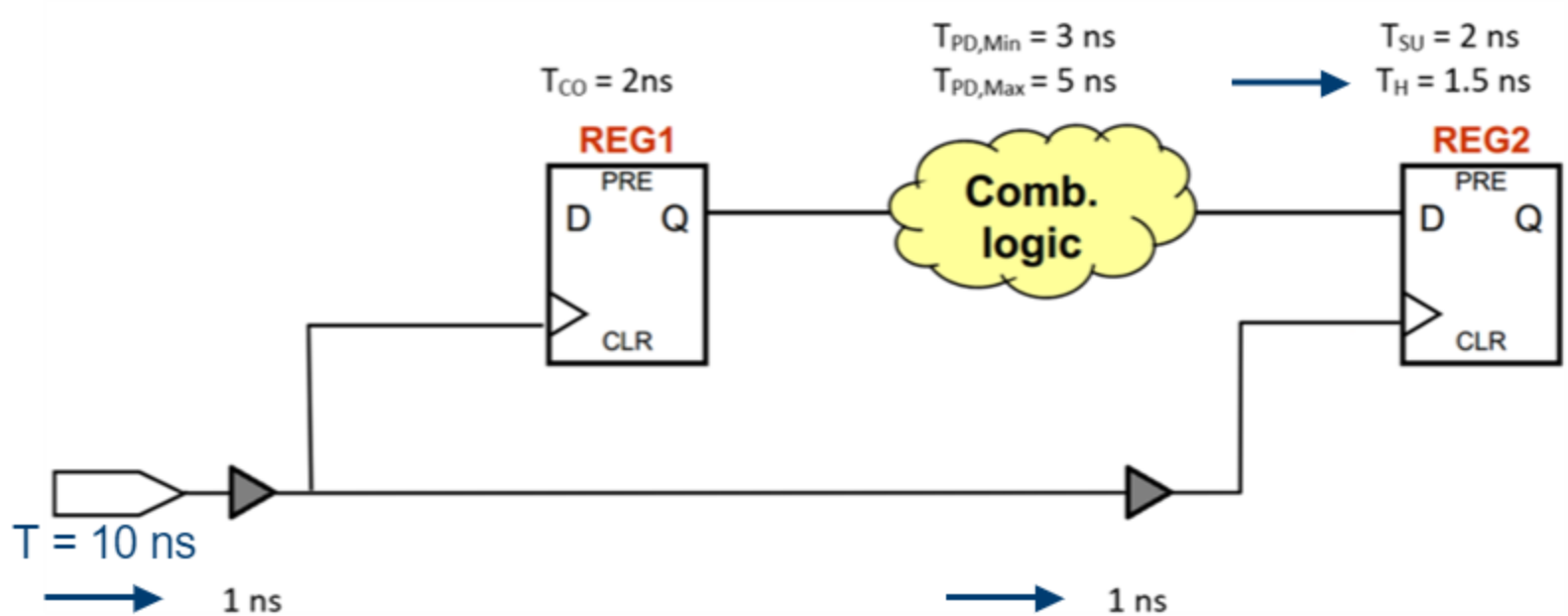


Setup Slack = min DRT – max DAT = (10 + 1 + 1 - 2) – (1 + 2 + 5) = 2 ns

Hold Slack = min DAT – max DRT = (1 + 2 + 3)

Solution

Exercise 1(a)

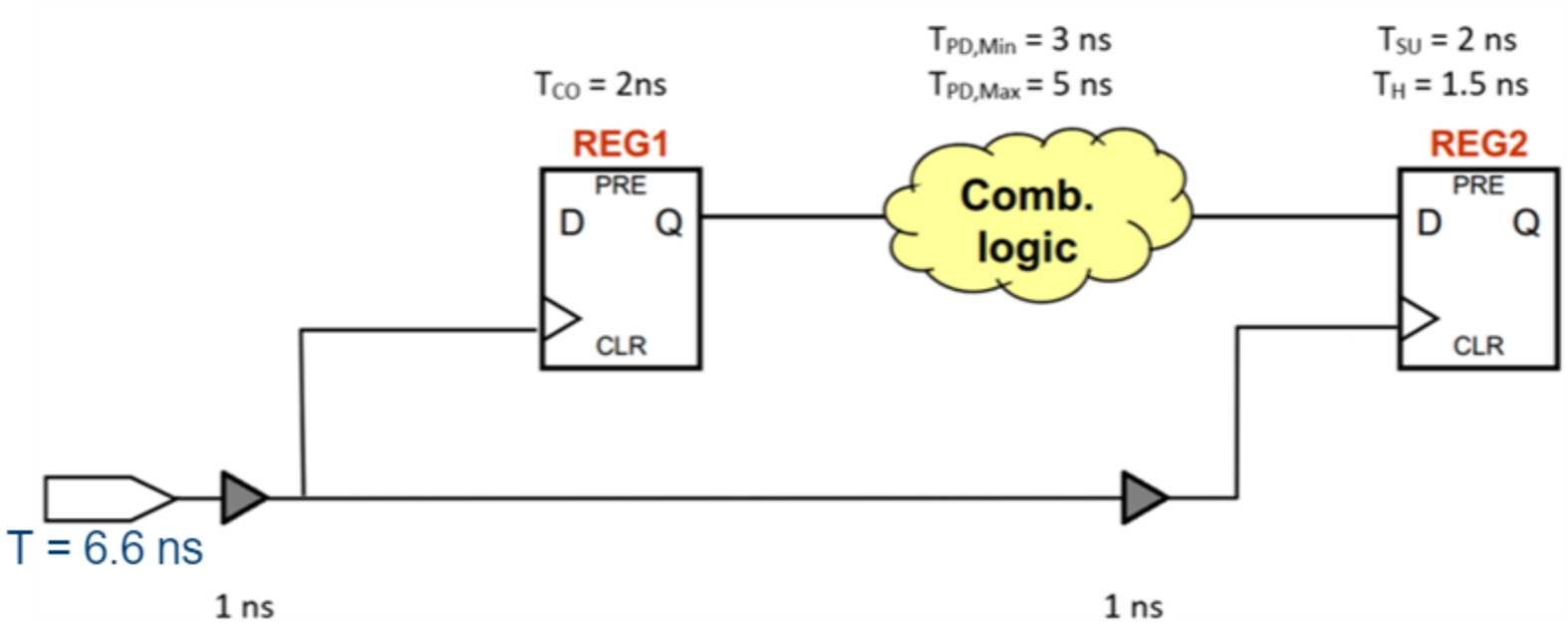


Setup Slack = min DRT – max DAT = (10 + 1 + 1 - 2) – (1 + 2 + 5) = 2 ns

Hold Slack = min DAT – max DRT = (1 + 2 + 3) – (1 + 1 + 1.5) = 2.5 ns

Solution

Exercise 1(b)

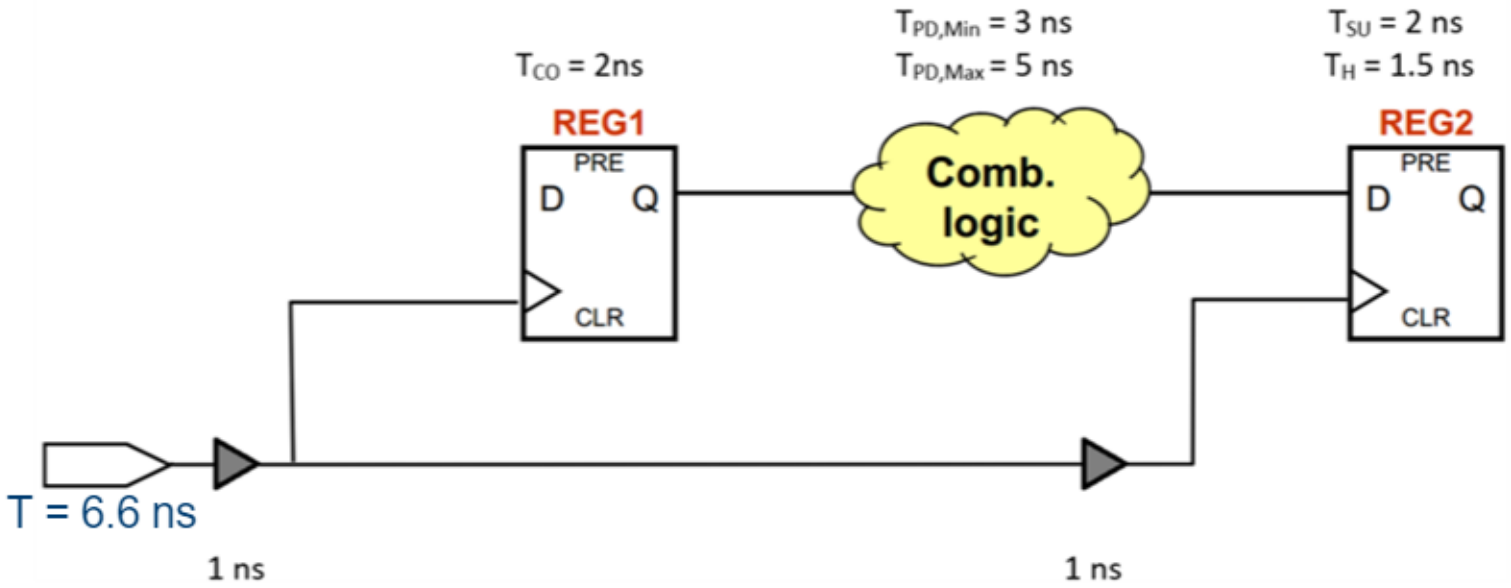


Setup Slack = min DRT – max DAT =

Hold Slack = min DAT – max DRT =

Solution

Exercise 1(b)



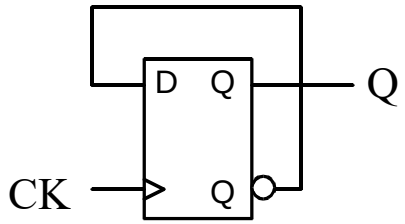
Setup Slack = min DRT – max DAT = (6.6 + 1 + 1 - 2) – (1 + 2 + 5) = **-1.4 (Fails!)**

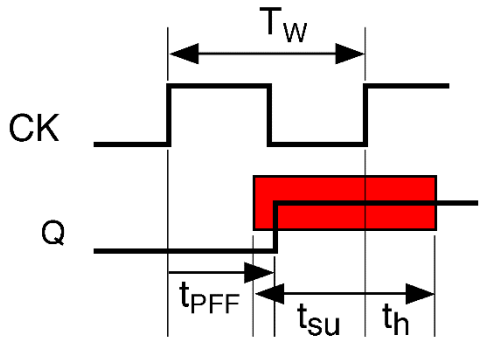
Hold Slack = min DAT – max DRT = (6.6 + 1 + 2 + 3) – (6.6 + 1 + 1 + 1.5) = 2.5 ns
(Doesn't change!)

Maximum Clock Frequency

- The clock frequency for a synchronous sequential circuit is limited by the timing parameters of its flip-flops and gates.
- This limit is called *the maximum clock frequency* for the circuit.
- The *minimum clock period* is the reciprocal of this frequency.
- Relevant timing parameters
  - Gates:
    - Propagation delays: min t_{PLH}, min t_{PHL}, max t_{PLH}, max t_{PHL}
  - Flip-Flops:
    - Propagation delays: min t_{PLH}, min t_{PHL}, max t_{PLH}, max t_{PHL}
    - Setup time: t_{su}
    - Hold time: t_h

- Example





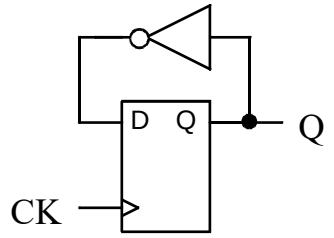
$$T_W \geq \max t_{PFF} + t_{su}$$

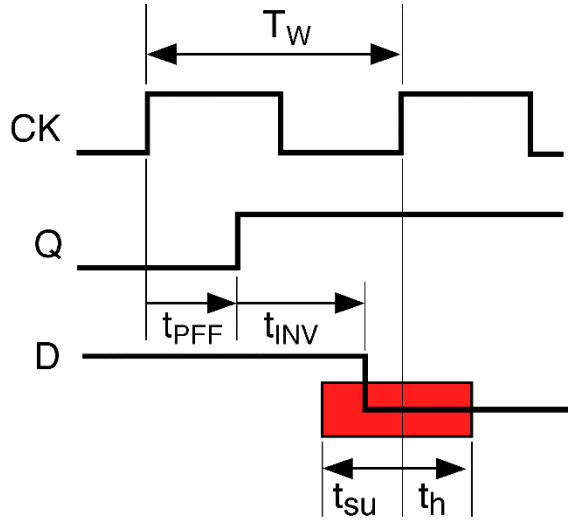
- Assume, max t_{PLH} = 25ns, max t_{PHL} = 40ns, t_{su} = 20ns

$T_W \geq \max (\max t_{PLH} + t_{su,} \max t_{PHL} + t_{su})$

$T_W \geq \max (25+20, 40+20) = 60$

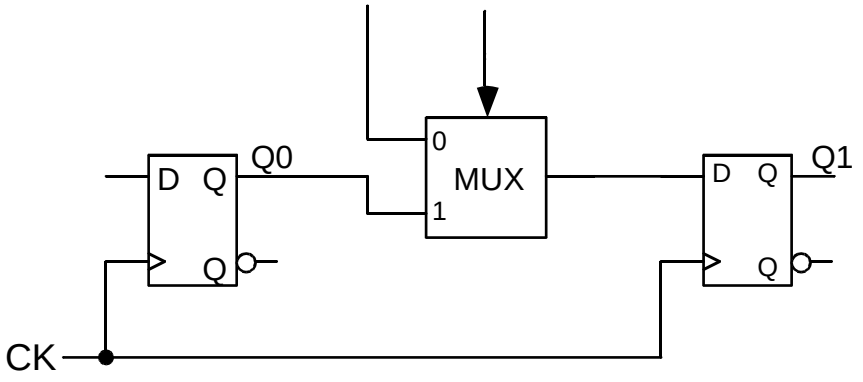
- Example

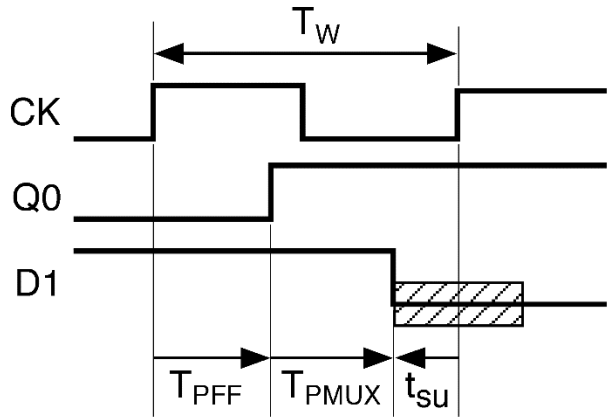




$$T_W \geq \max t_{PFF} + \max t_{PINV} + t_{su}$$

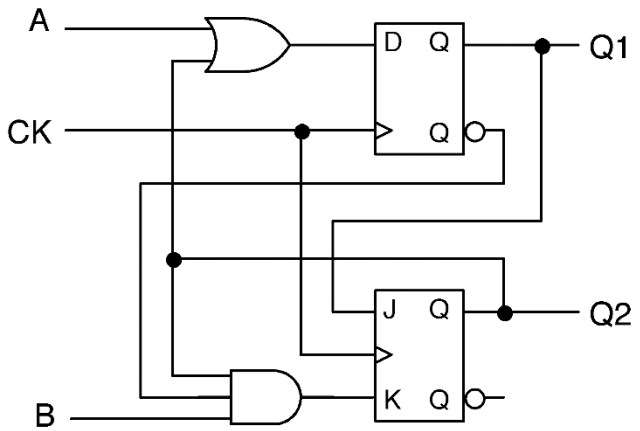
- Example





$$T_W \geq \max t_{PFF} + \max t_{PMUX} + t_{su}$$

- Example



	t_P	t_{su}
D Flip-Flop:	20 ns	5 ns
JK Flip-Fllp:	25 ns	10 ns
AND Gate:	12 ns	
OR Gate:	10 ns	

Paths from Q1 to Q1: None

Paths from Q1 to Q2: $T_W \geq \max t_{PDFF} + t_{JKsu} = 20 + 10 = 30$ ns

$T_W \geq \max t_{PDFF} + \max t_{AND} + t_{JKsu} = 20 + 12 + 10 = 42$ ns

Paths from Q2 to Q1: $T_W \geq \max t_{PJKFF} + t_{OR} + T_{Dsu} = 25 + 10 + 5 = 40$ ns

Paths from Q2 to Q2: $T_W \geq \max t_{PJKFF} + \max t_{AND} + t_{JKsu} = 25 + 12 + 10 = 47$ ns

$$T_W \geq 47 \text{ ns}$$