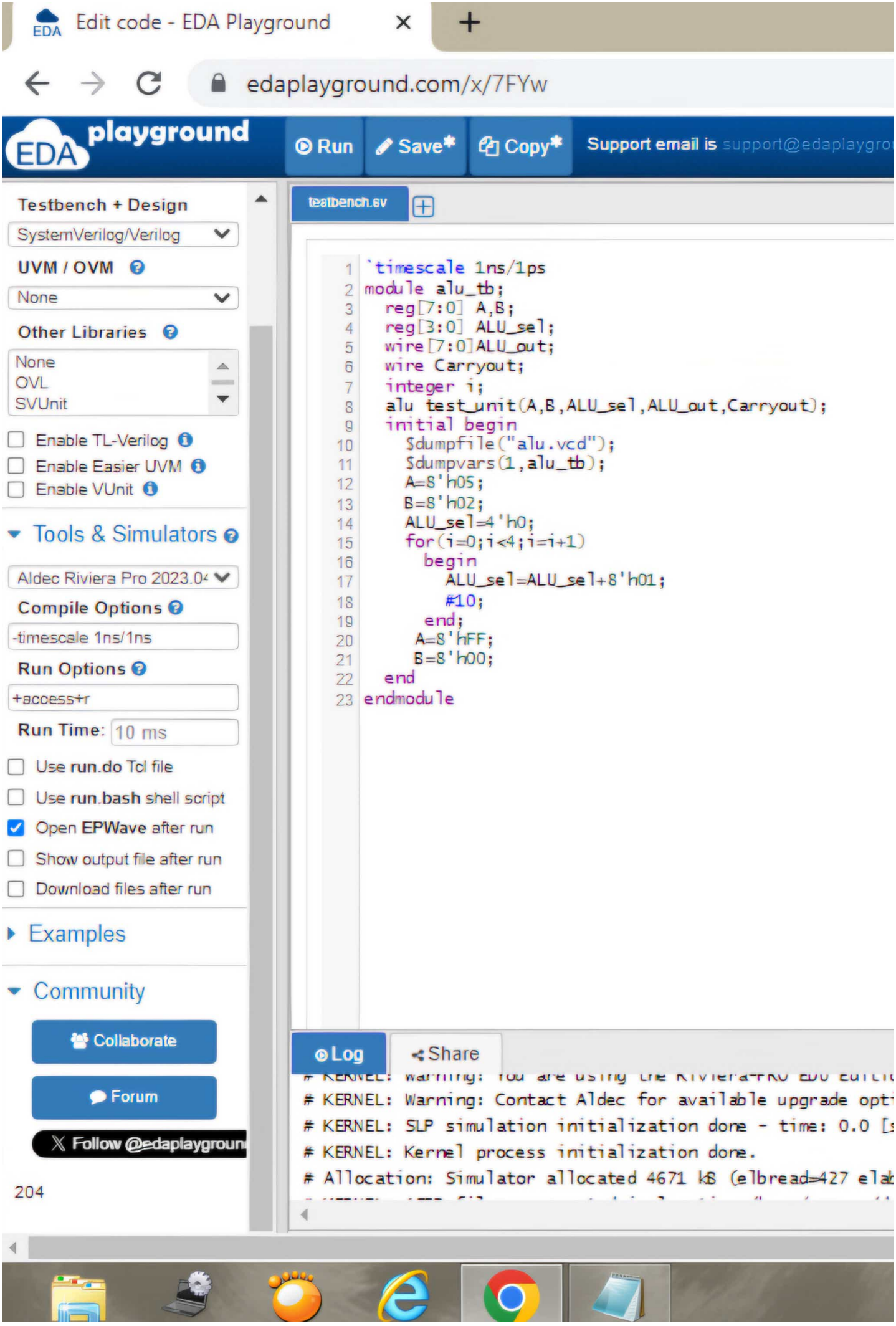
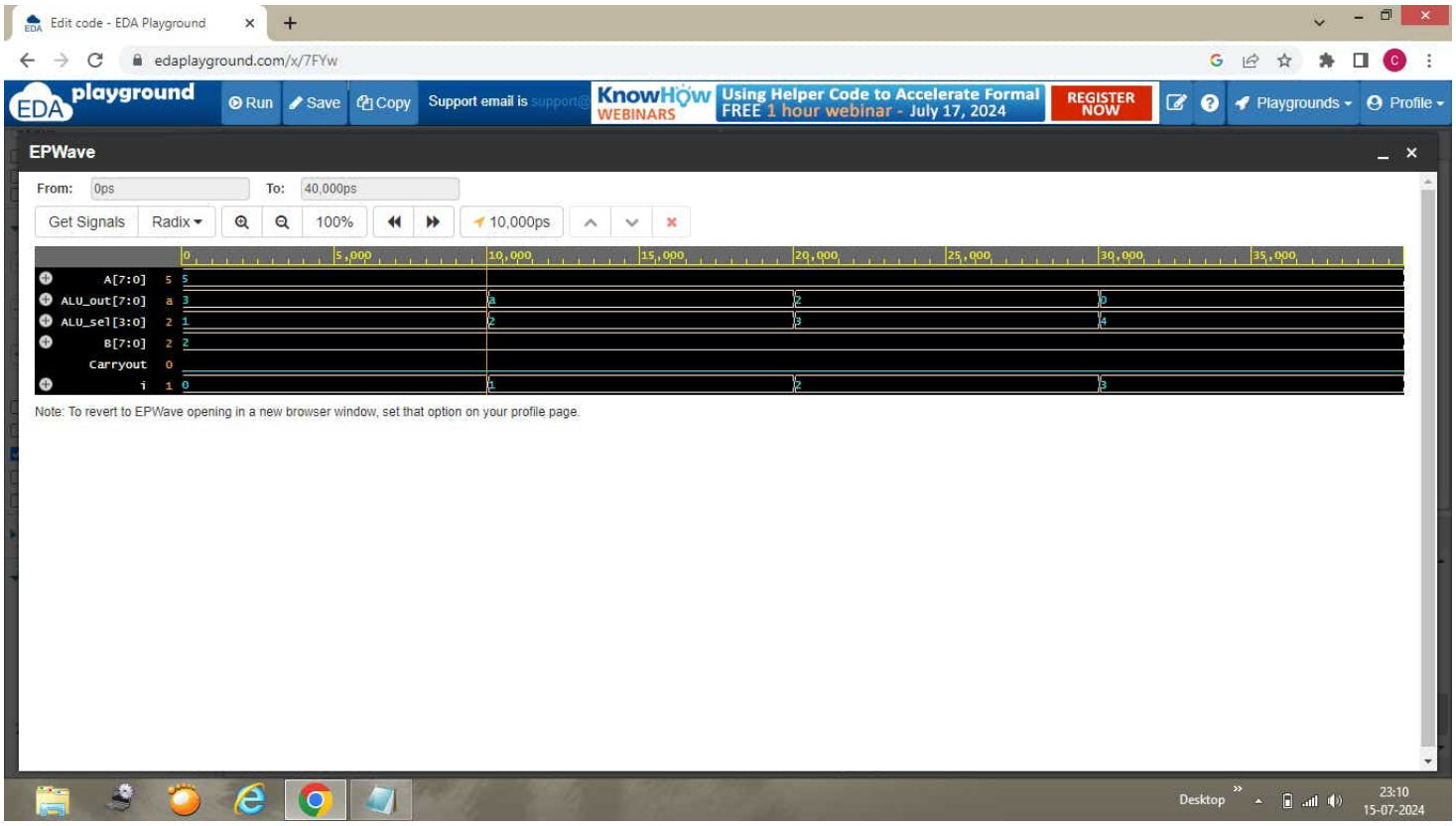
```
`timescale 1ns/1ps
module alu_tb;
reg[3:0] A,B;
reg[7:0]ALU_sel;
wire[7:0]ALU_out;
wire Carryout;
integer i;
alu test_unit(A,B,ALU_sel,ALU_out,Carryout
);
initial begin
$dumpfile("alu.vcd");
$dumpvars(1,alu_tb);
A=8'h05;
B=8'h02;
ALU_sel-4'h0;
for(i=0;i<4;i=i+1)
begin
ALU_sel-ALU_sel+8'h01;
#10;
end;
A=8 'hFF;
B=8'h00;
end
endmodule
```


Edit code - EDA Playground
edaplayground.com/x/7FYw
playground
Run
Save*
Copy*
Support email is support@edaplaygro
Testbench + Design
SystemVerilog/Verilog
UVM / OVM
None
Other Libraries
None
OVL
SVUnit
Enable TL-Verilog
Enable Easier UVM
Enable VUnit
Tools & Simulators
Aldec Riviera Pro 2023.04
Compile Options
-timescale 1ns/1ns
Run Options
+access+r
Run Time: 10 ms
Use run.do Tcl file
Use run.bash shell script
Open EPWave after run
Show output file after run
Download files after run
Examples
Community
Collaborate
Forum
Follow @edaplayground
204
testbench.sv
1 `timescale 1ns/1ps
2 module alu_tb;
3 reg[7:0] A,B;
4 reg[3:0] ALU_sel;
5 wire[7:0]ALU_out;
6 wire Carryout;
7 integer i;
8 alu test_unit(A,B,ALU_sel,ALU_out,Carryout);
9 initial begin
10 $dumpfile("alu.vcd");
11 $dumpvars(1,alu_tb);
12 A=8'h05;
13 B=8'h02;
14 ALU_sel=4'h0;
15 for(i=0;i<4;i=i+1)
16 begin
17 ALU_sel=ALU_sel+8'h01;
18 #10;
19 end;
20 A=8'hFF;
21 B=8'h00;
22 end
23 endmodule
Log
Share
KERNEL: Warning: Contact Aldec for available upgrade opti
KERNEL: SLP simulation initialization done - time: 0.0 [s
KERNEL: Kernel process initialization done.
Allocation: Simulator allocated 4671 kB (elbread=427 elab


Edit code - EDA Playground
edaplayground.com/x/7FYw
playground
Run
Save
Copy
Support email is
KnowHow WEBINARS
Using Helper Code to Accelerate Formal
FREE 1 hour webinar - July 17, 2024
REGISTER NOW
Playgrounds
Profile
EPWave
From: 0ps
To: 40,000ps
Get Signals
Radix
100%
10,000ps
A[7:0]
ALU_out[7:0]
ALU_sel[3:0]
B[7:0]
Carryout
i
Note: To revert to EPWave opening in a new browser window, set that option on your profile page.
Desktop
23:10
15-07-2024