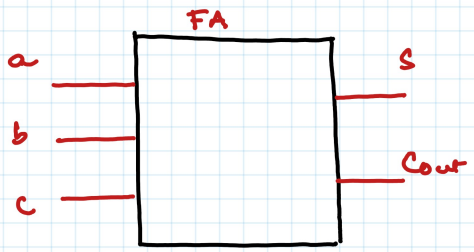
Write a Verilog program for Full adder




```
module FA (a, b, c, S, Cout);
    input a, b, c;
    output S, Cout;
  assign S = a ^ b ^ c;
  assign Cout = a&b | b&c | c&a;
endmodule
```

```
module FA_Test;
    reg a, b, c;
    wire S, Cout;
  FA mo (a, b, c, S, Cout);
  initial
    begin
        a=0; b=0; c=0;
    #10 a=0; b=0; c=1;
    #10 a=0; b=1; c=0;
    #10 a=0; b=1; c=1;
    end
  initial #30 $stop;
endmodule
```