DAY 51 – 100 DAYS VERIFICATION CHALLENGE

Topic: APB Protocol

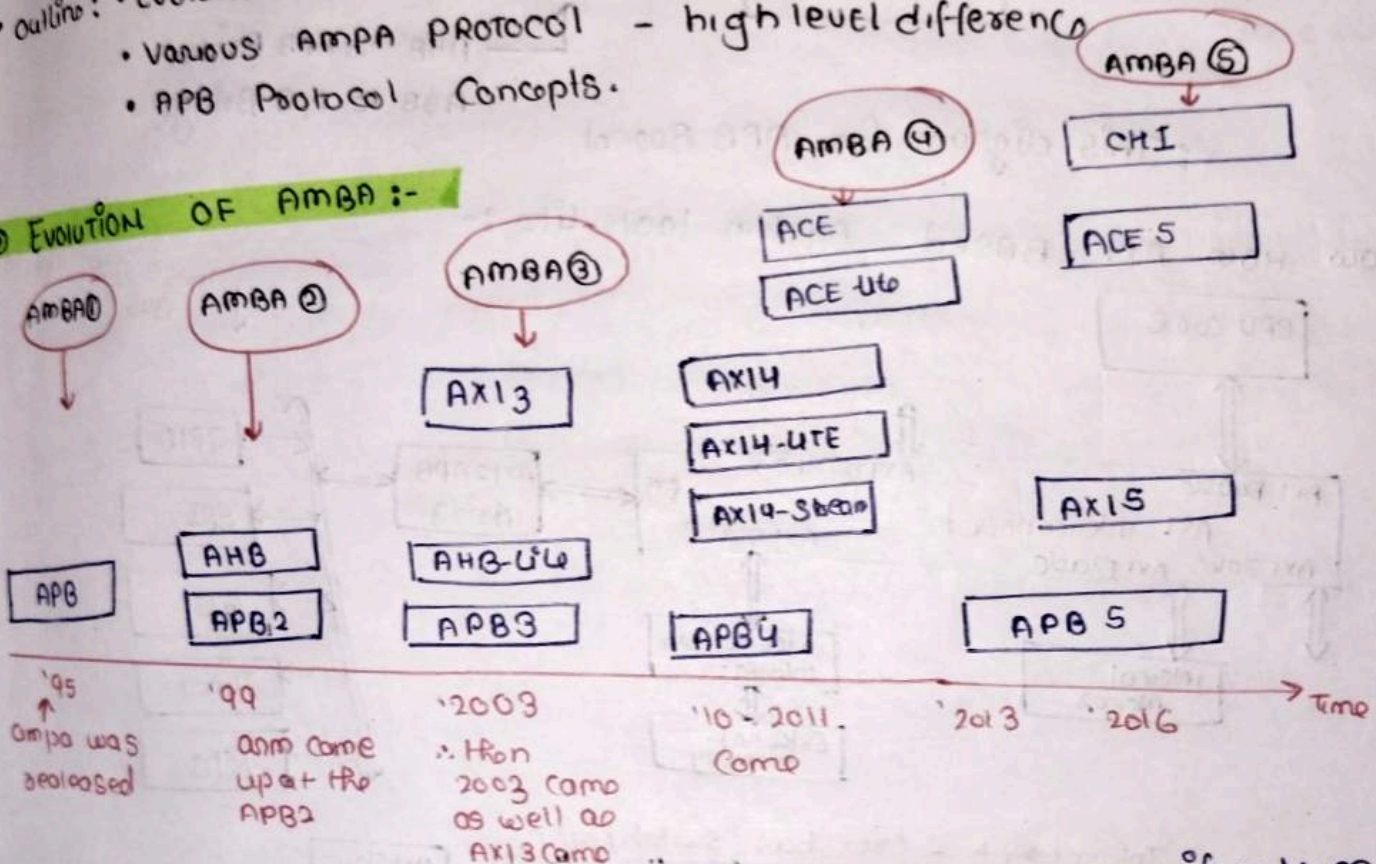
DAY 51 CHALLENGE:

1. Describe various input & output ports of APB protocol?
2. What are the phases of APB protocol?
3. How does APB work?
4. Why does APB not have any *wait* states?
5. How does APB handle accesses that are not 32 bits?
6. What are applications of APB?
7. What are operating frequencies of APB?
8. What is an APB bridge?
9. What are APB peripherals?
10. What is APB prescaler?
11. What is APB UART?
12. Which devices are connected to APB?
13. What is strobe in APB?

PART 1 :- AMBA PROTOCOL, EVOLUTION & APB 2/3/4 PROTOCOL CONCEPT OVERVIEW

- APB is the possible first AMBA PROTOCOL that was released by ARM.
- Outline :
  - EVOLUTION OF AMBA
  - VARIOUS AMPA PROTOCOL - high level difference
  - APB Protocol Concepts.

EVOLUTION OF AMBA :-

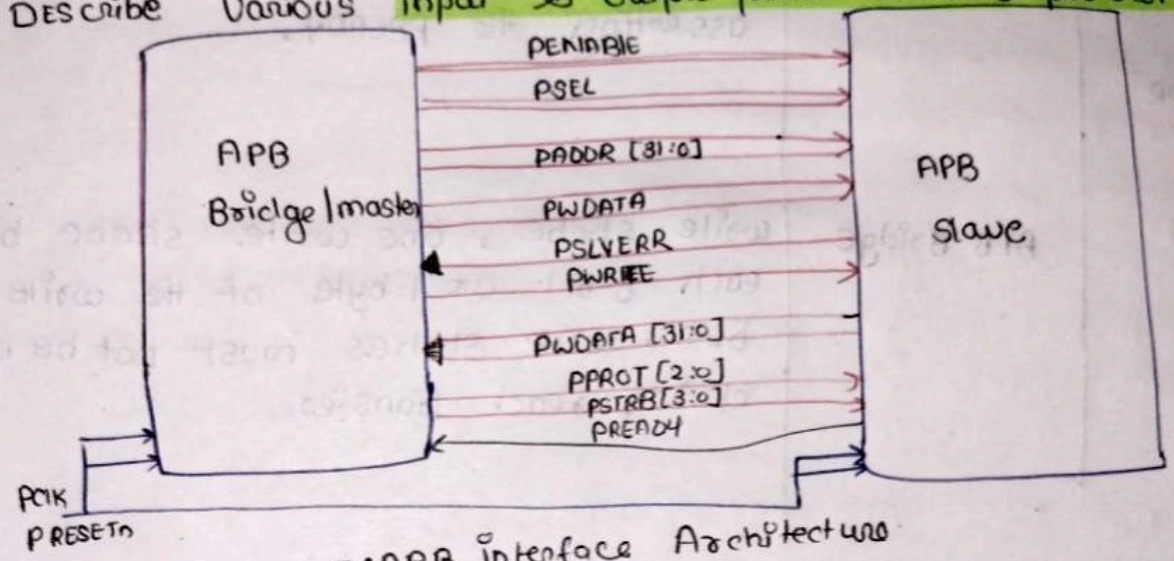


- So they add certain annoucement to the protocol specification like APB, APB2, APB3 etc) meeting certain design specification, requirement coz when time changes design requirements is changes.
- Initialy in SoC designs, AHB (Advance High performance Bus) used for High Bandwidth interconnect &
- APB (Advanced Peripheral Bus) for low Bandwidth peripheral interconnect.
- APB look like a single master to multiple slave.
- With increasing number of functional Blocks (IP) integrating into soc design, the shared Bus protocol started hitting limitation & then in 2003 AMBA3 introduced a new point to point connectivity protocol - AXI [advanced Extensible interface).
- Later in 2010, enhanced version AXI4 was introduced.

DAY : (61)

Topic : APB PROTOCOL

Soln ① Describe Various input & output ports of APB protocol?



-: APB interface Architecture

: APB Interface Signals :-

Signals	Source	Description
1. PCLK	Clock Source	• Generally System clock is directly connected to this.
2. PRESETn	System bus equivalent	• Reset, The APB reset signal is Active low Asynchronous Reset.
3. PADDR	APB BRidge	• Address bus from master to slave, can be up 32 to bit wide.
4. PWDATA	APB Bridge	• write data bus from master to slave, 32 bit wide.
5. PRDATA	APB Bridge	• Read data us from Slave to master, 32 bit wide
6. PSELX	APB Bridge	• Slave Select Signal, there will be one PSEL Signal for each slave Connected to master. If master Connected to 'n' number of slaves, PSELn is the maximum number of signals present in sys. eg: (PSEL1, PSEL2, PSEL3 --- PSELn).
7. PENABLE	APB Bridge	• APB ENABLE Signal, - indicates the 2nd & subsequent cycles to transfer. when PENABLE is asserted, the Access phase in the transfer starts.
8. PWRITE	APB Bridge	• Direction, when 1, write access else read access. means indicates write when High, READ when LOW.
9. PREADY	Slave interface	• Ready Signal, slave used this Signal to extend an APB transaction

		• Its used by the slave to in... in the transfer. ie. whenever slave is not ready to complete the transaction, it will request the master from some time by de... asserting the PREADY.
PSLVERR		
PSTRB	APB Bridge	write strobe, one write strobe bit for each 8-bit or 1 byte of the write data bus. write strobes must not be active during read transfer.

(2) what are the phase OF APB Protocal ?

∴ in APB, There are two phase,

① Setup phase
② Access phase

• The Access phase is indicated by assertion OF PENABLE signal.

1.) IDLE phase:

• ideal is a default state for the APB interface. if there is no transfer happening then it will remain in that ideal state.

2.) Setupphase:

• when a transfer is required the bus moves into SETUP state, where the appropriate select signal s PSELx is asserted.

• Bus only remains in the setup state for one clk cycle & always moves to Access state on the next rising edge of the clk.

• Address, write, select & write data signals must remain stable during the transition from SETUP to Access state.

3.) Access phase: • The enable signal, PENABLE is asserted in ACCESS state.

• Now exit from the ACCESS state is controlled by th... from the slave.

Soln ④ why does APB not have any wait states?

- its totally depends on the APB slave functionality or implem
  If there is no reason that prevent the data from being writte
  in to the designated area.
- PREADY - its used by the slave to include wait state in the
  transfer. i.e whenever slave is not ready to complete the
  transaction, it will request the master for some time by de-ass
  the PREADY. that's why the APB slave dosn't have to inser
  wait states.

Soln ⑤ How does APB HANDLE access that are 32 bits?

- The bridge should simply pass the entire 32-bit data
  bus through the Bridge.
- please note that, when transfer less than 32 bits are
  performed to an APB slave it is important to ensure
  that the peripheral is located on the appropriate bits
  of the APB data bus.

Soln ⑥ What are application of APB?

- APB is widely used in embedded system for connecting
  peripherals such as GPIO, timers, UART & other low speed device.
- Accessing the programmable control registers of peripheral
  device.
- Connected to low-Bandwidth peripherals.
- The APB, on the other hand, focuses on efficent &
  low Bandwidth connectivity Btw peripherals & slower
  device such as timers.
- it can be utilized for communication interfaces like I_2C
  & SPI that operate at relatively lower speeds
  compared to high speed buses.

Soln ① what are Operating frequencies of APB?

- APB Supports 32 bit and 66MHz signal frequency but it is not mandatory depends on requirements designer can vary the frequency.

Soln ⑧ what is an APB bridge?

- The AHB to APB bridge is an AHB slave, providing an interface btw the high speed AHB & the low-power APB.
- Read & write transfer on the AHB are Converted into equivalent transfer on the APB.
- As an APB not pipeline then wait states are added during transfer to & from the APB when the AHB is required to wait for the APB. Its required to Bridge the Communication gap btw low Bandwidth peripherals on APB with the high Bandwidth ARM Processor or other high-speed device on AHB.

Soln ⑨ what are APB peripherals?

- On-chip Storage
- Storage drivers
- Soc processors
- DMA sensors.

Soln ⑩ what is APB Prescaler?

- APB Timer module is 16-bit down Counter with a selectable prescaler. prescale values of 1, 32 & 256 can be selected.
- The prescaler extends the timer's range at the expense of precision. The timer provides two modes of operation that provide a free running value & also periodic interrupts
- The APB prescaler typically Consists of a clk divider, a delay element & Control logic

Soln (11) what is APB UART ?

- APB UART is a simple Universal Asynchronous Receiver/Transmitter that support 8-bit Asynchronous serial Communication without parity & fixed at one stop bit. The baud rate is fixed at 19200.
- UART also use two Fifo as buffer for both send & recive data. If the recive data (FIFO) is empty & a read request is sent the UART will drive PREADY Low & wait for data befor continuing.
- If the transfer FIFO becomes full the UART will also drive READY low & wait for the FIFO to become not full before continuing.

Soln (12) what devices are connected to APB ?

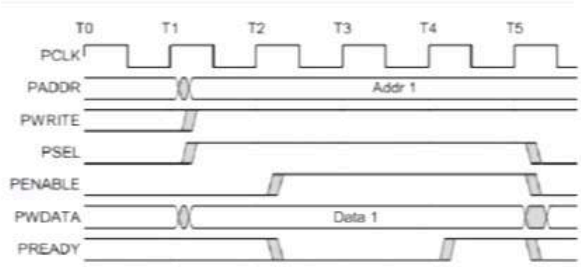
- APB is low Bandwidth & low performance bus. So the component requiring lower Bandwidth like the peripheal device as UART, keypad. Timer & PIO devices are connected to APB.
- The Bridge acted as the high performance AHB & ASB bus to the APB bus, so for APB the Bridge acts as the master & all the devices Connected On the APB bus act as slave.

Soln (13) what is Strobe in APB ?

- A specific timing signal, called a "Strobe", is used to indicate a valid timing window for data or Control signal
- each strobe is often a single clock cycle-wide pulse that marks the specific time when a signal is valid.
- OR in APB the Strobe signal indicates whether the transfer in transaction is valid or not by using PSTRB signal.
- 1 PSTRB signal is 1 then the transfer is valid else its invalid transfer.

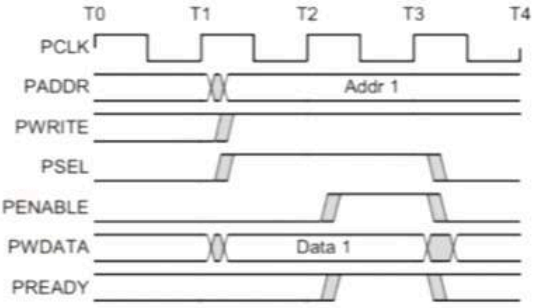
Ques:3 How does APB work?

WRITE Transfer – With Wait State



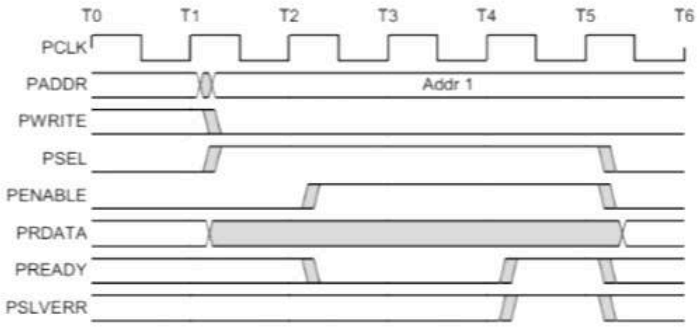
i. During the ACCESS Phase, when PENABLE is high, the slave extends the transfer by driving PREADY low.
ii. The PADDR, PWRITE, PSEL, PENABLE, PWDATA, PSTRB, PPROT signals should remain unchanged while PREADY is low
iii. PREADY can take any value when PENABLE is low.

WRITE Transfer – Without Wait States



i. At T1, a write transfer with address PADDR,PWDATA,PWRITE and PSEL starts.
ii. They will registered at the next rising edge of PCLK, T2.
iii. This is Setup Phase of Transfer.
iv. After T2, PENABLE and PREADY are registered at the rising edge of PCLK.
v. When asserted, PENABLE indicates starting of ACCESS Phase
vi. When asserted, PREADY indicates that slave can complete the transfer at the next rising edige of PCLK.
vii. PADDR, PDATA and control signals all should remain valid till the transfer completes at T3.
viii. PENABLE signal will be de-asserted at the end of transfer.

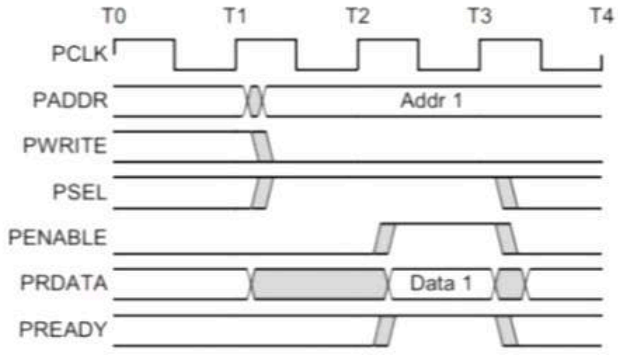
ERROR Response



Whenever there is a problem in the transfer, Slave indicates the error response for the transfer by asserting the PSLVERR signal. PSLVERR is only considered valid during the last cycle f and APB transfer, when PSEL, PENABLE and PREADY are all HIGH. It is recommended, but not mandatory that you drive PSLVERR low when it is not being sampled.

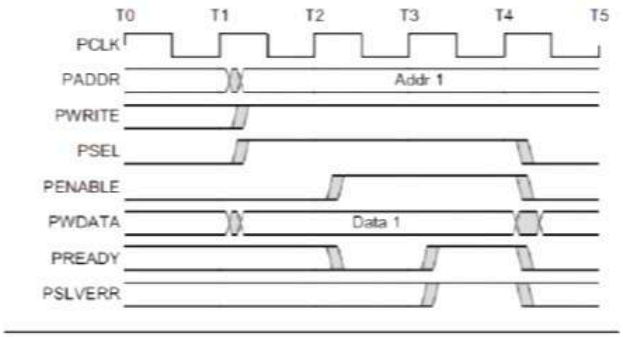
Transactions that receive an error response, might or might not have changed the state of peripheral. For example, If APB master performs a write transaction to an APB slave and received an error response, it is not guaranteed that the data is not written on the slave peripheral.

READ Transfer – Without Wait States



i. At T1, a READ transfer with address PADDR, PWRITE and PSEL starts.
ii. They will be registered at rising edge of PCLK.
iii. This is SETUP Phase of the transfer.
iv. After T2, PENABLE and PREADY are registered at the rising edge of PCLK.
v. When asserted, PENABLE indicates the starting of ACCESS phase.
vi. When asserted, PREADY indicates that slave can complete the transfer at next rising edge of PCLK by providing the data on PRDATA.
vii. Slave must provide the data before the end of read transfer. i.e. before T3.

READ Transfer – With Wait States



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