VLSI DESIGN TEST/POWER

PROJECT 3

LOW POWER ANALYSIS

Team members:

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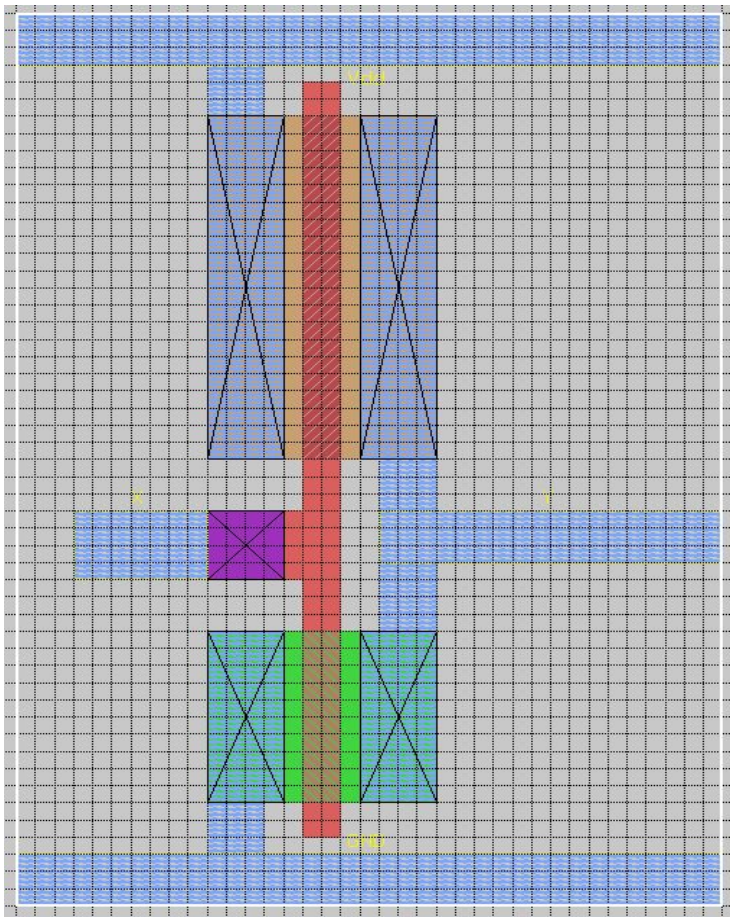
Question1:

To design an inverter using the CMOS with the given technology file with(channel length=2 lambda and for NMOS and PMOS, channel width= 10 lambda for NMOS and 20 lambda for PMOS) which drives a load with 10fF



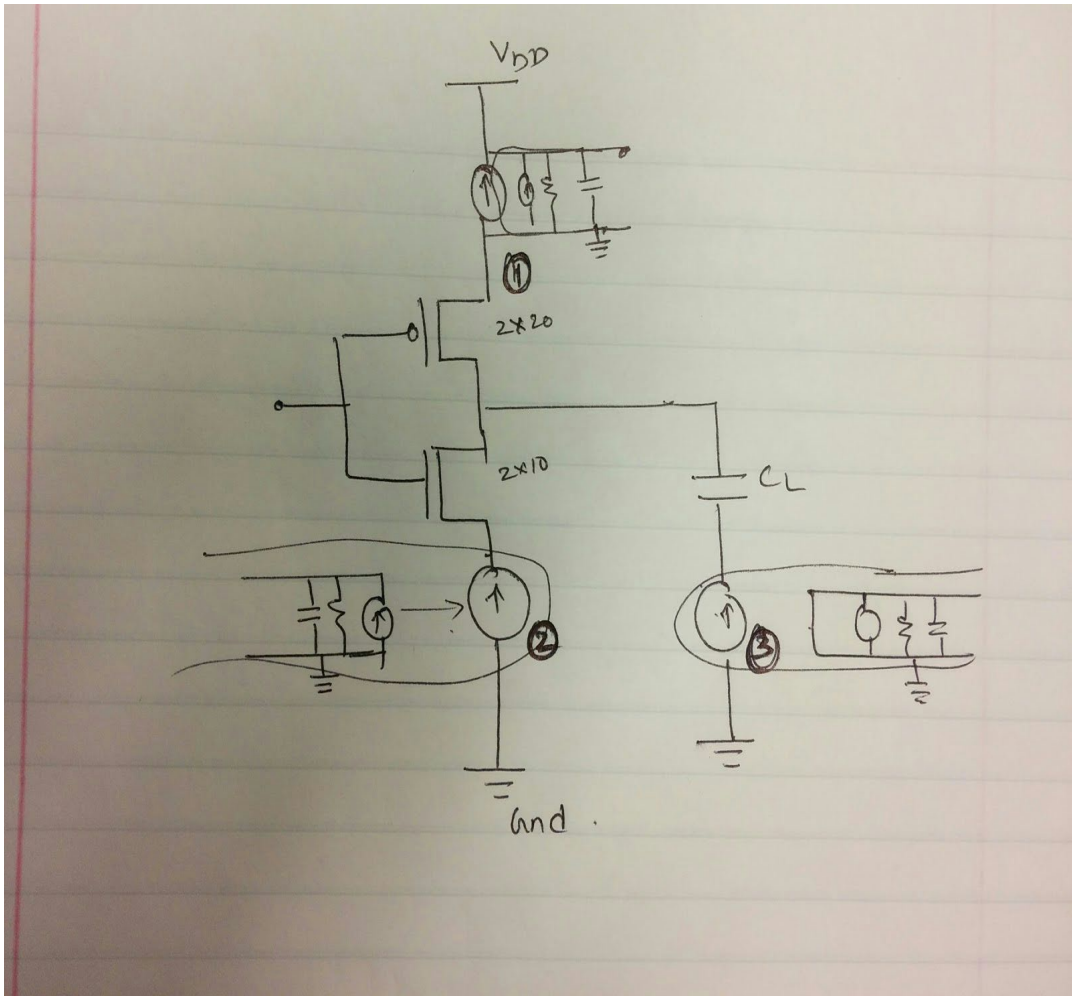
The layout is designed and the spice files are extracted for the layout.

SPICE FILE EXTRACTED:

```
.option scale=0.3u

m1000 Y X K Vdd pfet w=20 l=2
+ ad=100 pd=50 as=100 ps=50
m1001 Y X K1 K1 nfet w=10 l=2
+ ad=50 pd=50 as=50 ps=50
C0 GND GND 2.7fF
C1 Y GND 3.2fF
C2 Vdd GND 3.2fF
```

Circuit connections :



Spice File for simulation:

* HSPICE file created from invertor.ext - technology: scmos

.option scale=0.3u

m1000 Y X K Vdd pfet w=20 l=2
+ ad=100 pd=50 as=100 ps=50
m1001 Y X K1 K1 nfet w=10 l=2
+ ad=50 pd=50 as=50 ps=50
C0 GND GND 2.7fF
C1 Y GND 3.2fF
C2 Vdd GND 3.2fF

*C3 X GND 7.9fF

```
******************
C4 Y K2 10fF
VDD Vdd GND 5V
vgnd GND Gnd 0
******************
Vtstp Vdd K 0
Fp Gnd A Vtstp  0.025
Rp A Gnd 100k
Cp A Gnd 100pF
******************
Vtstp1 K1 Gnd 0
Fp1 Gnd A1 Vtstp1  0.025
Rp1 A1 Gnd 100k
Cp1 A1 Gnd 100pF
******************
Vtstp2 K2 Gnd 0
Fp2 Gnd A2 Vtstp2  0.025
Rp2 A2 Gnd 100k
Cp2 A2 Gnd 100pF
******************
.ic v(C0)=0
.ic v(C1)=0
.ic v(C2)=0
.ic v(C3)=0

.include /home/alamalhh/model_t36s.sp

*Va A Gnd PULSE(0 5 0n 1n 1n 400n 800n)
*Vb B Gnd PULSE(0 5 0n 1n 1n 200n 400n)
*Vc C Gnd PULSE(0 5 0n 1n 1n 100n 200n)
*Vd D Gnd PULSE(0 5 0n 1n 1n 50n 100n)

Vx X Gnd PWL (0n 5V 0.3n 5V 2n 5v 2.3n 0V 6n 0V 6.3n 5V 8n 5V 8.3n 0V 10n 0V 10.3n 5V
14n 5V 14.3n 0V 16n 0V 16.3ns 5V 18n 5V 18.3n 0V 20n 0V)

.options post
.tran 0.1n 25n
.print tran V(K3) V(X)
.print tran i(Vtstp)
.print tran V(A)
.print tran V(A1)
.print tran V(A2)
.end
```

****end line****

** hspice subcircuit dictionary

Note:

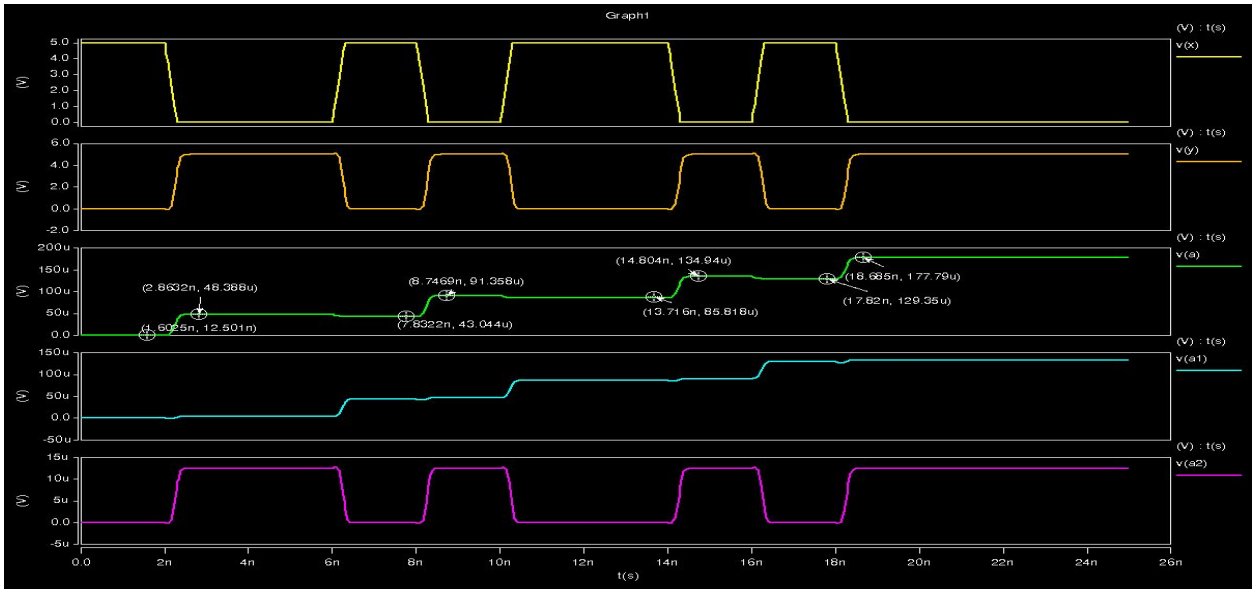
1.For all the questions the power units is taken as milli watt.The units are not repeatedly mentioned and just mentioned as units.

2. For the ease of calculations th intial value of the circuit is taken as 1 instead of 0.As if the initial value is 0 then the output will be 1 and the power is already present in the load capacitor by default, which needs to be subtracted for all the calculations.Instead if the input is with 1 and hen transitions to 0.the calculations and the prrof are much more clear.

Question2:

For the schematic of the inverter shown above the dummy circuits are added as shown in the above figure to measure the different sources of power the average,dynamic ,short circuit and the leakage power.

The below is the measure of the average power for the inverter measured by using the dummy circuit inserted at the place 1.



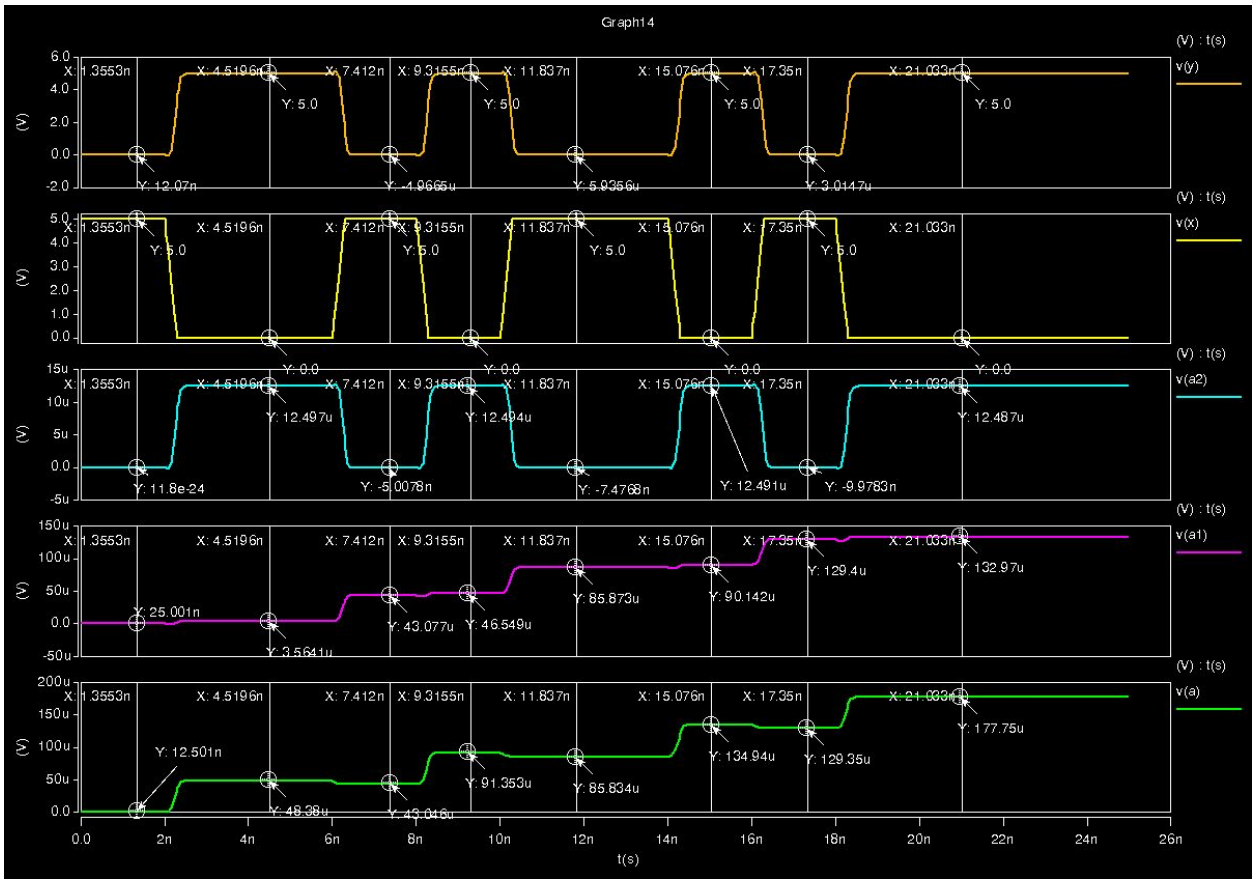
The average power consumed by the circuit is 48 units, which is measured by the V(a), from the dummy circuit at the position1. The 48,48,49,48 for the four peaks observed and the average is 48.25 units.

Question3:

The average dynamic ,leakage and the short circuit powers are measured by using the different dummy circuits connected as shown earlier.

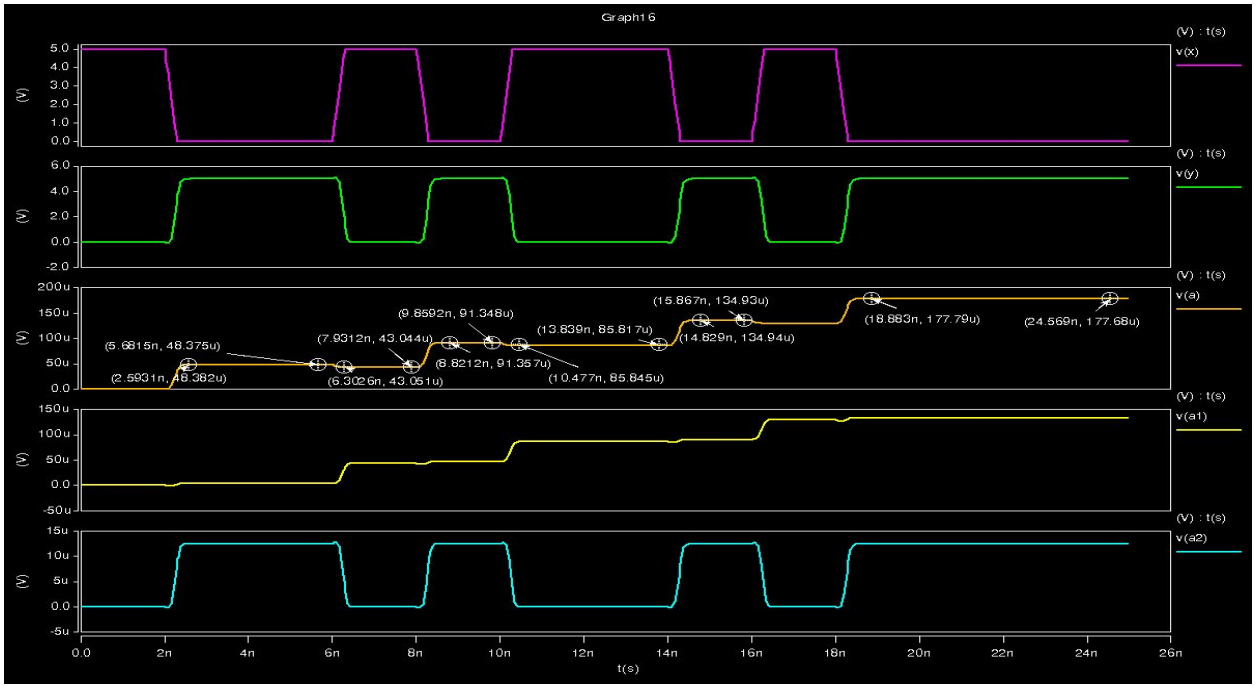
Dynamic Power calculation:

The dynamic power is the power consumed by the load capacitance connected at the the output of the inverter.



The dynamic power is the power consumed when the output of the inverter changes from 0 to 1, which charges the load capacitor.The power consumed for a single rise transition of 0 to 1 at output is 12.49 units. Here for the four different instances the power consumed is 12.48,12.49,12.48 and 12.49 units.This is seen at the node V(a2).

Leakage Power:

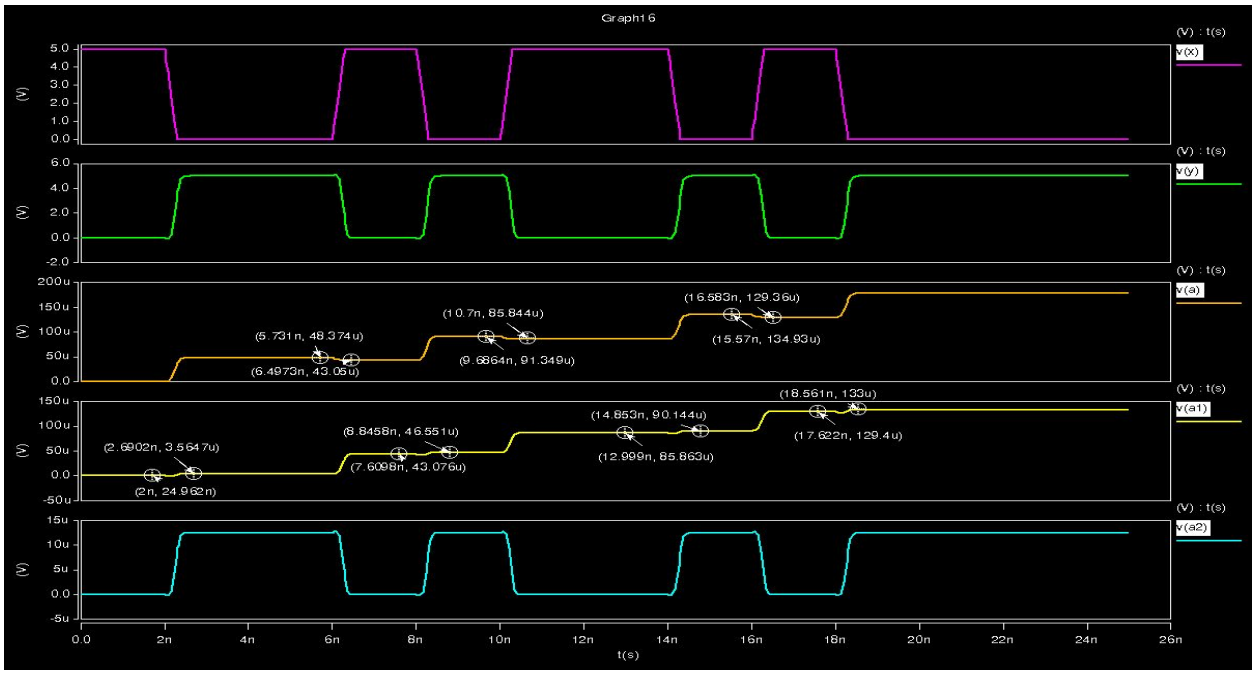


The leakage power consumed can be measured with the dummy circuit 1 when the outputs are stabilized to a stable value.

Leakage power when output is at 1:0.007 ,0.007,0.007,0.007 units.Average is 0.007
Leakage power when output is at 0:0.006 ,0.006,0.006 units.Average is 0.006

Short circuit power:

The short circuit power is drawn from the source when both the p and n transistors are switched ON at the same time.



The short circuit power drawn can be measured for the rise of the output measuring the power drawn at the dummy circuit 2.And the short circuit power drawn for the fall of the output by measuring the power in the dummy circuit 1.

Average short circuit power for rise of o/p is (3.5 +3.5 +4.2 +3.5)/4=14.7/4=3.675 units
Average short circuit power for rise of o/p is (5.3 +5.5+5.6)/3=16.4/3=5.466 units

Total Power analysis:

The total power drawn from the source should be equal to the sum of the dynamic ,short circuit,leakage powers and the power dissipated as heat.

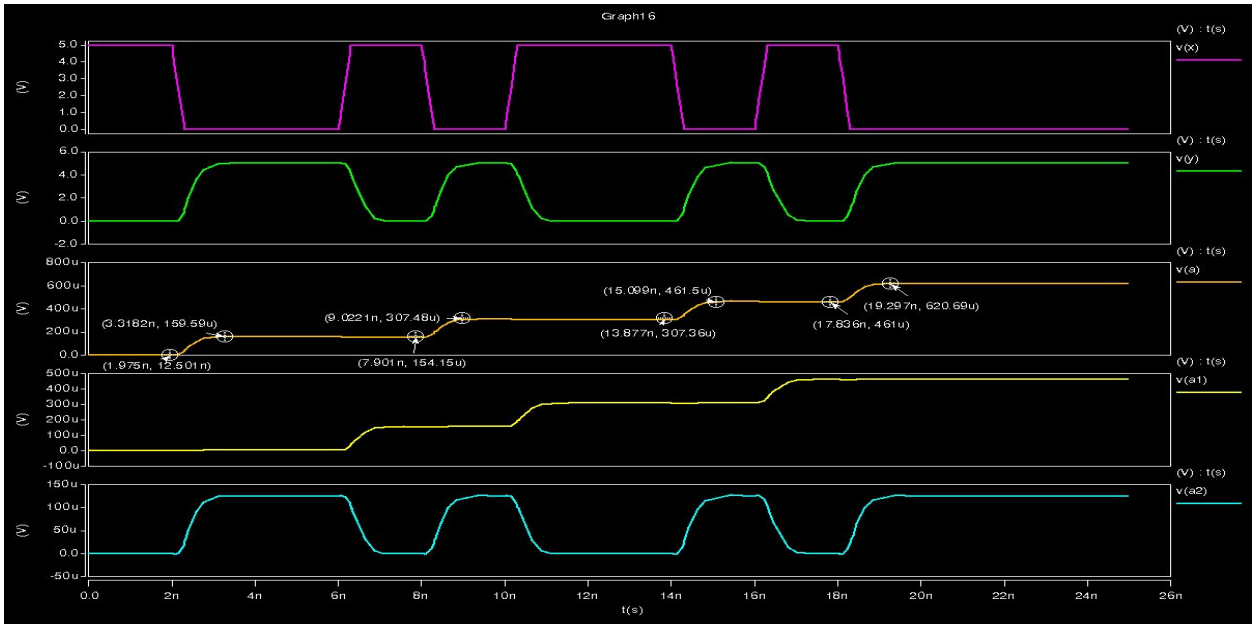
Total power consumed is 192 units
Total Dynamic power consumed is 12.5 x4 rise times= 60 units,
Total Short circuit power consumed = 31.1 units (both rise and falls)
Total leakage is ~ 1 unit

So the total power consumed is 60(dynamic) +60(heat) +31 (short circuit) +1(leakage) =152 units.
The remaining power of 40 units must be consumed by the parasitic capacitances.

So the total power consumed from the source is in the circuit and no power is lost during the circuit operation.

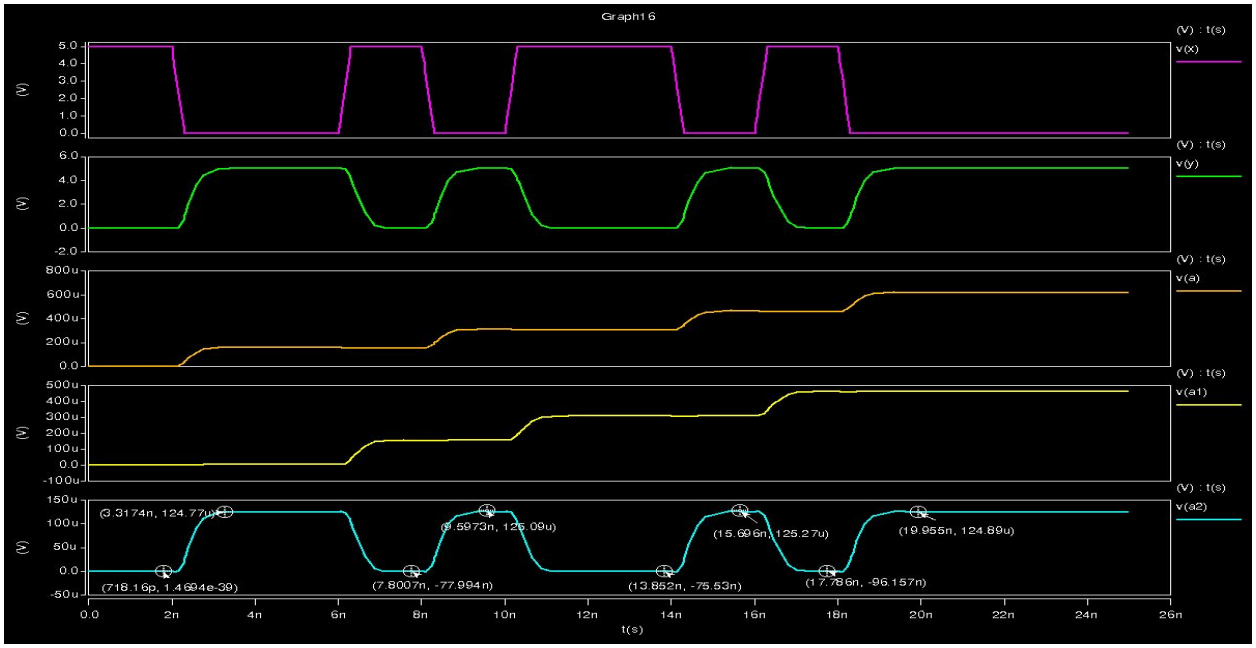
Question 4:

The average power consumed with 100fF is



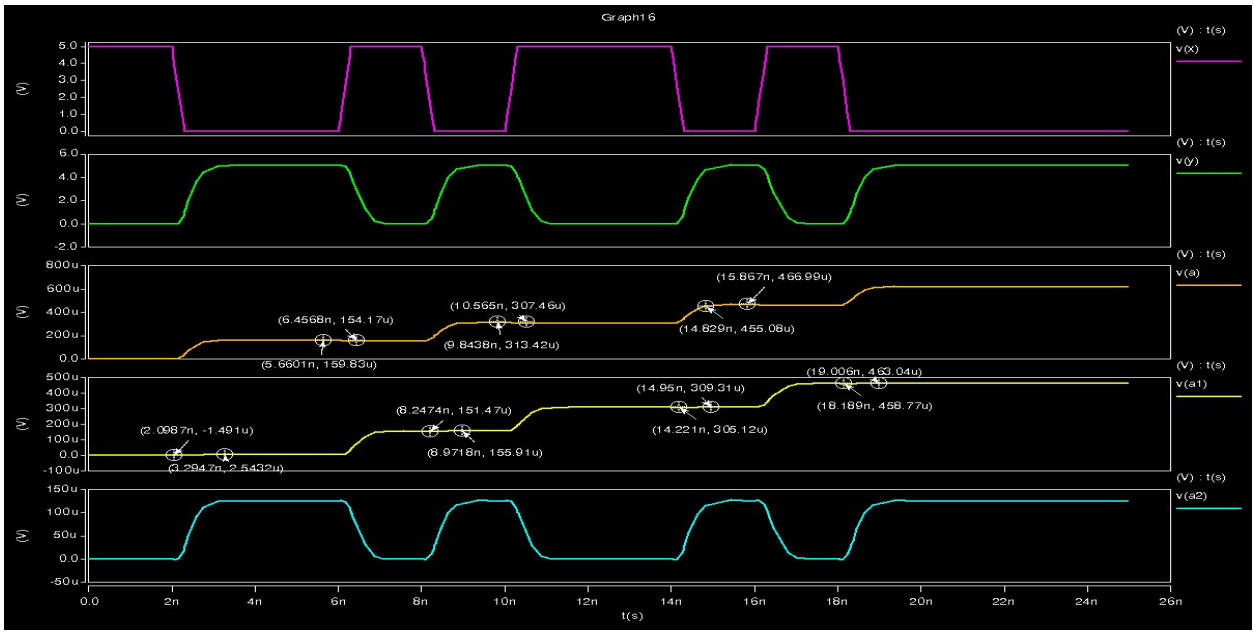
It is 159 units approximately.It is increased with load capacitance increase

The dynamic power with the 100fF load is



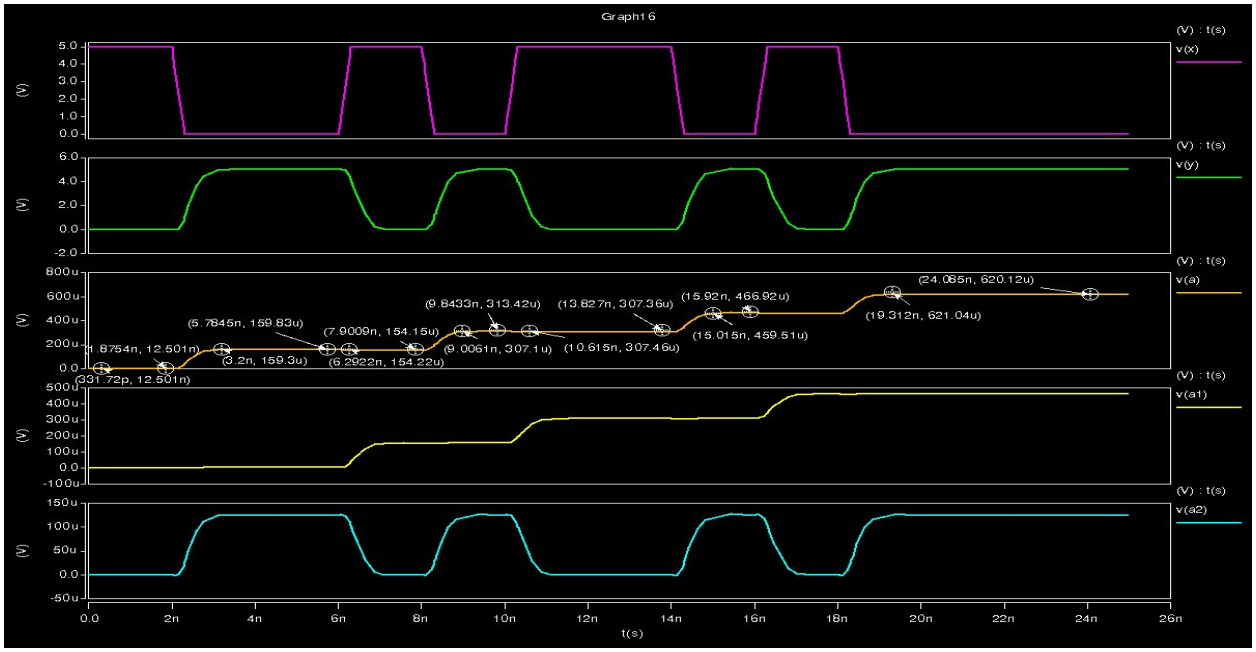
The dynamic power consumed in the circuit is around 124.7 units on average.
The 4 instances of the dynamic power is 124.77,125,125.27 and 124.1 units

The short circuit power is



Average short circuit power for rise of o/p is (3.9 +4.5 +4.0 +4.5)/4=16.9/4=4.225 units
Average short circuit power for fall of o/p is (4.5 +5.0+4.2)/3=13.7/3=4.566 units

The leakage power consumed with 100fF is



The leakage power consumed can be measured with the dummy circuit 1 when the outputs are stabilized to a stable value.

Leakage power when output is at 1:0.007 ,0.007,0.007,0.007 units.Average is 0.007
Leakage power when output is at 0:0.006 ,0.006,0.006 units.Average is 0.006

Conclusions and observations:

The total average power consumed in the circuit is increased with the load capacitance.With 10fF its 38 units and with the 100fF its 160 units.

The dynamic power consumption is increased with the increase in the load capacitance.With 10fF load it was 12.5 units and when the load capacitance is increased by 10 times which is if the load is 100fF , the dynamic power consumed is also increased by 10 times which is 125 units.

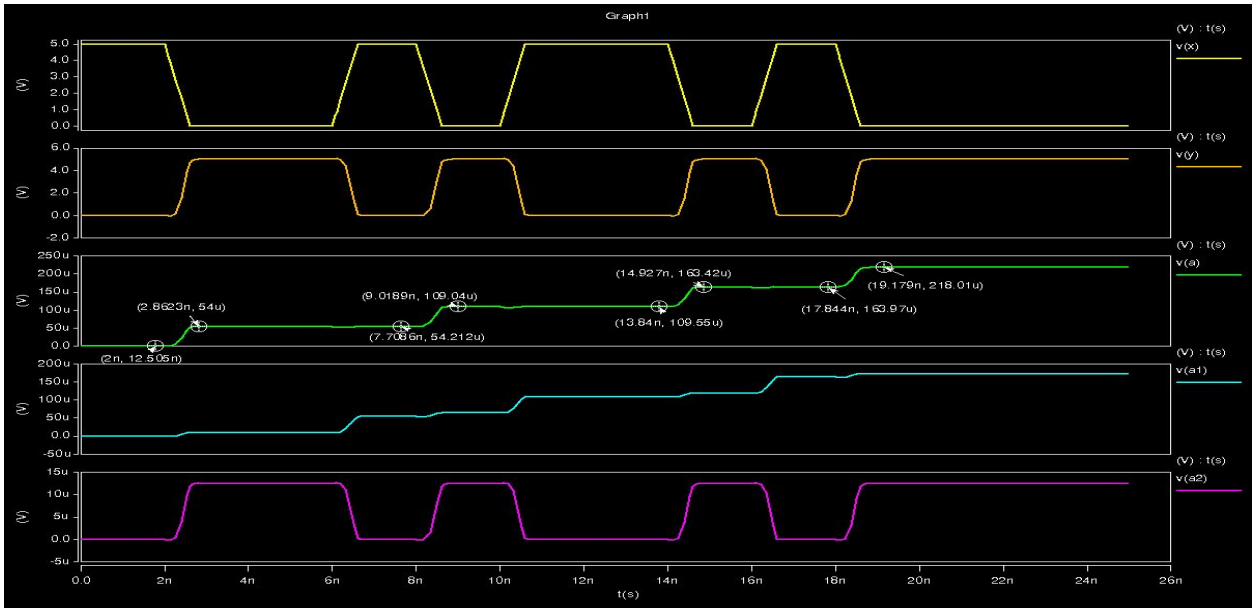
The total average short circuit power is 4.39 with the load of 100fF where in its 4.6 units with the load of 10fF.So it shows that as the load is increased the short circuit power is reduced.**This is because when the load is increased the output fall time is large than the input rise time.Vds of the pmos is essentially 0 during this period.So very Isc(short circuit current).**

When the Cl is small, output fall time is much smaller than the input rise time, So Vds of the pmos is close to VDD making more Isc(short circuit current) through the circuit.

The leakage current observed is same in both the 10fF and the 100fF cases.So the load capacitance has no much role on the leakage power consumed of the circuit.

Question5:

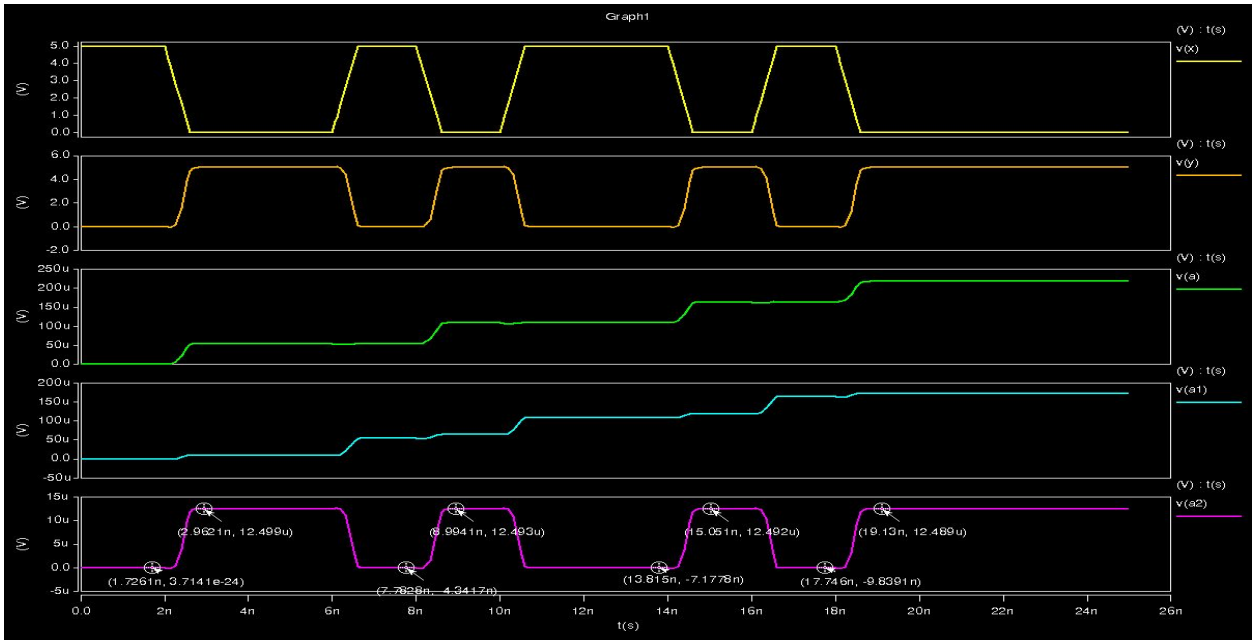
Average power consumption:



Observation and conclusion:

The average power increases because the short circuit power is increased

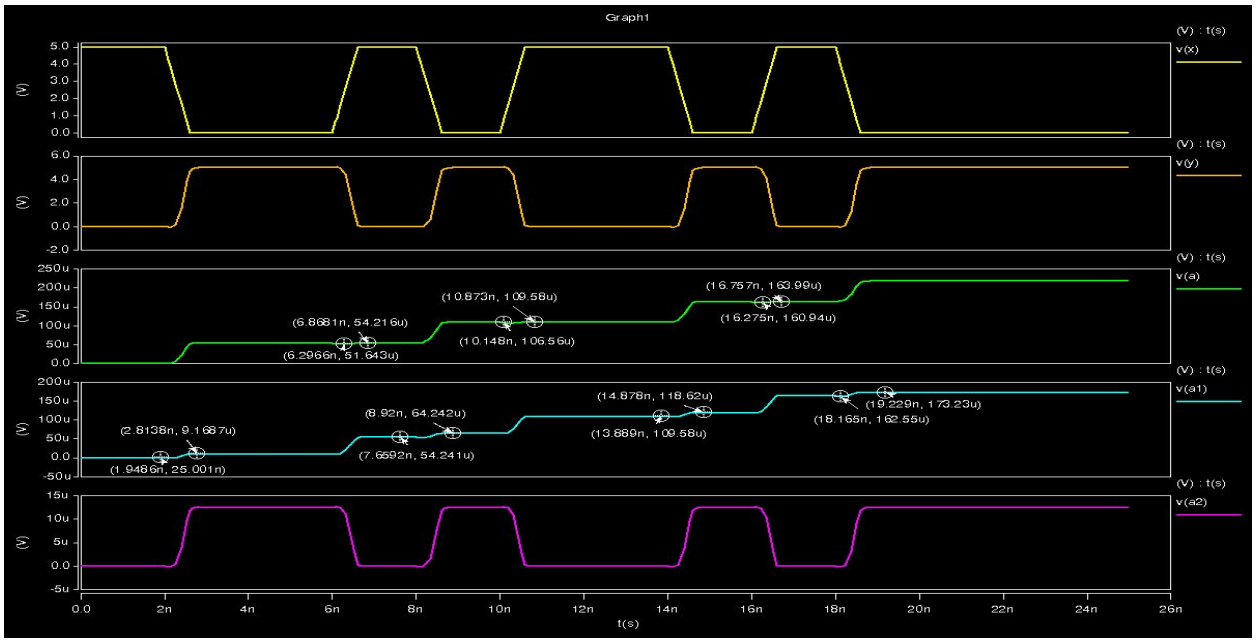
Dynamic power consumption:



Conclusions and observations:

The dynamic power consumed is the same with the rise and fall times of 0.3ns and 0.6 ns.So its same 12.49units in both the cases.

Short circuit power consumption:

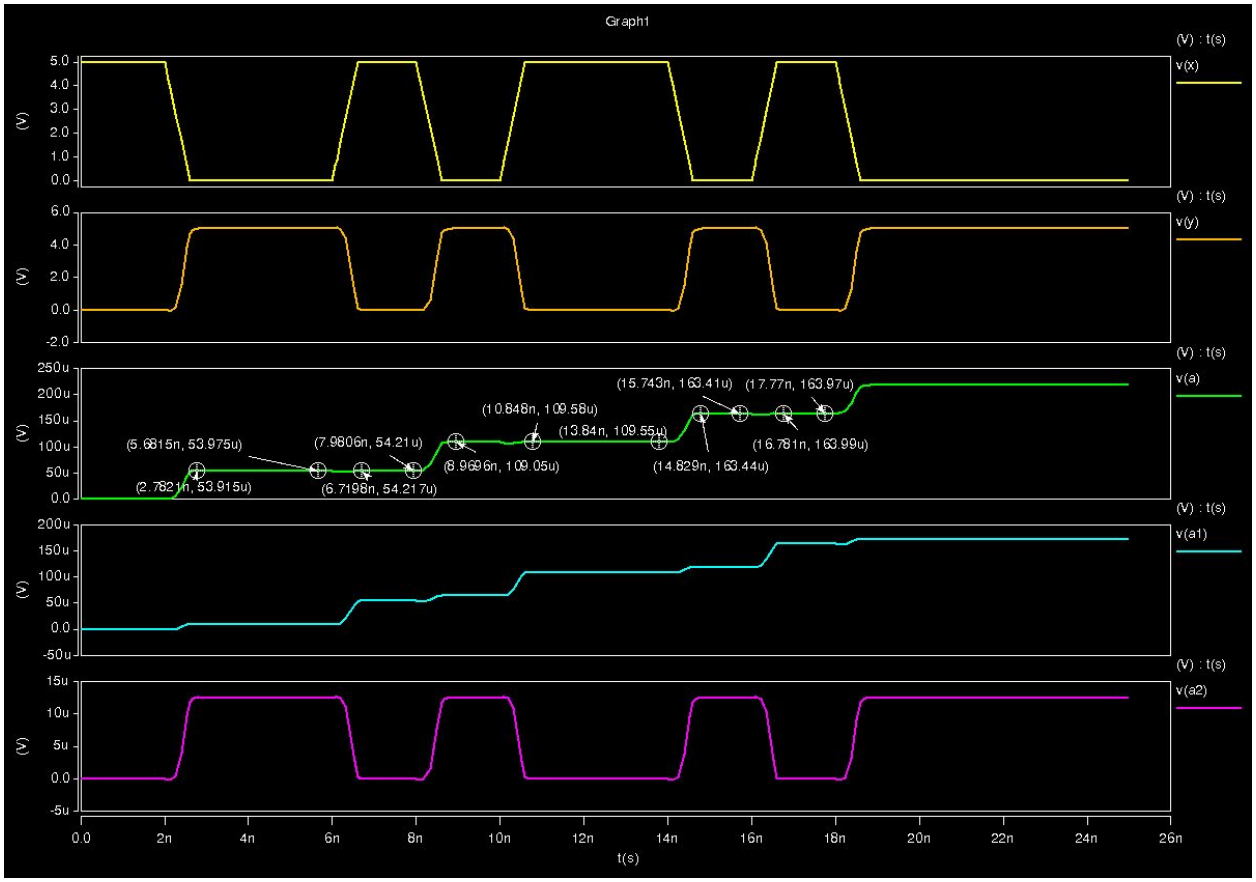


Average short circuit power for rise of o/p is (9.1 +10.01 +9.1 +11.1)/4=39.2/4=9.8 units
Average short circuit power for fall of o/p is (3.5 +3.0+3.9)/3=13.7/3=3.466 units

The total average short circuit power consumed is 6.66 units

Conclusions and observations:
The short circuit power consumed increases when the rise and fall times are increased.With 10fF its 3.49 units and with the 100fF load its 6.66 units.

Leakage power consumption:



The leakage power consumed can be measured with the dummy circuit 1 when the outputs are stabilized to a stable value.

Leakage power when output is at 1:0.007 ,0.007,0.007,0.007 units.Average is 0.007
Leakage power when output is at 0:0.006 ,0.006,0.006 units.Average is 0.006

Conclusions and observations:

The leakage power consumed is remained same irrespective of the increase in the rise and fall times of the input