	EC0319	: Digital	Electronics
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Date:

PRACTICAL-3

AIM: To Verify Half adder & Full adder Truth Table and Logic Diagram

- · To verify the half adder and full adder touth table and logic diagrams:
- is. Boolean Expression:
 - a). Half adder:
 - · Sum (5): 5 = A & B (xoR operation) · (arry (c): C = A.B (AND operation)
 - b. Full adder:
 - · 5um (s): 5 = A & B & Cin
 - · (arry ((-out): (out = (A.B) + ((in . (A &B))
- ii). Touth Table:
 - a). Half adder:-

A	В	Sum(5)	(crosy (c)
0	0	O	01
0	1	1	0
1	0	1	0
1		0	1

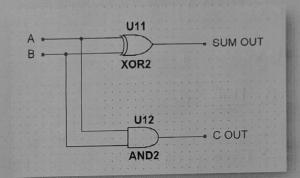
b). Full adder:

TA	B	Cin	5um (5)	(arry (Lout)
-			4-1	i
_ 0	0	0	0	0
0	0	1		0
0	1	0		0
0	1	1	0	i
1	0.	0		0

	0	1	0	1
1	1	0	0	1
1	1	1	1	1

iii). Logic (izcuit Diagram:

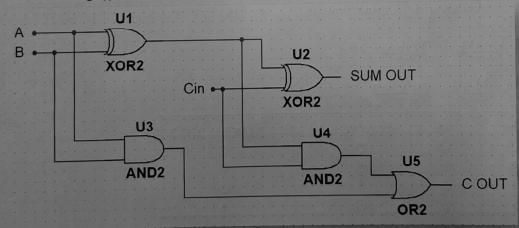
- as. Haif adder:
- · Sum (s): Use an XOR gate for A & B.
 · (arry (c): Use an AND gate for A.B.



b). Full adder:

· Sum (5) : 5 = A & B & Cin

· (avoy ((-out): (out = (A.B) + ((in. (A + B))



(onclusion :-

In this experiment, we successfully verified the operations of both the Half adder and full adder circuits using their respective touth tubles and logic diagrams.