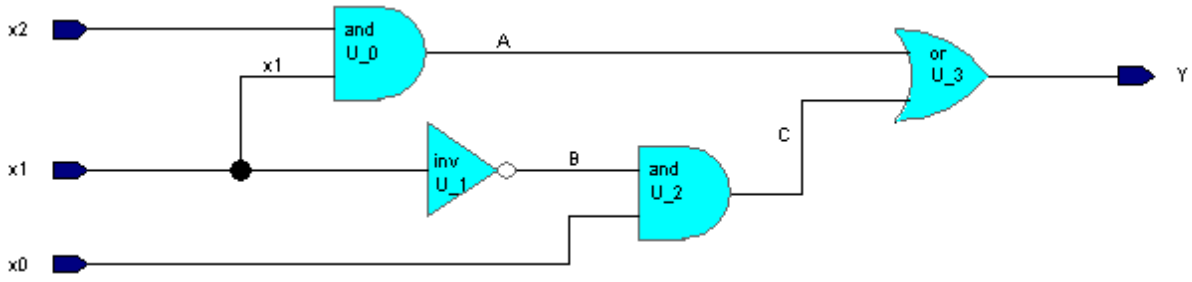
COMP.CE.200 Digital Design

Fall 2021

Paper Exercise 3

Problem 1



Examine the circuit shown above and answer the following questions.

a) Determine the output y equation from the diagram. Use the helper variables A, B, and C.
b) What is the critical path assuming each gate has the same unit delay regardless of load and gate type?
c) Draw the circuit timing when the input sequence is ("111", "111", "111", "101", "101", "101"). The values are given separated by one unit delay. X = "111" is the first input. You can use TimingDraw program and the given wave form or draw by hand using the given template picture.
d) How would you fix the problems in the circuit?