COMP.CE.200 Digital Design

Fall 2021

Paper Exercise 3 bonus

Problem 1

Design a circuit that performs the logical function $f_i = (x + y)zw_i, i \in [0,127]$, where x, y z, and w_i are binary inputs and f_i binary outputs (yes, the system really has 128 separate w inputs and outputs). Use the technology specified in the table below. The delay of the critical path must not exceed 1.5 ns when all output gates have a load factor of 2. Determine the delay. Try to achieve a result with small area within the timing restrictions. Determine the area.

Hint: Buffers are a great help here to manage fanout and delay

Gate	Fanin	Fanout	T_p (ns)	Load (L)	Area (EG)
NAND	2	12	0.05+0.04L	1	1
NOR	2	12	0.07+0.05L	1	1
NOT	1	12	0.02+0.02L	1	1
BUFFER	1	∞	0.15+0.01L	2	4

T_p = propagation delay, L = standard load, EG = equivalent gates