

### Paper Exercise 3

1.

a) The output equation  $Y$  with the helper variables is given by:

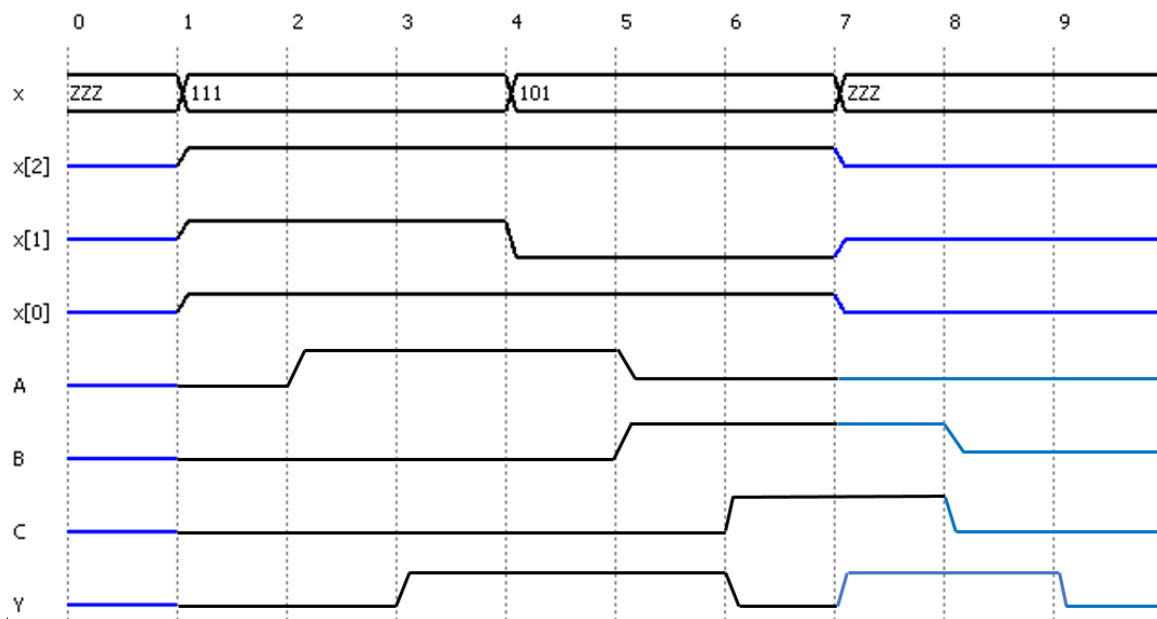
$$Y = A + C$$

$$= x_1 \cdot x_2 + \bar{x}_1 \cdot x_0$$

b) The critical path assuming each gate has the same unit delay regardless of load and gate type is expressed / defined as:

$$U-1 \rightarrow U-2 \rightarrow U-3$$

c) Timing diagram is shown below



- d) The problems in the circuit can be fixed by adding two buffers between gate and u-0 and or u-3. Each buffer should have unit delay.

