	SRI INDU COLLEGE OF ENGG & TECHNOLOGY QUESTION BANK (Regulation :R20) Department of CSE (AI&ML)		Prepared on oct-29-2021
	Sub. Code & Title	**R20CSE2102 Computer Organization and Architecture**	
	Academic Year: 2021-22	**Year/Sem./Section**	**Academic Year: 2021-22**
	Faculty Name & Designation	**M.SWATHI REDDY, ASST.PROFESSOR**	

QUESTION BANK WITH BLOOMS TAXONOMY LEVEL (BTL)

(1. Remembering 2. Understanding 3. Applying 4.Analyzing 5. Evaluating 6. Creating)

UNIT-I: Digital Computers, Basic Computer Organization and Design			
	1 MARK Questions	**BT LEVEL**	**COURSE OUTCOME**
1	Define Computer Architecture?	1	CO1
2	Define a Digital Computer? Draw block diagram of Computer?	1	CO1
3	What is the need of Register? Explain the different types of Registers?	1	CO1
4	What is control memory? Oct-2020	1	CO3
5	Define a Micro Program & Micro Instruction?	1	CO1
6	Define CO,CA and CD.?	1	CO1
7	Define Instruction Cycle?	1	CO1
8	List Computer Registers**?**	1	CO1
9	Discuss Timing And Control?	2	CO1
10	Explain About ALU?	2	CO1
	10 MARKS		
1	How to do address sequencing with diagram?	5	CO1
2	What is instruction format? Explain the different instruction formats in detail?	5	CO1
3	Explain the different phases of Instruction Cycle?	2	CO1
4	Explain the Micro Program Control with Diagram & Examples?	2	CO1
5	List out any 5 Registers with explains in detail?	5	CO1
6	Demonstrate the Three – State Bus Buffer with neat diagram?	3	CO1
7	List and Explain in detail about the memory reference Instructions?	1	CO1
8	Draw the flowchart for interrupt cycle and experiment with it with explanation? Oct-2020	3	CO1
9	Determine the input-output configuration?	3	CO1
10	Explain the stored program organization with neat diagram?	2	CO1
11	Explain the bus system for four registers using multiplexer with neat diagram?	2	CO1

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Unit -II : Micro programmed Control, Central Processing Unit			
	1 MARK Questions	**BT LEVEL**	**COURSE OUTCOME**
1	Define Data path.?	1	CO2
2	Define Latency and throughput?	1	CO2
3	Discuss the principle operation of micro programmed control unit?	2	CO2
4	What is control store?	2	CO2
5	Define Processor clock?	1	CO2
6	Write example micro programs?	2	CO2
7	Define control unit.?	1	CO2
8	Define Program Control?	1	CO2
9	Explain data representation?	2	CO5
10	What is Floating Point Representation?	2	CO5
	10 MARK Questions		
1	Draw and explain typical hardware control unit?	2	CO2
2.	Draw and explain about micro program control unit?	2	CO2
3.	Write short notes on (i) Micro instruction format **(ii)** Symbolic micro instruction.	2	CO2
4.	Explain multiple bus organization in detail?	2	CO2
5.	Explain in detail about address sequencing?	2	CO2
6.	Explain in detail about conditional branching with neat diagram?	2	CO2
7.	Explain general register organization in detail with neat diagrams ?	2	CO2
8	Explain Stack organization in detail with neat diagrams?	2	CO2
9.	Evaluate the following program using three address Instruction format X = (A+B) * (C+D) Nov-2019	3	CO2
10.	Evaluate the following program using two address Instruction format X = (A+B) * (C+D) Nov-2019	3	CO2
11.	Evaluate the following program using one address Instruction format X = (A+B) * (C+D) Nov-2019	3	CO2
12.	Classify addressing modes and explain each type with example? Oct-2020	1	CO2

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Unit -III : Data Representation,Computer Arithmetic			
	1 MARK Questions	**BT LEVEL**	**COURSE OUTCOME**
1.	Convert the following decimal number to the base indicated 7562 to octal 1938 to hexadecimal?	1	CO3
2.	Find the 1's and 2's complement of the following eight digit binary number a. 10101110 b. 10000001?	1	CO3
3	List the steps of Booth's Multiplication algorithm? Dec-2019	1	CO3
4	Convert the following decimal number to the base indicated 17562 to octal 11938 to hexadecimal?	2	CO3
5	Briefly explain r's complement with example?	2	CO3
6	List out computer arithmetic operations?	1	CO3
7	Design division algorithm? Nov-2018	6	CO2
8	Explain floating point arithmetic?	2	CO3
9	Explain about different Data types?	2	CO3
10	Explain about Fixed point Representation?	2	CO3
	10 MARKS		
1.	Draw and explain the hardware for signed – magnitude addition and subtraction?	2	CO3
2	Explain the booth's multiplication algorithm with neat sketch of hardware design?	2	CO3
3.	Perform division of 1000 and 0011 using restoring division algorithm?	3	CO3
4	Multiply 7 and 3 using Booth's algorithm?	2	CO3
5.	Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation?	2	CO3
6	Multiply each of the following pairs of signed 2's compliment numbers using the Booth multiplication and n- bit multipliers. In each case assume that A is multiplicand and B is multiplier. (i) A=010111 and B=110110. (ii) A=110011 and B=101100 ?	3	CO3
7.	Discuss about the IEEE standard for binary floating point arithmetic?	2	CO3
8.	Draw the flowchart for divide operation and explain?	2	CO3
9.	Draw and explain the one stage decimal arithmetic unit**?**	2	CO3
10.	Explain in detail about the derivation of BCD adder? Nov-2018	2	CO3

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Unit-IV : Input Output Organization, Memory Organization

1 MARK QUESTIONS

1.	What is DMA? Oct-2020	2	CO4
2.	What is the need of I/O Interface? Oct-2020	1	CO4
3.	Define Priority Interrupt?	1	CO4
4.	List out any 5 IO Devices?	1	CO4
5.	What are peripheral devices? Give a note on video monitors?	2	CO4
6.	Discuss Asynchronous Data?	2	CO4
7.	Explain Main Memory ?	2	CO3
8	Define Cache Memory, Auxilary Memory, Associate Memory? Nov-2019	1	CO3
9	Explain Modes of transfer ?	2	CO4
10	Define IOI?	1	CO4

10 MARKS QUESTIONS

1.	What is asynchronous data transfer? Explain the different types of Asynchronous data transfer techniques?	2	CO4
2.	Explain in detail floating point arithmetic operations with examples?	2	CO4
3.	What is IOP? Explain the communication between IOP and CPU?	2	CO4
4.	Explain the following data transfer modes/techniques? a)Program Controlled IO b)Interrupt Initiated IO	2	CO4
5.	Write a note on memory hierarchy with the neat diagram? Nov-2019	2	CO3
6.	Consider a cache consisting of 256 blocks of 8 words each, for a total of 2048 words, and assume that the main memory is addressable by a 16-bit address. The main memory has 64K words which are divided into 8192 blocks of 8 words each. Find the number of bits in Tag, Block and Word Field of the main memory address for direct mapping scheme?	1	CO4
7.	Explain in detail about DMA operation with neat diagram ? Nov-2019	2	CO4
8	Describe in brief the different modes by which data transfer can take place between a Computer unit and its I/O devices. What is the difference between synchronous and asynchronous data transfer? Nov-2018	2	CO4
9	Explain in detail about Cache memory mechanisms? Oct-2020	2	CO3
10	Explain in detail about Associative memory mechanisms?	2	CO3

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Unit-V: Reduced Instruction Set Computer, Pipeline &Vector Processing , Multiprocessors			
1 MARK QUESTIONS			
1.	List out the memory hierarchy?	1	CO3
2.	What is associative memory?	1	CO3
3.	What is the need of Cache Memory?	1	CO3
4.	Define a Pipeline? Give an example?	2	CO4
5.	What is inter process arbitration?	2	CO6
6.	Define Vector Processing?	2	CO6
7.	Define RISC & CISC?	1	CO6
8.	Define IPC And Synchronization?	1	CO6
9.	List out pipelining types?	1	CO4
10.	Discuss the difference between RISC & CISC? (Dec 2019)	2	CO6
10 MARKS QUESTIONS			
1.	Explain the different types of Pipeline techniques? Nov-2019	2	CO4
2.	What is mean by IPC. Explain the Concurrency & Synchronization with IPC?	2	CO6
3.	What is Multiprocessors? Explain in detail ?	1	CO6
4	List out Cache mapping techniques and Explain all the mapping techniques?	2	CO6
5.	Define Auxiliary memory ? Explain with neat diagram?	2	CO6
6.	Explain in detail about the RISC Characteristics? Oct-2020	2	CO6
7.	Explain in detail about the CISC Characteristics?	2	CO6
8	Explain in detail about the Instruction Pipeline?	2	CO4
9	List the Characteristics of Multiprocessors. Explain in detail about the Interconnection structures of Multiprocessor?	2	CO6
10	Explain in detail about the Inter processor arbitration ?	2	CO6

END EXAMINATION- MODEL PAPER

BR-20 **D4**
Subject Code: R20CSE2102

SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY

(An Autonomous Institution under UGC, New Delhi)Recognized under 2(f) and 12(B) of UGC Act 1956

II B.Tech - I Semester –End Examinations (Model paper)

COMPUTER ORGANIZATION & ARCHITECTURE

Duration: 3 Hrs **Max Marks: 70M**

Section – A

Answer *All* the following questions **Marks: 5Qx4M = 20M**

1. Define Computer Architecture?
2. What is Floating Point Representation?
3. Find the 1's and 2's complement of the following eight digit binary number?
   a. 10101110
   b. 10000001
4. Explain Modes of transfer**?**
5. Differentiate between the RISC & CISC**?**

Section – B

Answer any *FIVE* questions choosing at least one from each Unit

Marks: 5Qx10M = 50M

UNIT - I

6. Explain the stored program organization with neat diagram?

(OR)

7. Draw the flowchart for interrupt cycle and experiment with it with explanation**?**

UNIT - II

8. Evaluate the following program using one address Instruction format
   X = (A+B) * (C+D)?

(OR)

9. Draw and explain typical hardware control unit?

UNIT - III

10. Perform division of 1000 and 0011 using restoring division algorithm**?**

(OR)

11. Explain floating point arithmetic**?**

UNIT - IV

12. Describe in brief the different modes by which data transfer can take place between a computer unit and its I/O devices. What is the difference between synchronous and asynchronous data transfer**?**

(OR)

13. Write a note on memory hierarchy with the neat diagram?

UNIT - V

14. Write the Characteristics of Multiprocessors. Explain in detail about the Interconnection structures of Multiprocessor**?**

(OR)

15. Explain the different types of Pipeline techniques**?**

MID I MODEL PAPER

BR-20 SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY D4

(An Autonomous Institution Under 2(f) and 12(B) of UGC Act 1956, New Delhi)

II B.Tech - I Semester - I Mid Term Examinations (Model paper)

(R20CSE2102) COMPUTER ORGANIZATION & ARCHITECTURE

Duration: 90Mins **Max Marks: 25M**

Section – A

Answer *All* the questions **5Qx1M = 5M**

1. Define Computer Architecture?
2. Explain data representation?
3. What is control memory**?**
4. Define control unit?
5. Find the 1's and 2's complement of the following eight digit binary number.
   a. 10101110
   b. 10000001

Section – B

Answer any *FOUR* questions **4Qx5M = 20M**

6. Explain about Von Neumann architecture**?**
7. Draw the flowchart for interrupt cycle and experiment with explanation**?**
8. Evaluate the following program using three address Instruction format
   X = (A+B) * (C+D) **?**
9. Explain multiple bus organization in detail?
10. Explain the booth's algorithm with neat sketch of hardware design **?**
11. Explain the different phases of instruction cycle?

MID-2 MODEL PAPER

BR-20 SRI INDU COLLEGE OF ENGINEERING & TECHNOLOGY D4

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II B.Tech - I Semester - II Mid Term Examinations (Model paper)

(R20CSE2102) COMPUTER ORGANIZATION & ARCHITECTURE

Duration: 90Mins **Max Marks: 25M**

Section – A

Answer *All* the questions **5Qx1M = 5M**

1. List out the steps of Booth's algorithm**?**
2. Define Priority Interrupt**?**
3. Define Cache Memory, Auxilary Memory, Associate Memory**?**
4. Differentiate between the RISC & CISC**?**
5. Explain Vector Processing?

Section – B

Answer any *FOUR* questions **4Qx5M = 20M**

6. Explain about Von Neumann architecture**?**
7. Evaluate the following program using one address Instruction format
   X = (A+B) * (C+D) **?**
8. Describe in brief the different modes by which data transfer can take place between a computer unit and its I/O devices. What is the difference between synchronous and asynchronous data transfer**?**
9. Explain the different types of Pipeline techniques**?**
10. Write the Characteristics of Multiprocessors. Explain in detail about the Interconnection structures of Multiprocessor**?**
11. . Explain in detail about the Instruction Pipeline?