Multi-Beam 8×8 RF Aperture Digital Beamformers Using Multiplierless 2-D FFT Approximations

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***Abstract*—The two-dimensional (2-D) discrete Fourier transform (DFT) is widely used in digital signal processing (DSP) and computing applications. Fast Fourier transforms (FFTs) are widely used as low-complexity algorithms for the computation of the DFT as it reduces the required computation operations from $O(N^2)$ to $O(N \log_2 N)$. The multiplicative complexity is used as a benchmark in comparing different algorithms as it affects the circuit complexity, chip area and power. This paper introduces a new class of multiplierless hardware algorithm consisting only of arithmetic adder circuits that closely approximates the 2-D version of the 8-point DFT. The paper discusses the theory behind the proposed new algorithm, with the DFT presented in the form of an 8×8 matrix. Furthermore it provide a multi-beam RF aperture application example where the 2-D DFT approximation has been used to closely obtain the antenna array patterns.**

***Keywords*—DSP, FFT, arrays, beamforming, aperture, multi-beam.**

I. Introduction

Radio-frequency (RF) antenna arrays have extensive applications in wireless communications [1], [2], radar [3], and microwave/mm-wave imaging systems [4]. The ability to generate a large amount of simultaneous wideband RF beams, where a "beam" refers to the directional enhancement of a propagating spatio-temporal electromagnetic planar wave based on the direction of arrival (DOA) of the wave, is highly-desired in a plethora of RF and wireless applications [5], [6].

A particularly important emerging application for multiple beams would be in the area of massively multiple-input multiple-output (MIMO) wireless systems that are attempting to utilize unused and currently unlicensed bandwidth in the 25-150 GHz region of the electromagnetic spectrum [7]. The exploitation of mm-wave frequencies at these high frequency bands is particularly suited for establishing a large number of high-bandwidth connections over relatively short distances (within a room, for example), to connect a base station with a multitude of mobile wireless devices as shown in Fig. 1.

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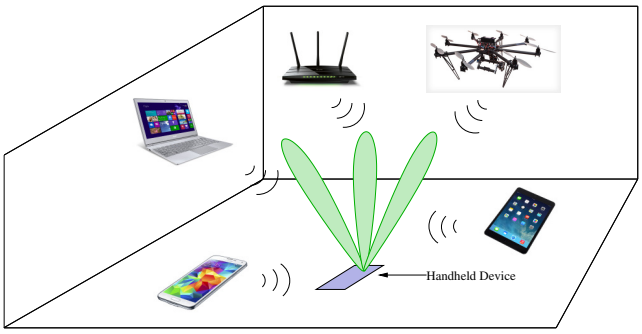

Fig. 1: Example of high-bandwidth connections over relatively short distances.

The need for such massive connectivity within a small geographic area is an expected outcome of the rapidly expanding topic of the internet of things (IoT) [8], [9]. The IoT may involve wearable technologies, body area networks (BANs), consumer electronics, network infrastructure, smart home technologies, security, smart connected health, and vehicular technologies and networks, such as vehicle to vehicle (V2V) and vehicle to infrastructure (V2I), and urban unmanned aerial systems (UAS), for example [10], [11]. In light the above, this paper discusses a new technique for achieving 64 multi-beams at RF using a low-complexity digital signal processing (DSP) architecture, which makes use of the proposed 8-point *approximate* discrete Fourier transform (DFT) operation [12].

As a design specific ratio, we assume our need is to realize a miniaturized digital antenna aperture array receiver providing 64 RF beams arranged in an 8×8 grid in the angular domain. The operational (center) frequency is assumed at 70 GHz, for purposes of explanation. The bandwidth per beam is

assumed to be 500 MHz, which is sufficient for maintaining 500 Mbps data rates, as a minimum requirement, using even the basic binary phase shift keying (BPSK) modulation method. In practice, advanced modulation and coding schemes support better data rates over each RF beam. We chose 500 MHz of bandwidth per RF beam so that the required digital architecture is easily achievable using relatively low-cost VLSI CMOS fabrication techniques. At an RF frequency of $f = 70$ GHz, the wavelength is $\lambda = 4.28$ mm, which makes the Nyquist spacing of the array $\Delta x = \lambda/2 = 2.14$ mm. For an 8×8 element planar square antenna array, the total array size is 15×15 mm in size, making it small enough to fit on a variety of wearable/mobile devices.

II. Approximate DFT Rectangular Aperture

The two-dimensional (2-D) DFT is widely used in digital signal processing and computing applications, such as multi-beamforming radio-frequency (RF) and ultrasonic apertures, image watermarking [13], fingerprint recognition [14], texture feature extraction [15], medical imaging [16], [17], synthetic aperture radar (SAR) processing [18], and digital holographic imaging [19]. The fast Fourier transforms (FFTs) are a class of low-complexity algorithms for efficient DFT computation. A direct computation of a DFT requires a number of arithmetic operations in $O(N^2)$, whereas FFTs usually require as few as $O(N \log_2 N)$ operations. The multiplicative complexity is employed as a figure-of-merit for comparing different algorithms. The multiplicative complexity directly relates to the circuit complexity, chip area, and power consumption of a given implementation. Recently, fast approximation DFT algorithms have played a key role in offering low computational cost replacements for real world applications that can tolerate a provably small amount of error in the DFT filterbank responses. The main goal of this paper is to exploit multiplierless DFT approximations and their fast algorithm realizations for furnishing high-speed multi-beam RF receive and transmit-mode apertures for wireless communications, radar, RF sensing, and microwave/mm-wave imaging systems.

In this context, we introduce a new class of multiplierless hardware algorithm consisting only of highly-parallel fine-grain pipelined digital arithmetic adder circuits that closely-approximates the 2-D 8×8-point DFT. By completely eliminating multiplications in the proposed approximate DFT, we furnish major reductions in circuit complexity, chip area, and power consumption in any digital system that utilizes the 2-D DFT. The circuit complexity, area, and power consumption of parallel multipliers exceed that of parallel adders. By realizing the proposed approximation, we advanced low-complexity low-power circuit designs for digital signal processing systems.

The paper discusses the theory behind the proposed new algorithm, along with the required calculations. The proposed 8-point DFT is presented in the form of an 8×8 matrix. Fig. 2 provides a multi-beam RF aperture application example, where we can use the 2-D DFT approximation to closely resemble antenna array patterns. The whole antenna grid will consist of 64 independent beam patterns. Several of them have been graphically shown in the figure.

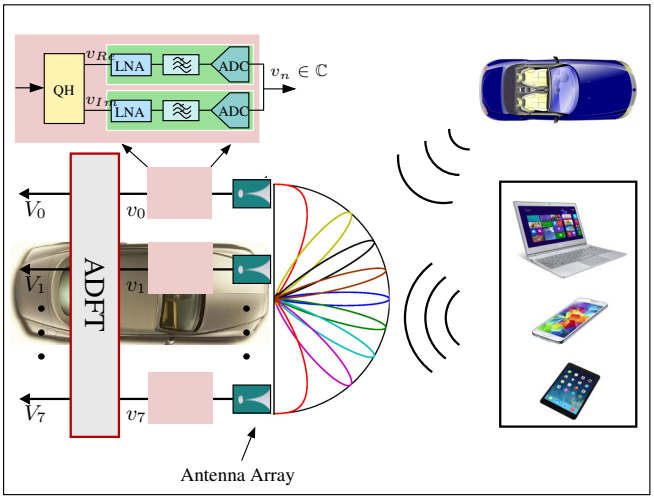

Fig. 2: ULA based multi-beam RF aperture application using a spatial DFT.

III. Proposed Low-Complexity DFT Approximations

The DFT is a linear orthogonal transformation where the N-point input signal is a vector of values $\mathbf{v} = [v_0 \quad v_1 \quad \dots \quad v_N]^\top$ and can be related to an output vector in the frequency domain $\mathbf{V} = [V_0 \quad V_1 \quad \dots \quad V_N]^\top$ according to

$$V_k = \sum_{n=0}^{N-1} v_n \cdot \omega_N^{kn}, \quad k = 0, 1, \dots, N-1,$$

where $j = \sqrt{-1}$ and $\omega_N = \exp\left\{\frac{-2\pi j}{N}\right\}$ is the Nth root of unity [20]. The above expression is available in matrix form as

$$\mathbf{V} = \mathbf{F}_N \mathbf{v},$$

where $\mathbf{F}_N$ is the transformation matrix of the DFT, whose (i,k)-element is given by $\mathbf{F}_{i,k} = \omega_N^{(i-1)(k-1)}$ for $i, k = 1, 2, \dots N$. To derive a low complexity algorithm, each $\mathbf{F}_{i,k}$ must be defined over a set of small integer values, usually $\mathcal{P} = \{0, \pm 1/2, \pm 1, \pm 2\}$ [21]. Small integer multipliers are important in digital VLSI design of real-time architectures because they can be realized using simple re-wiring schemes that do not consume energy to accomplish a multiplication operation. Hence $\mathcal{P}$ is designed to approximate discrete transforms the following set of low complexity values in the complex field is proposed:

$$\mathcal{Q} = \Big\{ z \in \mathbb{C} : \Re\{z\} \in \mathcal{P} \wedge \Im\{z\} \in \mathcal{P} \Big\},$$

The set of values represented by $\mathcal{Q}$ can be used for both real and imaginary components of the transform and then combined together to form the complex-valued approximate DFT.

A. 8-point DFT Approximation

We employ an approximate DFT to minimize the adder arithmetic complexity of the 8-point approximate DFT computation. The proposed 8-point approximate DFT matrix $\mathbf{F}_8$ can be derived using the parametric optimization method described in [22]. The two major constraints that is imposed on the proposed approximation are: (i) near-orthogonality and

(ii) low-complexity. As a result, we can obtain that the optimal elements for the parametric approximation of $\mathbf{F}_8$, and can be given by

$$\alpha_8^* = \begin{bmatrix} 1 & \dfrac{1-j}{2} & -j \end{bmatrix}.$$

Such parameters result in the following matrix approximation:

$$\hat{\mathbf{F}}_8 = \frac{1}{2} \cdot \begin{bmatrix} 2 & 2 & 2 & 2 & 2 & 2 & 2 & 2 \\ 2 & 1-j & -2j & -1-j & -2 & -1+j & 2j & 1+j \\ 2 & -2j & -2 & 2j & 2 & -2j & -2 & 2j \\ 2 & -1-j & 2j & 1-j & -2 & 1+j & -2j & -1+j \\ 2 & -2 & 2 & -2 & 2 & -2 & 2 & -2 \\ 2 & -1+j & -2j & 1+j & -2 & 1-j & 2j & -1-j \\ 2 & 2j & -2 & -2j & 2 & 2j & -2 & -2j \\ 2 & 1+j & 2j & -1+j & -2 & -1-j & -2j & 1-j \end{bmatrix}.$$

The proposed 8-point transform $\hat{\mathbf{F}}_8$ preserves the symmetry of

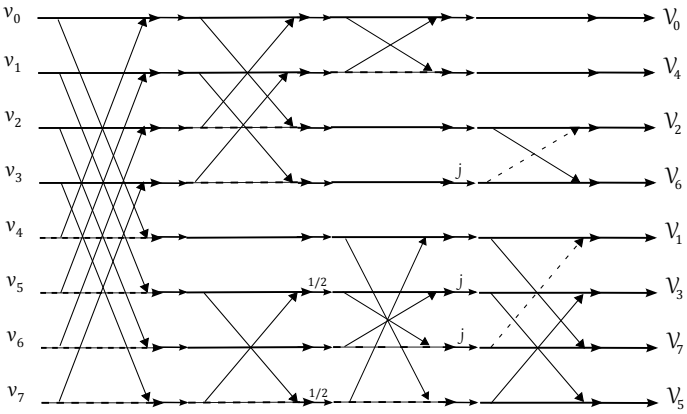

Fig. 3: Signal flow graph for the factorization of $\hat{\mathbf{F}}_8$. Input data v_i, $i = 0, 1, \ldots, 7$, relates to the output V_k, $k = 0, 1, \ldots, 7$. Dotted arrows represent multiplications by -1.

the DFT and has zero multiplicative complexity requiring only 64 real additions and 32 bit-shifting operations. A tailored fast algorithm based on the matrix factorization methods suggested in [23], can be used to further reduce the additive complexity. The fast algorithm can be represented as:

$$\hat{\mathbf{F}}_8 = \mathbf{Y}_4 \cdot \mathbf{Y}_3 \cdot \mathbf{D}_1 \cdot \mathbf{Y}_2 \cdot \mathbf{D}_2 \cdot \mathbf{Y}_1 \cdot \mathbf{P},$$

where

$$\mathbf{Y}_4 = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 \end{bmatrix}, \mathbf{Y}_3 = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 \end{bmatrix},$$

$$\mathbf{Y}_2 = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & -1 \end{bmatrix}, \mathbf{Y}_1 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix},$$

$\mathbf{D}_1 = \text{diag}\,[1, \ 1, \ 1, \ 1, \ 1, \ 1/2, \ 1, \ 1/2]$,
$\mathbf{D}_2 = \text{diag}\,[1, \ 1, \ 1, \ j, \ 1, \ j, \ j, \ 1]$,
$\mathbf{P} = \begin{bmatrix} \mathbf{e}_1 & \mathbf{e}_5 & \mathbf{e}_3 & \mathbf{e}_7 & \mathbf{e}_2 & \mathbf{e}_4 & \mathbf{e}_8 & \mathbf{e}_6 \end{bmatrix}^\top$ is a permutation matrix, and $\mathbf{e}_i$ is the 8-point column vector with element 1 at the ith position and 0 elsewhere. The above proposed 8-point algorithm has reduced the required real additions to 26 along with two bit-shifting operations. Fig. 3 depicts the signal flow graph of the fast algorithm of the 1-D 8-point approximate DFT. Traditionally, the 2-D version of the DFT is computed using a row-column (RC) decomposition, where initially instantiations of the 1-D DFT are computed along the rows followed by calls of the 1-D DFT along the columns to get the 2-D version of the algorithm. For the 8×8 block $\mathbf{A}_8$ has its 2-D transform mathematically expressed by [24]:

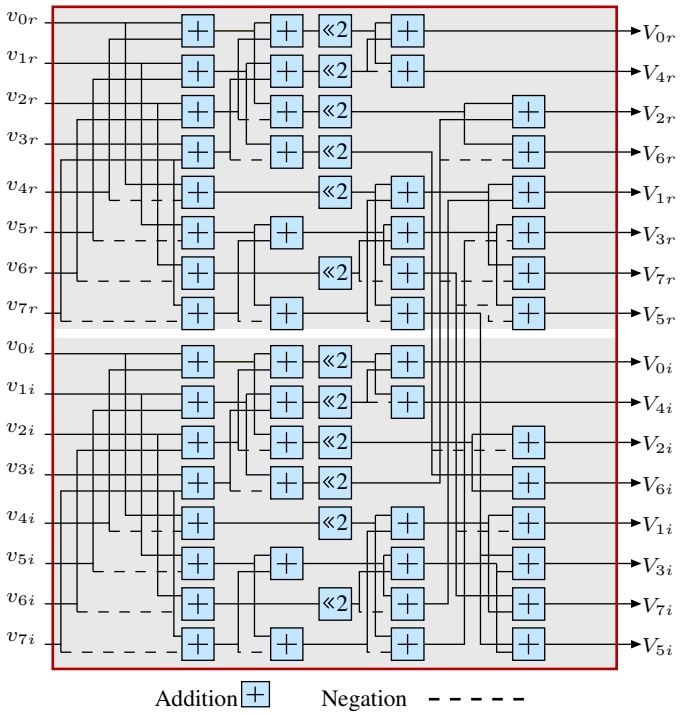

Fig. 4: Digital architecture of the proposed 8-point DFT.

$$\mathbf{B}_8 = \hat{\mathbf{F}}_8 \cdot \mathbf{A}_8 \cdot \hat{\mathbf{F}}_8^\top,$$

where $\mathbf{B}_8$ is the 8×8 block output matrix in frequency.

IV. Simulation Results and Array Patterns

The 1-D DFT over eight antennas arranged in a ULA leads to the well-known 8-beam complex-valued multi-beamformers [5], where at each time sample, the array "snapshot" or frame of ADC values, is subject to an 8-point spatial DFT using an FFT algorithm (e.g., Cooley-Tukey Algorithm or Winograd Algorithm). The typical arithmetic complexity for an FFT is $O(N \log_2 N)$ [23]. The replacement of the FFT with the the proposed approximation, with implementation of the proposed fast algorithm, leads to eight beams that are almost identical in shape (main lobe and side-lobe responses) while being totally free of parallel hardware multipliers. The digital architecture of the 8-point approximate DFT is shown in Fig. 4.

The 2-D DFT can also be generated from a 8×8 idealized antenna array and the Fig. 5 show the signal flow graph implementations of a real-time 64 beam RF aperture. Simulation results were taken for an 8×8 idealized antenna array and the normalized array factors for the 8-beams are shown in Fig. 6. The absolute difference between the normalized approximate beams and the beams from the ideal DFT is shown in Fig. 7,

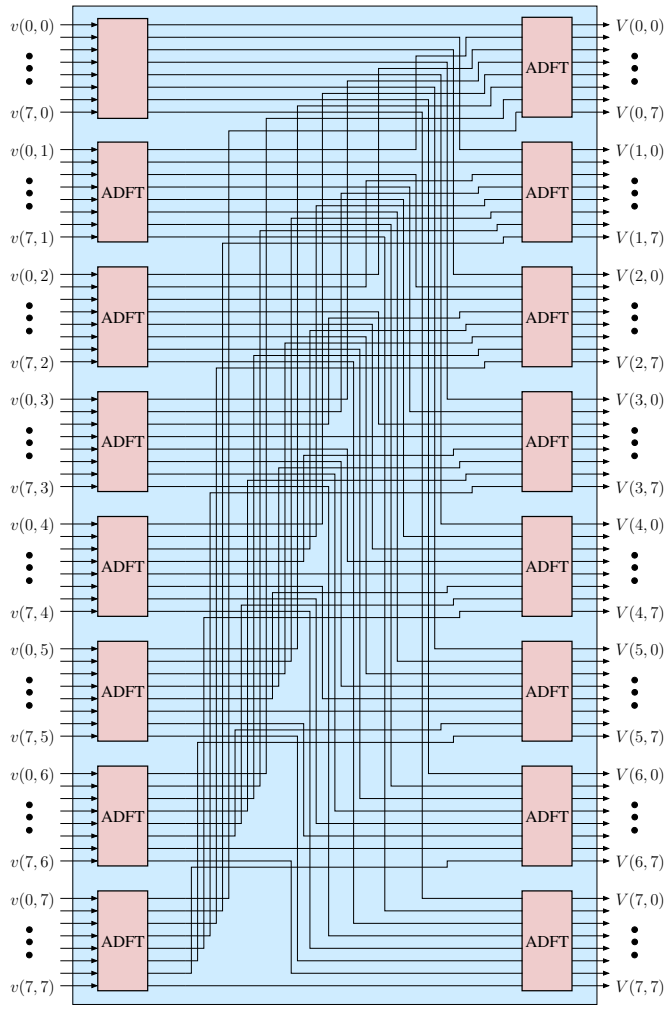

Fig. 5: Signal flow graph implementation of a real-time 64 beam RF aperture.

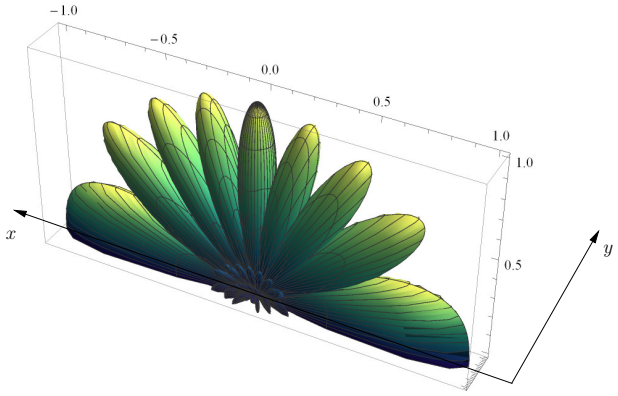

Fig. 6: Normalized array beams for the 8-beams.

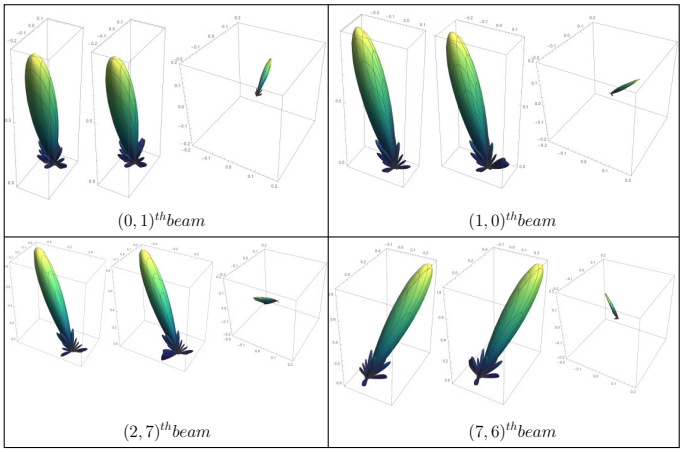

Fig. 7: Array pattern from the Ideal DFT, array pattern from the approximate DFT and the absolute difference.

where it is clear that the adoption of the approximate DFT in place of the DFT leads to only minor differences in the beam shapes. In our simulation setup, we modeled the complex filter bank responses of both DFT and approximated-DFT and found the complex error between each of the bins. The magnitude of this error was plotted as a function of frequency, in polar format. The error characteristics appear as a small deviation of the minor lobes in the array factor of the aperture antenna. The major advantage of the proposed approximation beamformer is that it does not require multiplier digital VLSI hardware, in turn, leading to lower VLSI silicon real-estate on chip and lower power consumption. The reduction in chip-area and power consumption is expected because parallel multipliers are significantly larger and complicated compared to parallel adder hardware. Further, the approximate DFT—although free of multipliers—does not require any more adders than an equivalent FFT (generally, the adder arithmetic complexity for both FFT and its approximation is $\mathrm{O}(N \log N)$), making the reduction in circuit complexity quite significant.

V. Conclusion

We introduce a new class of multiplierless hardware algorithm consisting only of arithmetic adder circuits that closely-approximates the 2-D version of the 8-point DFT. By eliminating multiplication operations in the proposed approximate DFT, unprecedented improvements in circuit complexity, chip area and power consumption can be achieved in any digital system that utilizes 2-D DFTs. We discuss design specifications in establishing a large number of high-bandwidth connections over relatively short distances and miniaturized digital antenna aperture array receivers. Simulation results that closely resemble the antenna array patterns for the 2-D DFT and several beam examples for the ideal DFT, approximate DFT and the absolute difference are provided

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