Nine Level Cascaded H Bridge Inverter (For High Performing UPS Applications)

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***Abstract*— This paper proposes a nine level Cascaded H-Bridge Multi-Level Inverter, realized via Distortion Minimization PWM technology which is incorporated in an Uninterrupted Power Supply (UPS), operating in the low power end. The proposed UPS is capable of supplying four typical personal computers simultaneously. Due to the increased number of switching power poles used, switching frequency per device is reduced, minimizing the switching stress per device. Thus a prolonged lifetime of the inverter can be anticipated. Moreover, the suitability of Distortion minimization PWM for this inverter design is discussed compared to Selective Harmonic Elimination PWM (SHEPWM): one of the most popular PWM methods for multi-level inverters.**

Furthermore, in order to incorporate the designed inverter in a UPS application such that cost, weight and size are minimized while ensuring a good transient response at the failure of the mains supply, a novel approach named "Offline Synchronization": an attempt to combine the advantages of both offline UPSs and Online UPSs is introduced.

Keywords—Cascaded H-Bridge Multi-Level Inverter technology, Uninterrupted Power Supply (UPS), Offline Synchronization, Total Harmonic Distortion (THD), Distortion minimization PWM, Selective Harmonic Elimination PWM (SHEPWM)

I. INTRODUCTION

Multi-level inverters have been a great concern of many researchers, for more than three decades, fostering the growth of many successful industrial applications. Among those techniques, Cascaded H-Bridge (CHB) Multi-Level Inverter technology is rapidly gaining popularity due to many of its advantages [1-3]. The basic idea of this technology is cascading several DC sources to obtain a stepped voltage output of higher magnitude [3], which can then be filtered out (if necessary), to get a sinusoidal output waveform.

So far, the CHB technology had been predominantly used in high power applications. But here, a successful attempt has been taken to incorporate this technology for a low power application: a high performing Uninterrupted Power Supply (UPS).

The proposed UPS has the capacity of serving four typical personal computers (230V, 1.5A maximum current), and thus can be used in place of four separate UPSs. The design is flexible of expanding into a higher capacity, simply by upgrading the current ratings of the components and therefore has the potential of serving much larger loads as well. The voltage and the current ratings of the proposed UPS are 230V and 6A respectively.

The proposed UPS comprises of several units, of which the basic arrangement is shown below.

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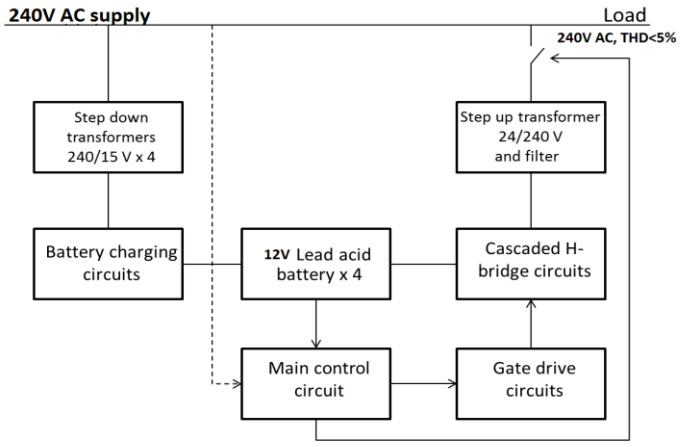

Fig. 1. Schematic diagram of the UPS

II. INVERTER WITH NINE LEVEL CASCADED H BRIDGE TOPOLOGY

A. Multilevel cascaded H bridge topology

The most salient feature of this UPS is its inverter, designed using Cascaded H-Bridge Multi-Level Inverter technology. Among the many advantages of a multi-level inverter, reduced switching frequency and reduced voltage applied per semiconductor device are prominent. Both these attributes significantly reduce the switching stress per semiconductor device and thereby prolong the semiconductor devices' lifetimes improving the durability of the proposed UPS.

Diode-clamped multilevel inverter, Flying-capacitor multilevel inverter, or Hybrid multilevel inverters are further options [2,4]. Anyway, Cascaded H-bridge multilevel technology is more appropriate for this particular application as the input is in the form of four separate batteries, which are used to achieve a stepped AC voltage waveform at the output.

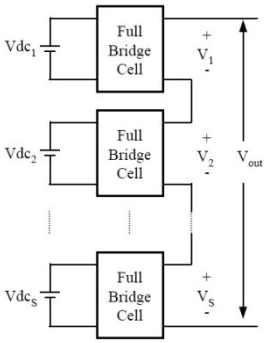

Fig. 2. Topology of cascaded H-bridge multi-level Inverter

The voltages of each of the four batteries are approximately equal and thus equal step size is assumed, reducing the complexity of the controller. Therefore, this can be identified as a symmetrical source inverter. Furthermore, the use of equal size batteries gives the advantage of easy replacement as well.

The relationship between the number of DC sources and the output levels are given by the following equation [5];

$$N = 2 \times s + 1 \tag{1}$$

Where;

N: Number of levels of the output

s: Number of separate DC sources

With the increasing number of output levels (N), the output quality improves, yet at the cost of elevated complexity, size and expense. Thus, to achieve a compromise between those factors, the proposed inverter is designed for nine levels, for which four separate DC sources are required. Moreover, as the proposed UPS is intended to replace four conventional UPSs, selection of four DC sources is justified.

B. Switching algorthim of the inverter

As it is one of our major considerations to keep the switching stress per device at a minimum, intermediate switching is not used. Therefore, only four switching angles per quarter cycle are used, which control the switching of four batteries, resulting in a stepped output waveform. (Anyway, there are other approaches as well, to reduce the switching loss [6].)

The use of an appropriate switching technique holds an utmost importance in designing an inverter with an output of satisfactory quality [5, 8]. Selective Harmonic elimination pulse width modulation (SHE PWM) and Distortion Minimization pulse width modulation are two of the best techniques which can be used when a given number of switching points is used per quarter cycle [5,7-10].

It is worthwhile to note that certain modifications have to be made to these conventional PWM technologies, when used with multi-level inverters [5]. Following is a comparison of the applicability of modified versions of Distortion Minimization PWM and Selective Harmonic Elimination PWM in suppressing the harmonic content of multi-level inverters.

The equation for THD can be written as;

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} h_n^2}}{h_1} \tag{2}$$

If we consider the output waveform of a multilevel cascaded H bridge inverter, due to its odd symmetry, Cosine terms of the Fourier series vanish out. Furthermore due to the quarter wave symmetry, even harmonics too are not present [10].

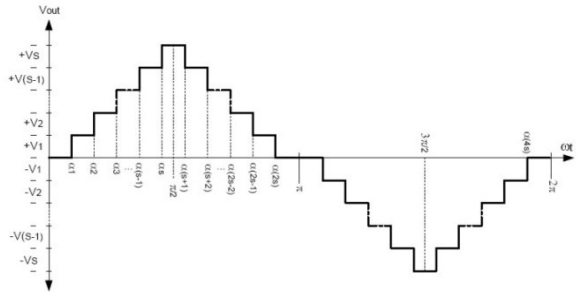

Fig. 3. Stepped output waveform

Considering the odd symmetrical nature, the Fourier series of the waveform can be written in the following form. Let

$$\alpha = \omega t \tag{3}$$

$$f(\alpha) = \sum_{n=1}^{\infty} a_n \sin(n\alpha) \tag{4}$$

Where, amplitude of the n^{th} harmonic is given by,

$$a_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} f(\alpha) \sin(n\alpha) d\alpha \tag{5}$$

If we take switching angles in the quarter cycle as $a_1, a_2, a_3, .. a_{s-1}, a_s$
For odd n,

$$a_n = \frac{4E}{n\pi}[\cos(na_1) + \cos(na_2) + \cdots + \cos(na_s)] \tag{6}$$

For even n,

$$a_n = 0 \tag{7}$$

In a more convenient form,
For odd n,

$$a_n = \frac{4E}{n\pi}\sum_{k=1}^{s} \cos(n\alpha_k) \tag{8}$$

Thus, the equation for the THD can be rearranged as;

$$THD = \frac{\sqrt{\sum_{n=1}^{\infty}\left\{\frac{1}{(2n+1)}\sum_{k=1}^{s}\cos[(2n+1)\alpha_k]\right\}^2}}{\sum_{k=1}^{s}\cos(\alpha_k)} \tag{9}$$

The modulation index (m) for the multilevel case can be defined as;

$$m = \frac{V_{out}}{sV_{dc}} \tag{10}$$

Where, V_{out} is the amplitude of the output voltage at the fundamental frequency.

Here, there are only four switching angles per quarter cycle of the output voltage waveform (since four DC sources are used and no intermediate switching is done).

After substitution and simplification, the equation for the fundamental can be given as;

$$m\pi = \cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) \tag{11}$$

$$0 = (\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) - m\pi \tag{12}$$

For all practical purposes, reasonable approximation for the THD can be done by considering only the first 61 harmonics [5].

$$THD = \frac{\sqrt{\sum_{n=1}^{30}\left\{\frac{1}{(2n+1)}\sum_{k=1}^{4}\cos[(2n+1)\alpha_k]\right\}^2}}{\sum_{k=1}^{4}\cos(\alpha_k)} \quad (13)$$

Thus, using distortion minimization PWM, four angles can be calculated, for which the THD is minimized. Therefore now the problem is about minimization of a function subjected to a constraint, which can be solved using MATLAB.

In contrast, SHE PWM can completely eliminate a number of harmonics in the output waveform, which is equal to one less than the switching angles per quarter cycle of the voltage output [8]. Therefore in this case, three harmonics can be completely eliminated.

Since only odd harmonics are present and it is the lowest harmonics that contribute most for the Total Harmonic Distortion (THD), 3rd, 5th and 7th harmonics have been eliminated. Simplifying equation (06) followed by the substitution of zeros to the magnitudes of the harmonics to be eliminated, following set of equations are obtained.

$$0 = \cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3) + \cos(3\alpha_4) \quad (14)$$

$$0 = \cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) \quad (15)$$

$$0 = \cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) \quad (16)$$

For each modulation index, there are four unknowns and four non-linear equations. Thus switching angles corresponding to a given modulation index can be found.

As the modulation index is increased in SHE PWM, the first switching point of the waveform tends to lose from the picture. As a result THD tends to increase. Therefore with SHE PWM, it is not desirable to move into higher modulation indices.

In contrast, with distortion minimization PWM, it is possible to operate at higher modulation indices such as 0.90, with comparatively low THD values like 11.74% (before filtering). Therefore it can be stated that with distortion minimization PWM, higher voltage utilization is possible for multilevel inverters.
And also for a given modulation index, the response obtained by distortion minimization is always better than that of SHE PWM, in terms of THD. In SHE PWM, when a certain number of first most significant harmonics are completely eliminated, the next significant harmonics tend to boost.

Therefore distortion minimization, which is comparatively good in harmonic suppression and in voltage utilization, is implemented in the proposed inverter.

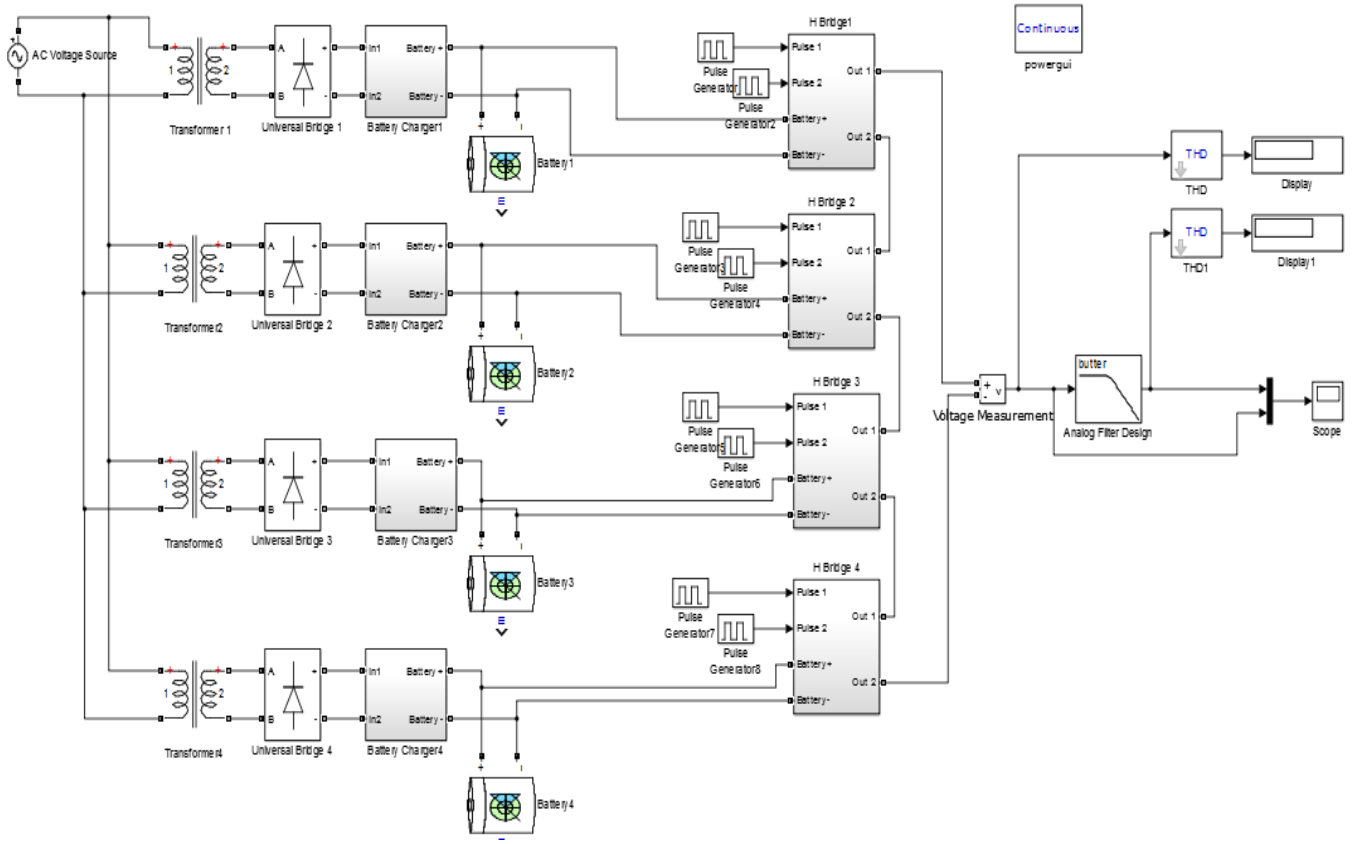

Fig. 4. MATLAB Simulink model

TABLE I. RESULTS FOR EACH MODULATION INDEX, THROUGH DISTORTION MINIMIZATION PWM

m	switching angels in degrees				THD%
	α_1	α_2	α_3	α_4	
0.84	8.2147	25.128	45.417	87.59793	12.01
0.85	8.0968	24.66	45.607	85.87338	11.86
0.86	8.2411	25.038	45.835	83.72189	11.99
0.87	8.2055	24.866	44.656	82.8307	12.04
0.88	8.0904	24.626	45.447	80.56414	12
0.89	8.0778	24.561	45.197	78.94443	11.93
0.9	8.1876	24.787	44.260	77.66770	11.74
0.91	8.2081	24.829	43.257	76.51152	11.54
0.92	8.1288	24.587	42.896	75.02459	11.32

TABLE II. RESULTS FOR EACH MODULATION INDEX THROUGH SHE PWM

m	switching angels in degrees				THD%
	α_1	α_2	α_3	α_4	
0.83	8.3916	26.9190	49.2507	85.76591	12.31
0.84	7.0621	27.4298	47.8687	84.94466	12.58
0.85	5.2538	28.1201	46.3875	84.09859	13.13
0.86	2.0330	29.0198	44.7651	83.22630	14.64
0.87	0	29.088	43.6784	82.17859	15.65
0.88	0	28.8939	42.8977	80.99525	15.57

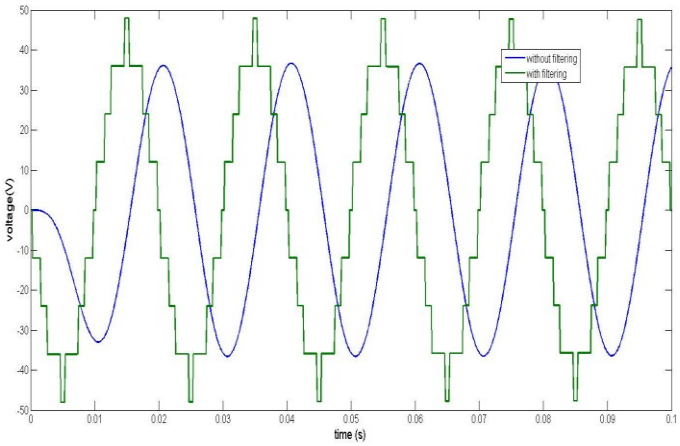

Fig. 5. Output waveform for modulation index of 0.85

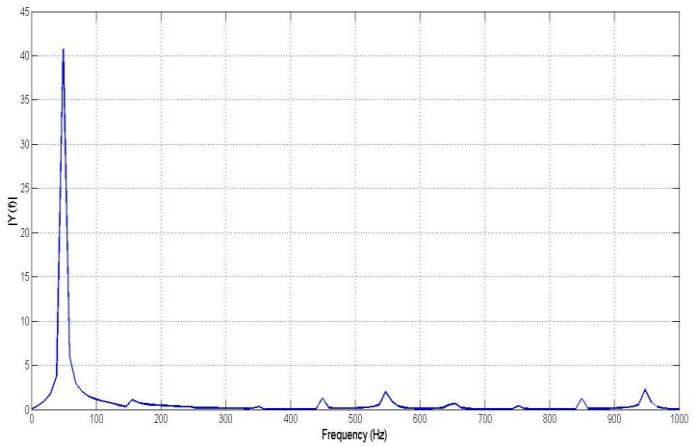

Fig. 6. Frequency spectrum (for m= 0.85), with distortion minimization PWM

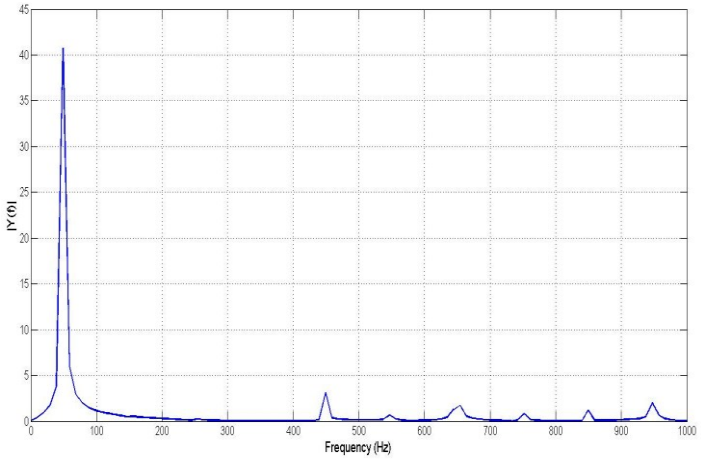

Fig. 7. Frequency spectrum (for m= 0.85), with SHE PWM

TABLE III. RESULTS OF DISTORTION MINIMIZATION PWM BEFORE AND AFTER FILTERING

m	THD%	
	Before filtering	*After filtering*
0.84	12.01	4.57
0.85	11.86	3.27
0.86	11.99	2.41
0.87	12.04	3.2
0.88	12	3.71
0.89	11.93	4.39
0.9	11.74	4.85
0.91	12.01	4.57
0.92	11.86	3.27

III. OPERATING MECHANISM OF THE UPS

As stated earlier, the proposed nine-level Cascaded H-Bridge (CHB) Multi-Level Inverter is incorporated in a UPS application. One key aspect of this UPS is "offline synchronization; an approach to achieve a good transient performance while ensuring reduced cost, size and weight".

Instead of using the conventional offline technology, here an advanced approach is introduced. Under normal conditions, the load is powered by the mains supply bypassing the inverter. Meanwhile, the batteries get charged, and most importantly, the inverter remains synchronized with the utility supply, producing the voltage waveform, yet disconnected from the load by means of a static switch.

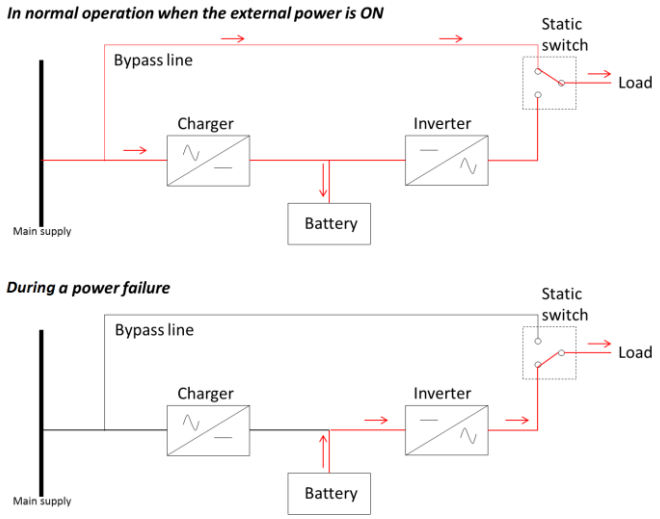

Fig. 8. Two main operation modes

At the failure of the mains supply, the static switch operates to connect the inverter output to the load. Thereafter, the load is powered by the inverter (from battery inputs).

The transition time from the mains supply to the batteries is comparatively lesser than that of a conventional offline UPS since the inverter stays always powered up and synchronized with the mains supply. Therefore, the transition time is simply the time taken for the operation of the static switch. Moreover, the surges encountered during this transition too are minimal as the inverter starts supplying the load at the same point on the voltage waveform, at the occurrence of the utility supply failure.

Due to the introduction of this simple change, the proposed UPS ensures an advanced performance, while enjoying all the advantages of a conventional offline UPS such as reduced cost, weight and size [11].

IV. SMART BATTERY CHARGER

Proper charging mechanism for the batteries plays a vital part in this design, as a symmetrical source inverter is considered. The specialty of the battery charging unit embedded in the proposed UPS is that it has two modes of operation, designed to ensure proper functionality of the batteries for a prolonged period. At a given moment, the charger operates in one of the following two modes [12].

- Current regulated mode
- Voltage regulated mode

If a fully discharged battery is connected across a constant voltage source, it tends to draw an excessive current, which would harm the battery. The commonly accepted convention for the healthy operation is that the maximum charging current must be limited to one tenth of the Ampere-hour rating of the battery, in Amperes. Therefore, the effective voltage applied across the battery is continually adjusted (increased gradually) to ensure that the charging current limit is not exceeded. This is called the current regulated mode of operation [13].

Charging under the current regulated mode, the applied voltage across the battery keeps on increasing. As it tends to reach the limiting voltage, which is slightly greater (about 1-2V) than the voltage rating of the battery, the voltage regulated mode takes over. Under this mode, the main consideration is to maintain the charging voltage within a range, of which the ceiling value is defined by the limiting voltage. This continues until the battery gets fully charged.

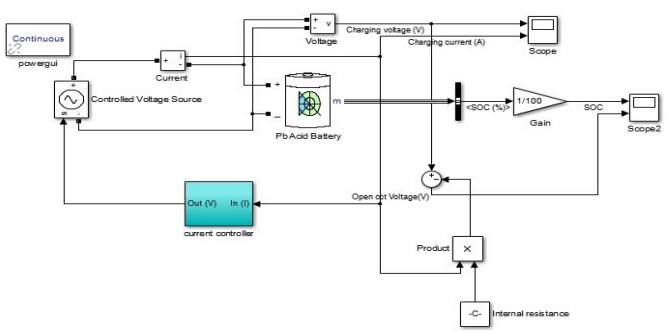

Fig. 9. MATLAB Simulink model for the battery charging circuit

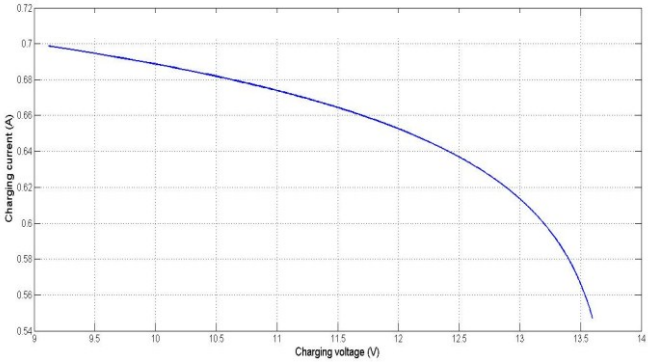

Fig. 10. Variation of charging current with voltage

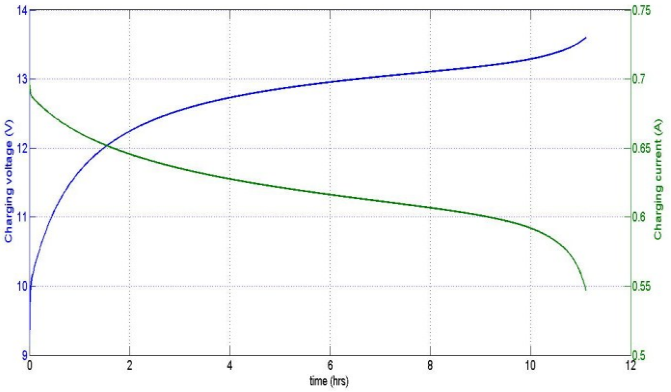

Fig. 11. Variation of charging voltage and current with time, for a battery with an initial charge of 10%

Once the battery is fully charged, in order to maintain its fully charged condition, the charger continues to supply the limiting voltage. This mode of operation is commonly termed as trickle charging mode.

V. PRACTICAL IMPLEMENTATION

In order to provide control signals, a control circuit (main control circuit) consisting of ATmega 2560 microcontroller is used. Four gate drive circuits have been used in between the main control circuit and the H bridges. As gate-drive ICs (IR2110) used are half bridge drivers, each H bridge needs a pair of those. Furthermore, high speed optocouplers are embedded in these circuits to provide isolation between the main control circuit and the H bridges.

RC type snubbers are used in the H bridge circuits to suppress the voltage surges. In order to eliminate the probability of shoot through of H bridges, a dead band circuit is implemented, of which the theory of operation lies in the time delay of an RC circuit. The charging units are realized by means of the adjustable regulator ICs (LM338) to achieve the functionality described above.

The output of the CHB inverter is sent through a Butterworth, low pass, L –C –L filter of order 3 having the cut off frequency of 350Hz before stepping up using a transformer to obtain 230V, 6A output.

Fig. 12. Practical implementation of the inverter

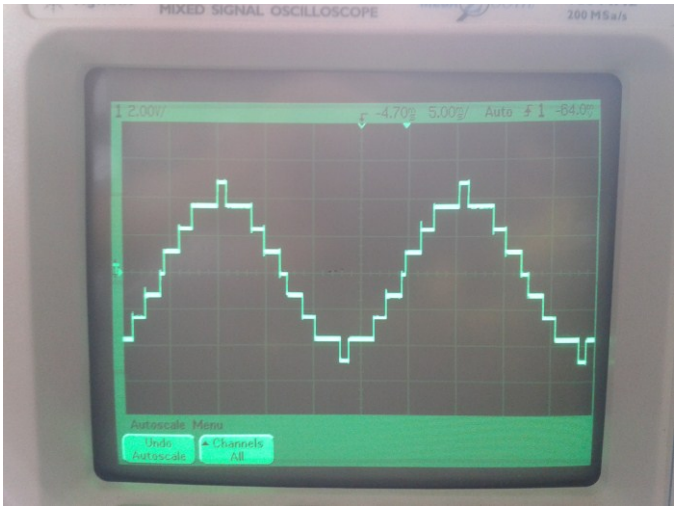

Fig. 13. Oscilloscope output of the nine-level inverter

VI. CONCLUSION

In this paper, the design of a nine-level Cascaded H-Bridge (CHB) Multi-Level Inverter is presented. Here the use of Distortion Minimization PWM for this particular inverter design is justified, based on a comparison between Distortion Minimization PWM and Selective Harmonic Elimination PWM in suppressing the harmonic content.

Despite many of the researches related to CHB inverters being made in the high power end, here the successful implementation of this technology in a low power application is presented by incorporating the proposed inverter in a low power UPS application. This UPS is intended to replace four separate conventional UPSs designed to serve four typical personal computers. Therefore, the use of four separate DC sources is justified, giving rise to a nine level inverter output waveform.

Instead of using the typical offline UPS technology, here a novel approach called Offline Synchronization is introduced to improve the UPS performance, by means of a simple, yet innovative change to the prevailing offline technology.

Considering both simulation results as well the results obtained through real world implementation, it can be concluded that a nine-level Cascaded H Bridge Inverter realized via Distortion Minimization PWM, when incorporated in an Offline Synchronized UPS, results in a high performing UPS application.

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