Department of Electronic and Telecommunication Engineering

University of Moratuwa

EN3021 – Digital System Design

RISC-V Pipelined Processor

Report

Team Leftovers

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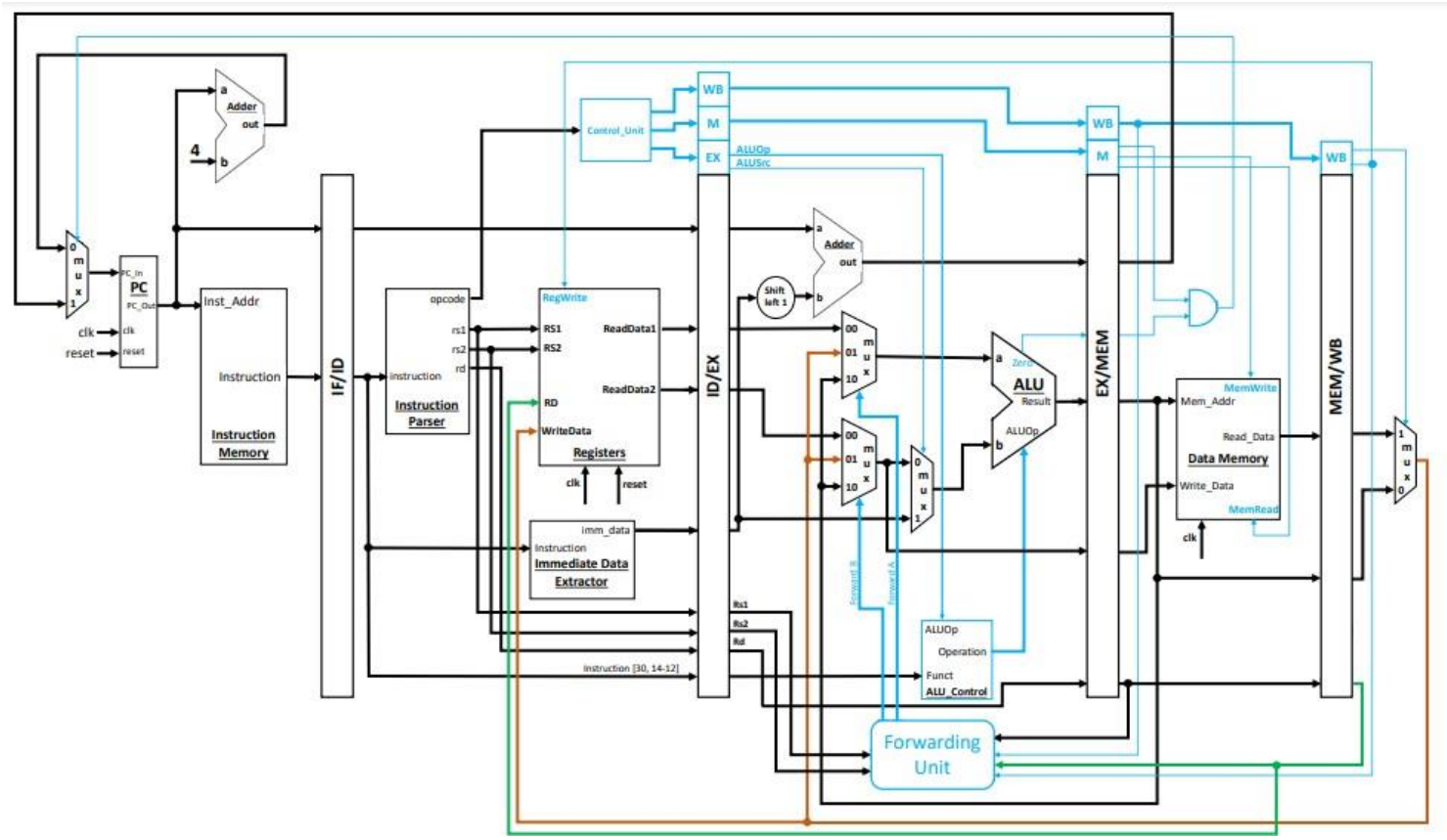
31st of December 2023

Design

This is an extension to the non-pipelined RISC V processor that was designed for the individual project. Here, we have designed a 5-stage pipelined RISC V processor with basic support against data and control hazards.

Given below is a diagram with the proposed microarchitecture.



Design decisions

Hazard detection unit

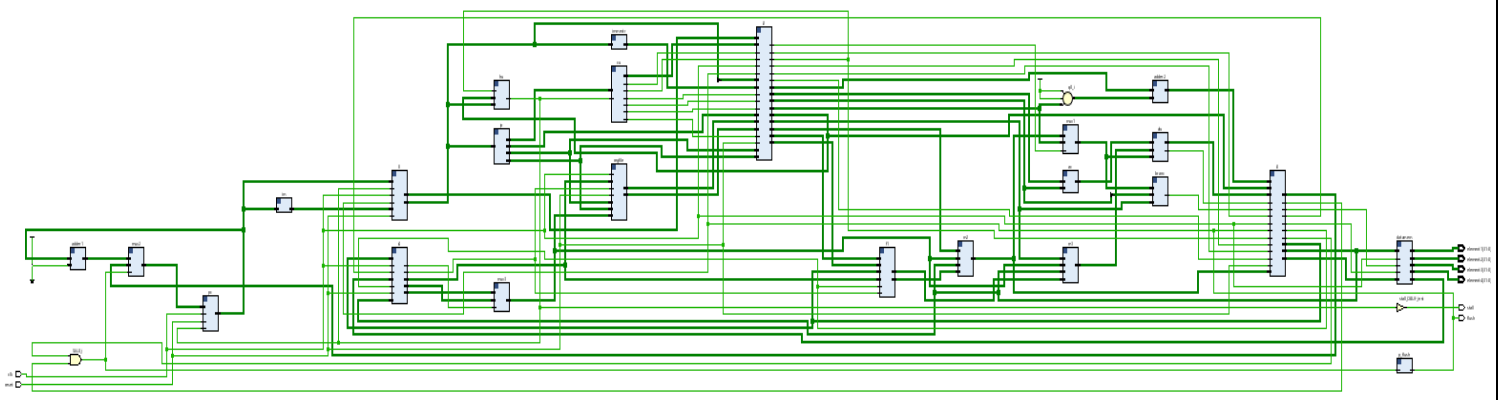
To prevent true data dependencies that occur during RAW, we have implemented control logic for data forwarding.
However, since stalling cannot be completely eliminated, we have implemented control logic for stalling as well.

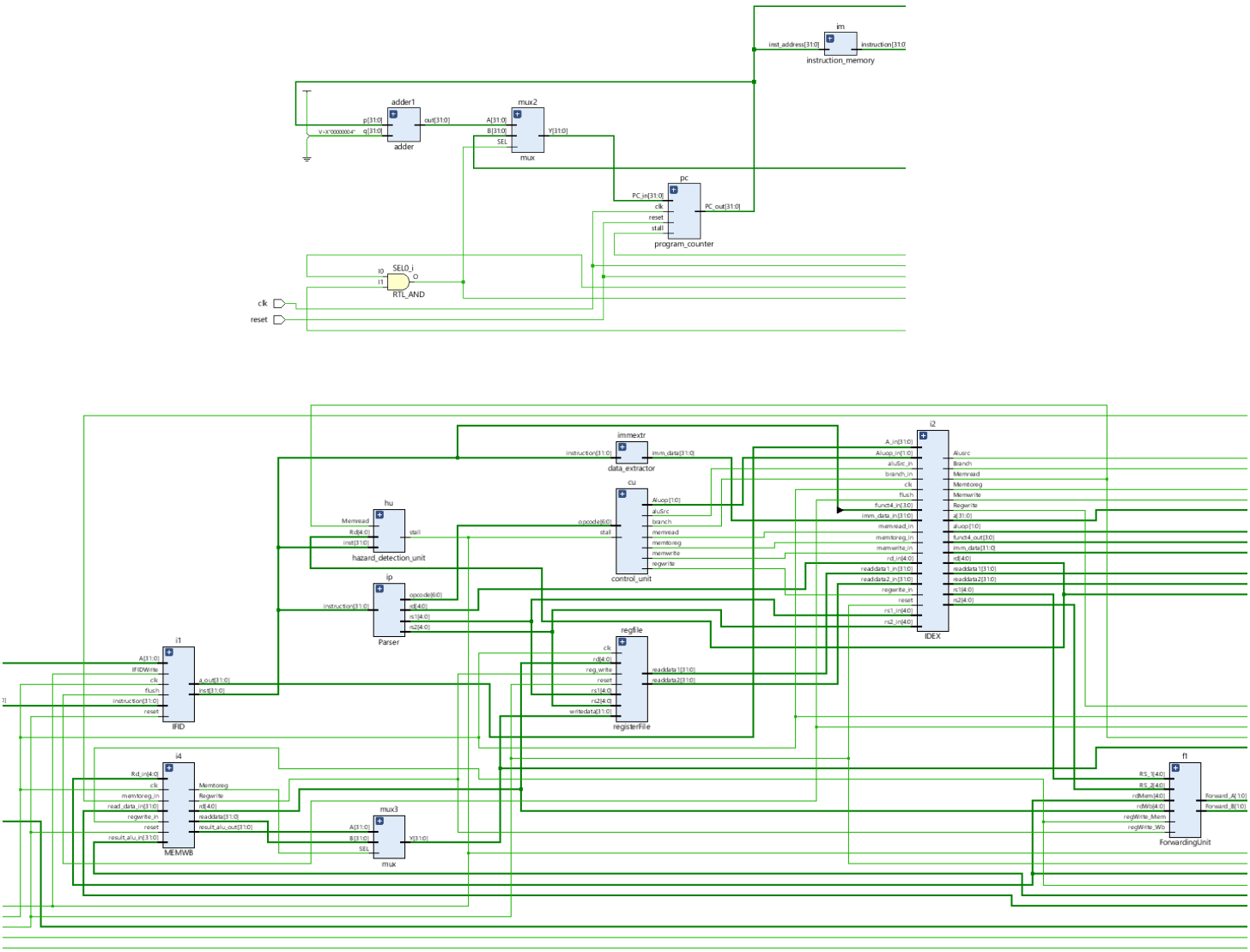
Branch Prediction

Initially, we tried using a 2-bit branch predictor, but we could not successfully integrate it with the rest of the design. Therefore, we have used static branch prediction, and we assume branches will not be taken. We have implemented flush control logic to flush the pipeline in the case of a taken branch.

Implementation

Netlist




im
inst_address[31:0]
instruction[31:0]
instruction_memory
adder1
p[31:0]
q[31:0]
out[31:0]
adder
mux2
A[31:0]
B[31:0]
SEL
Y[31:0]
mux
pc
PC_in[31:0]
clk
reset
stall
PC_out[31:0]
program_counter
SEL0_i
I0
I1
O
RTL_AND
clk
reset
immextr
instruction[31:0]
imm_data[31:0]
data_extractor
cu
opcode[6:0]
stall
ALuop[1:0]
aluSrc
branch
memread
memtoreg
memwrite
regwrite
control_unit
hu
Memread
Rd[4:0]
inst[31:0]
stall
hazard_detection_unit
ip
opcode[6:0]
rd[4:0]
rs1[4:0]
rs2[4:0]
Parser
i2
A_in[31:0]
ALuop_in[1:0]
aluSrc_in
branch_in
clk
flush
funct4_in[3:0]
imm_data_in[31:0]
memread_in
memtoreg_in
memwrite_in
rd_in[4:0]
readdata1_in[31:0]
readdata2_in[31:0]
regwrite_in
reset
rs1_in[4:0]
rs2_in[4:0]
Alusrc
Branch
Memread
Memtoreg
Memwrite
Regwrite
a[31:0]
aluop[1:0]
funct4_out[3:0]
imm_data[31:0]
rd[4:0]
readdata1[31:0]
readdata2[31:0]
rs1[4:0]
rs2[4:0]
IDEX
i1
A[31:0]
IFIDWrite
clk
flush
instruction[31:0]
reset
o_out[31:0]
ins[31:0]
IFID
regfile
clk
rd[4:0]
reg_write
reset
rs1[4:0]
rs2[4:0]
writedata[31:0]
readdata1[31:0]
readdata2[31:0]
registerFile
i4
Rd_in[4:0]
clk
memtoreg_in
read_data_in[31:0]
regwrite_in
reset
result_alu_in[31:0]
Memtoreg
Regwrite
rd[4:0]
readdata[31:0]
result_alu_out[31:0]
MEMWB
mux3
A[31:0]
B[31:0]
SEL
Y[31:0]
mux
f1
RS_1[4:0]
RS_2[4:0]
rdMem[4:0]
rdWb[4:0]
regWrite_Mem
regWrite_Wb
forward_A[1:0]
forward_B[1:0]
ForwardingUnit
adder2
p[31:0]
q[31:0]
out[31:0]
adder
qf0_i
I1
I2
I0[31:0]
O[31:0]
RTL_LSHIFT
mux1
A[31:0]
B[31:0]
SEL
Y[31:0]
mux
alu
ALuop[3:0]
a[31:0]
b[31:0]
Result[31:0]
zero
alu
ac
ALuop[1:0]
funct3[3:0]
operation[3:0]
alu_control
branc
b[31:0]
funct3[2:0]
readData1[31:0]
addermuxselect
branching_unit
i3
Adder_out[31:0]
Rd_in[4:0]
Result_in_alu[31:0]
Zero_in
addermuxselect_in
branch_in
clk
flush
memread_in
memtoreg_in
memwrite_in
regwrite_in
reset
writedata_in[31:0]
Addersout[31:0]
Branch
Memread
Memtoreg
Memwrite
Regwrite
addermuxselect
rd[4:0]
result_out_alu[31:0]
writedata_out[31:0]
EXMEM
m2
a[31:0]
b[31:0]
c[31:0]
sel[1:0]
out[31:0]
ThreebyOneMux
m1
a[31:0]
b[31:0]
c[31:0]
sel[1:0]
out[31:0]
ThreebyOneMux
datamem
address[31:0]
clk
memoryread
memorywrite
write_data[31:0]
element1[31:0]
element2[31:0]
element3[31:0]
element4[31:0]
read_data[31:0]
data_memory
stall_OBUF_inst
I
O
OBUF
stall
flush
p_flush
branch
flush
pipeline_flush

Resource Utilization

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	1532	0	17600	8.70
LUT as Logic	1532	0	17600	8.70
LUT as Memory	0	0	6000	0.00
Slice Registers	1742	0	35200	4.95
Register as Flip Flop	1598	0	35200	4.54
Register as Latch	144	0	35200	0.41
F7 Muxes	416	0	8800	4.73
F8 Muxes	64	0	4400	1.45

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
158	Yes	-	Reset
0	Yes	Set	-
1584	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	60	0.00
RAMB36/FIFO*	0	0	60	0.00
RAMB18	0	0	120	0.00

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	80	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	132	0	100	132.00
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	2	0.00
PHASER_REF	0	0	2	0.00
OUT_FIFO	0	0	8	0.00
IN_FIFO	0	0	8	0.00
IDELAYCTRL	0	0	2	0.00
IBUFDS	0	0	96	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	8	0.00
PHASER_IN/PHASER_IN_PHY	0	0	8	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	100	0.00
ILOGIC	0	0	100	0.00
OLOGIC	0	0	100	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	3	0	32	9.38
BUFIO	0	0	8	0.00
MMCME2_ADV	0	0	2	0.00
PLLE2_ADV	0	0	2	0.00
BUFMRCE	0	0	4	0.00
BUFHCE	0	0	48	0.00
BUFR	0	0	8	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
FDRE	1584	Flop & Latch
LUT6	1214	LUT
MUXF7	416	MuxFx
LUT5	184	LUT
LUT3	148	LUT
LDCE	144	Flop & Latch
OBUF	130	IO
LUT4	81	LUT
MUXF8	64	MuxFx
LUT2	38	LUT
CARRY4	25	CarryLogic
FDCE	14	Flop & Latch
BUFG	3	Clock
LUT1	2	LUT
IBUF	2	IO

Contribution

Gunawardena M.N. 200201V	Data Hazards (Hazard detection, Forwarding, Flushing)
Kavinda W.M.C. 200301D	Pipeline Registers (IFID, IDEX, EXMEM, MEMWB)
Kishokkumar R. 200306X	Branch Prediction