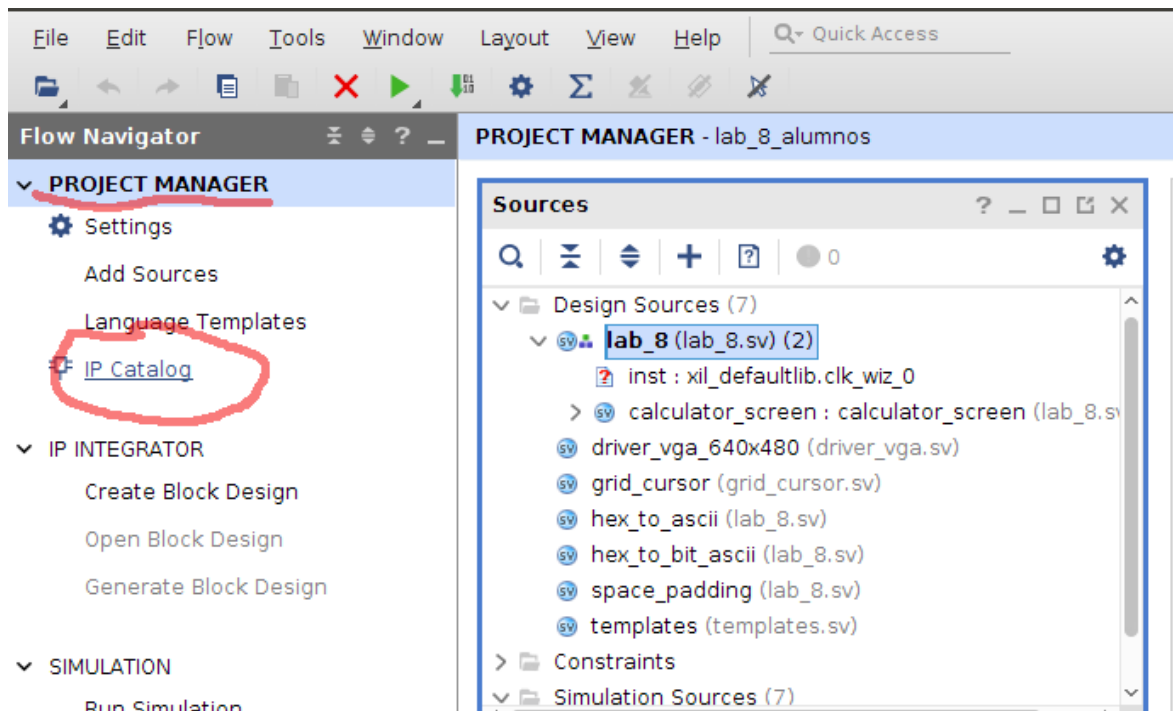
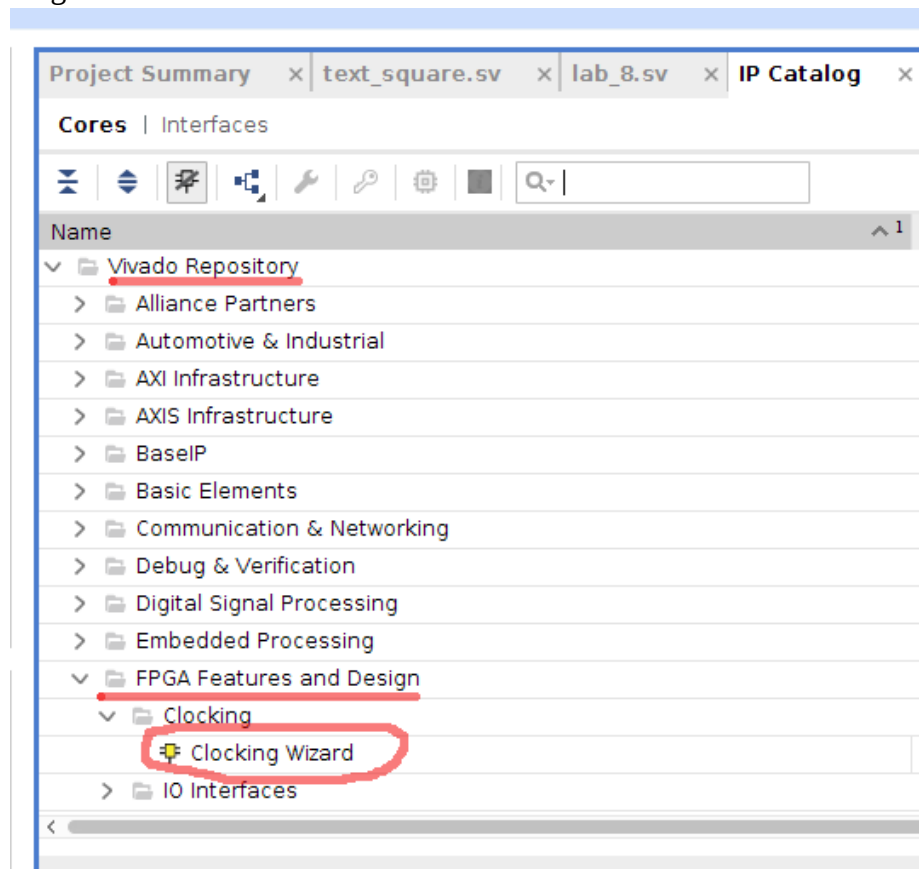


Ejemplo de configuración del DCM

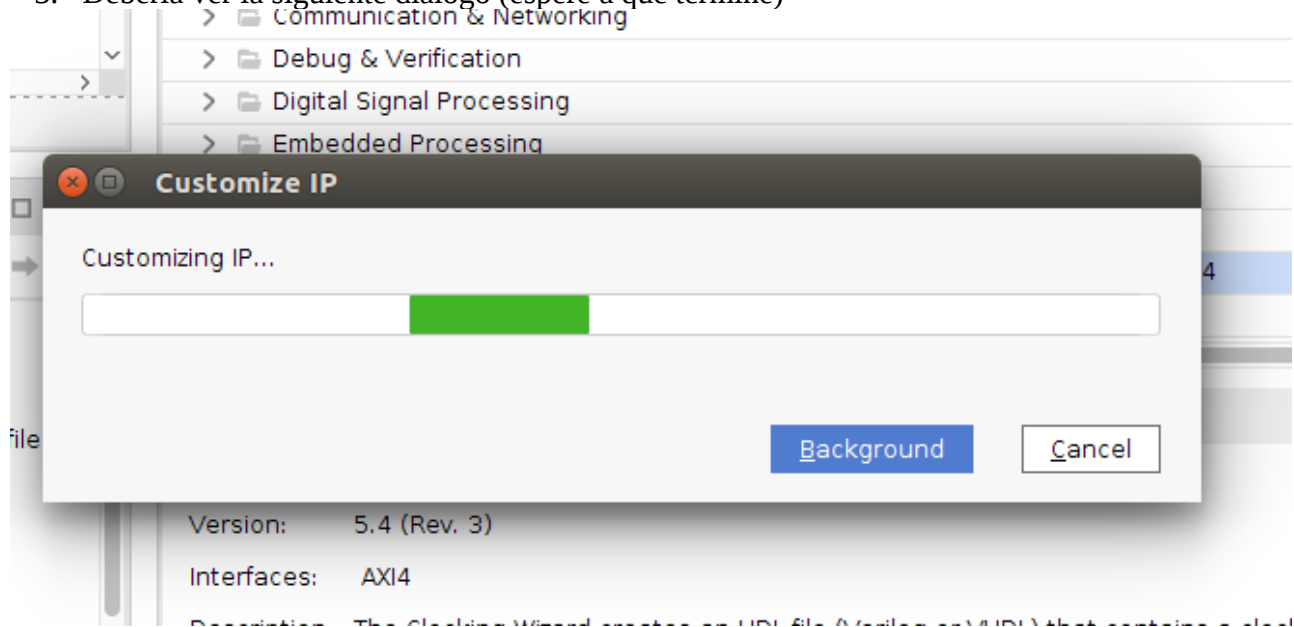
1. Para crear un nuevo IP hay que ir a la subsección IP Catalog debajo de Project Manager



2. Luego seleccionar seleccionar Vivado Respository → FPGA Features and Design → Clocking → Clocking Wizard.



3. Debería ver la siguiente diálogo (espere a que termine)



4. Ponga un nombre al módulo en la pestaña Clocking Options y deje el resto tal como estaba.

Clocking Wizard (5.4)

Documentation IP Location Switch to Defaults

Component Name clk_wiz_0 Poner un nombre

Clocking Options Output Clocks Port Renaming MMCM Settings Summary

Clock Monitor

☐ Enable Clock Monitoring

Primitive

☒ MMCM ☐ PLL

Clocking Features

☒ Frequency Synthesis ☐ Minimize Power

☒ Phase Alignment ☐ Spread Spectrum

☐ Dynamic Reconfig ☐ Dynamic Phase Shift

☐ Safe Clock Startup

Jitter Optimization

☒ Balanced ☐ Minimize Output Jitter ☐ Maximize Input Jitter filtering

Dynamic Reconfig Interface Options

☒ AXI4Lite ☐ DRP ☐ Phase Duty Cycle Config ☐ Write DRP registers

Input Clock Information

Input Clock	Port Name	Input Frequency(MHz)	Jitter Options	Input Jitter	Source
<input checked="" type="checkbox"/> Primary	clk_in1	100.000	10.000 - 800.000	0.010	Single ended clock ca
<input type="checkbox"/> Secondary	clk_in2	100.000	60.000 - 120.000	0.010	Single ended clock ca

IP Symbol Resource

☒ Show disabled ports

+ s_axi_lite
 + CLK_IN1_D
 + CLK_IN2_D
 + CLKFB_IN_D
 s_axi_aclk
 s_axi_aresetn
 reset
 resetn
 ref_clk
 user_clk0
 user_clk1
 user_clk2
 user_clk3
 clk_in1

CLKFB_OUT_D
 clk_stop[3:0]
 clk_glitch[3:0]
 interrupt
 clk_oor[3:0]
 clk_out1
 locked

- ### Clocking Wizard (5.4)



Documentation
IP Location
Switch to Defaults

IP Symbol Resource

☒ Show disabled ports

Component Name clk_wiz_0

Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary

The phase is calculated relative to the active input clock.

Output Clock	Port Name	Output Freq (MHz)		Phase (degrees)		Duty Cycle (%)	
		Requested	Actual	Requested	Actual	Requested	Actual
<input checked="" type="checkbox"/> clk_out1	clk_out1	100.000	100.000	0.000	0.000	50.000	50.000
<input type="checkbox"/> clk_out2	clk_out2	100.000	N/A	0.000	N/A	50.000	N/A
<input type="checkbox"/> clk_out3	clk_out3	100.000	N/A	0.000	N/A	50.000	N/A
<input type="checkbox"/> clk_out4	clk_out4	100.000	N/A	0.000	N/A	50.000	N/A
<input type="checkbox"/> clk_out5	clk_out5	100.000	N/A	0.000	N/A	50.000	N/A
<input type="checkbox"/> clk_out6	clk_out6	100.000	N/A	0.000	N/A	50.000	N/A
<input type="checkbox"/> clk_out7	clk_out7	100.000	N/A	0.000	N/A	50.000	N/A

☐ USE CLOCK SEQUENCING

Output Clock	Sequence Number
clk_out1	1
clk_out2	1
clk_out3	1
clk_out4	1
clk_out5	1
clk_out6	1
clk_out7	1

Clocking Feedback

Source

☒ Automatic Control On-Chip

☐ Automatic Control Off-Chip

☐ User-Controlled On-Chip

☐ User-Controlled Off-Chip

Signaling

☒ Single-ended

☐ Differential

CLKFB_OUT_D

clk_stop[3:0]

clk_glitch[3:0]

interrupt

clk_oor[3:0]

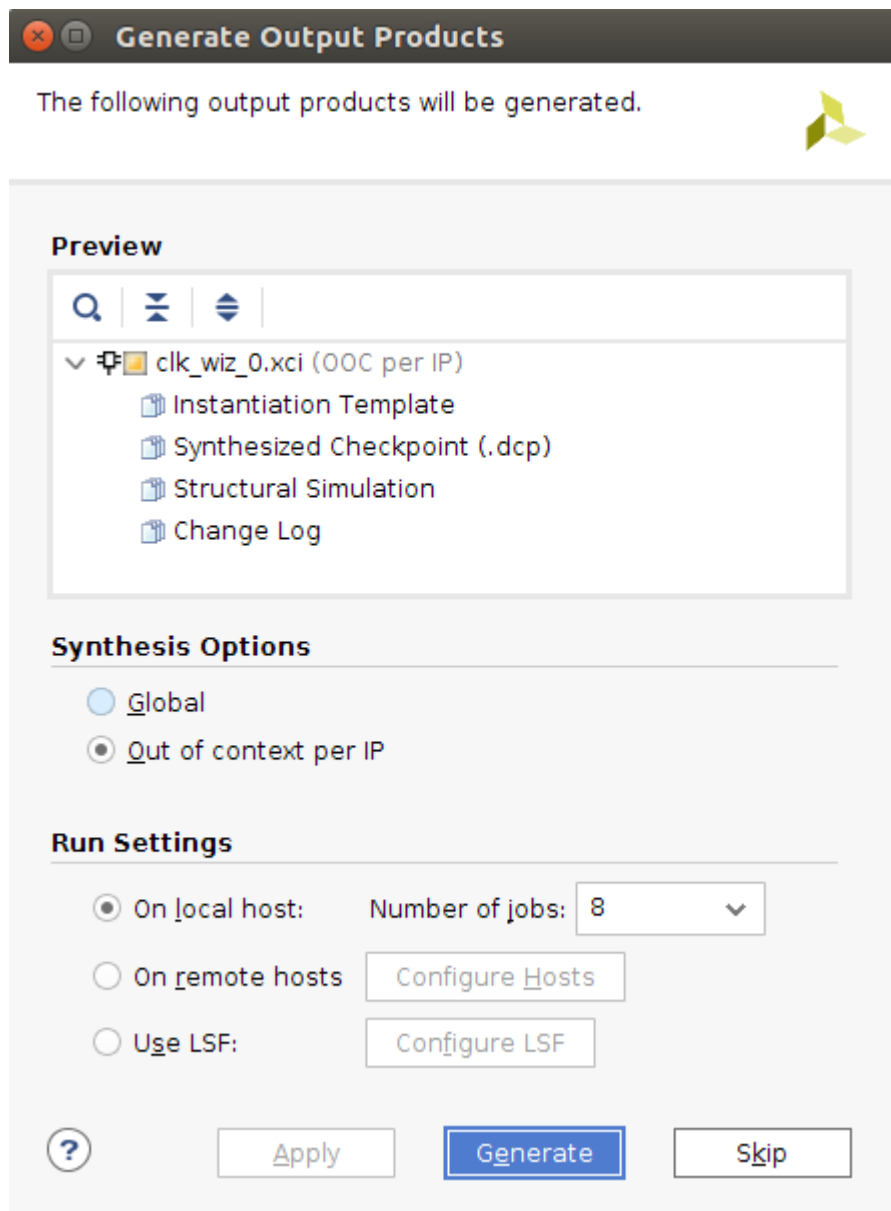
locked

Enable Optional Inputs / Outputs for MMCM/PLL

☒ reset
 ☐ power_down
 ☐ input_clk_stopped
 ☒ Active High
 ☐ Active Low

☒ locked
 ☐ clkfbstopped

6. Luego aparecerá un diálogo de confirmación para crear el módulo. Presione Generate.



7. Una vez que se termine de crear el IP, hay que ver la manera en que se instancia, para ello expanda el módulo como se muestra en la figura. Lo que está de color morado es la instancia del módulo. Puede utilizar dicho código para crear la instancia.

The screenshot displays a Verilog IDE interface with three main panels:

- Sources Panel:** Shows a project hierarchy under 'Design Sources (8)'. The 'lab_8' directory is expanded, showing sub-modules like 'calculator_screen', 'clk_wiz_0', 'driver_vga_640x480', 'grid_cursor', 'hex_to_ascii', 'hex_to_bit_ascii', 'space_padding', and 'templates'. The 'clk_wiz_0' module is selected and highlighted in blue.
- Source File Properties Panel:** Displays properties for the selected file 'clk_wiz_0.v'. It shows the file is 'Enabled', its location is '/home/mauricio/Ramos/Elo212/2018/Laboratorios/lab_8', its type is 'Verilog', its library is 'xilinx_defaultlib', its size is '3.9 KB', and it was modified 'Today at 22:29:12 PM'.
- Code Editor:** Shows the Verilog code for the 'clk_wiz_0' module. The code includes comments for clock parameters and a module instantiation. The instantiation code is highlighted in blue:

```
58 //-----
59 // clk_out1____82.000____0.000____50.0_
60 //
61 //-----
62 // Input Clock   Freq (MHz)   Input Jitter
63 //-----
64 // __primary____100.000____0.0_
65
66 `timescale 1ps/1ps
67
68 (* CORE_GENERATION_INFO = "clk_wiz_0,clk_wiz_0" *)
69
70 module clk_wiz_0
71 (
72     // Clock out ports
73     output        clk_out1,
74     // Status and control signals
75     input         reset,
76     output        locked,
77     // Clock in ports
78     input         clk_in1
79 );
80
81 clk_wiz_0_clk_wiz inst
82 (
83     // Clock out ports
84     .clk_out1(clk_out1),
85     // Status and control signals
86     .reset(reset),
87     .locked(locked),
88     // Clock in ports
89     .clk_in1(clk_in1)
90 );
91
92 endmodule
```