Microprocessor and Computer Architecture

UE24CS251B

4th Semester, Academic Year 2025-26

Date:

Name: Harshit Chandak	SRN:PES2UG24CS185	Section C

LAB #____2_____ Program Number: ____1___

Title of the Program

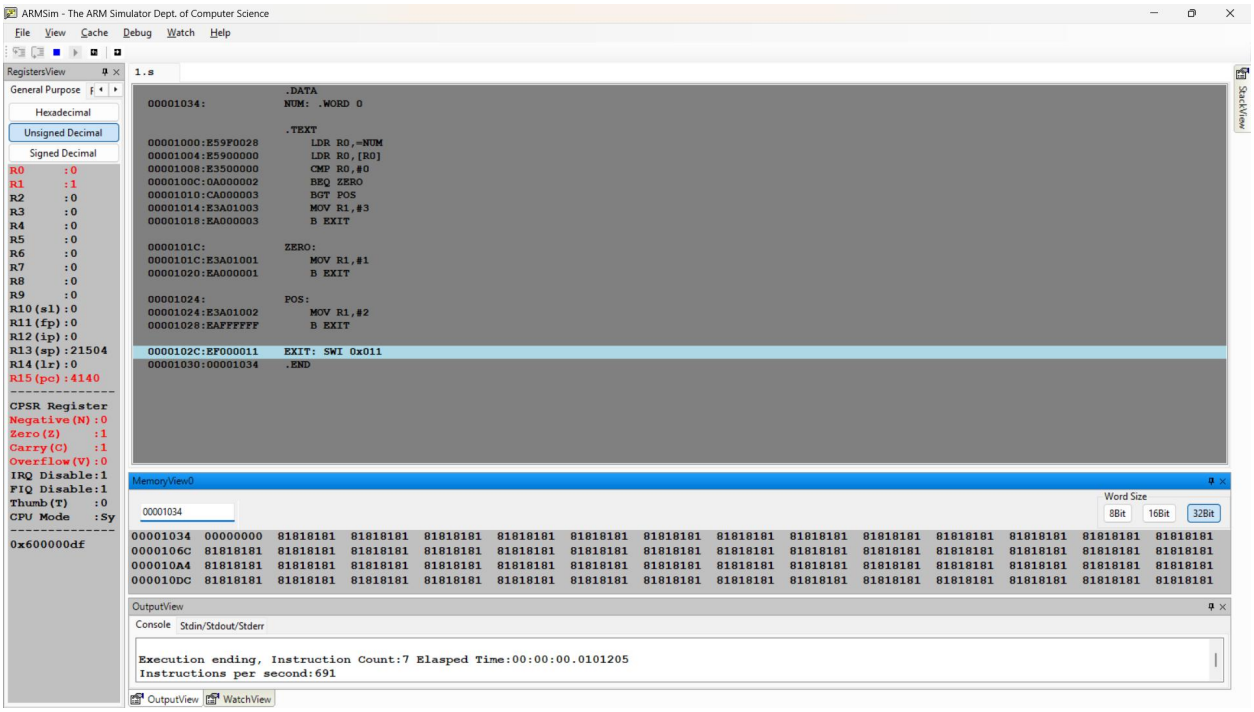
Based on value of number in r0,

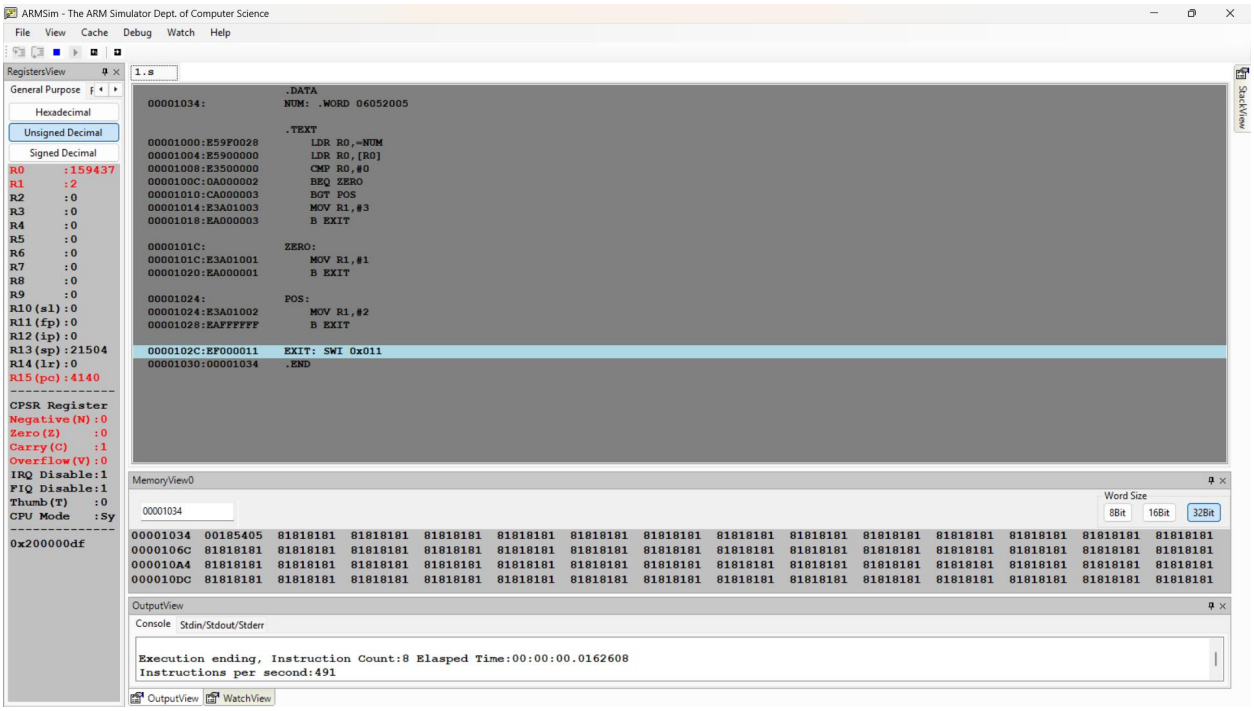
i. store 1 in r1 if r0 is 0
ii. store 2 in r1 if r0 is positive
iii. store 3 if r0 is negative

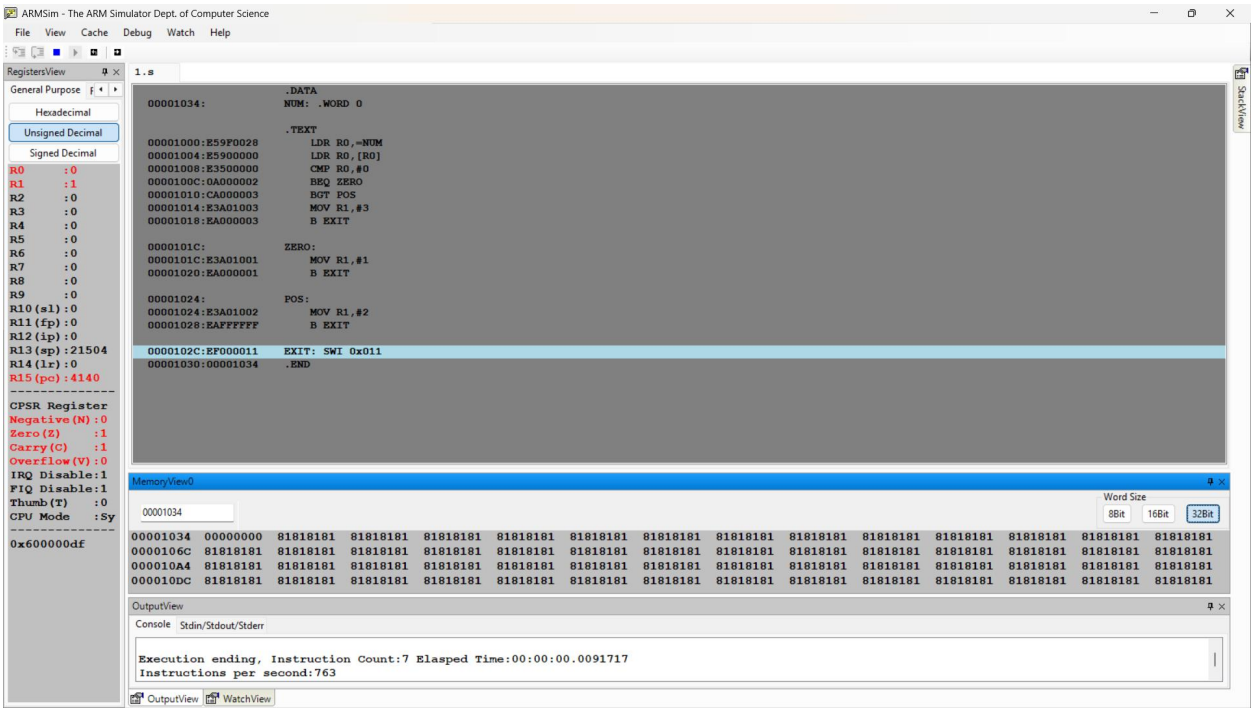
I. Typed ARM Assembly Code
II. Three Output Screen Shots (one for each case)
(Screenshot including Register Window,Output Window and Code Window)

```
.DATA

NUM: .WORD 0


.TEXT
```

```
    LDR R0,=NUM
    LDR R0,[R0]
    CMP R0,#0
    BEQ ZERO
    BGT POS
    MOV R1,#3
    B EXIT

ZERO:
    MOV R1,#1
    B EXIT

POS:
    MOV R1,#2
    B EXIT

EXIT: SWI 0x011
.END
```


ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :0
R1 :1
R2 :0
R3 :0
R4 :0
R5 :0
R6 :0
R7 :0
R8 :0
R9 :0
R10(sl):0
R11(fp):0
R12(ip):0
R13(sp):21504
R14(lr):0
R15(pc):4140
CPSR Register
Negative(N):0
Zero(Z) :1
Carry(C) :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :Sy
0x600000df
1.s
00001034: .DATA
NUM: .WORD 0
.TEXT
00001000:E59F0028 LDR R0,=NUM
00001004:E5900000 LDR R0,[R0]
00001008:E3500000 CMP R0,#0
0000100C:0A000002 BEQ ZERO
00001010:CA000003 BGT POS
00001014:E3A01003 MOV R1,#3
00001018:EA000003 B EXIT
0000101C: ZERO:
0000101C:E3A01001 MOV R1,#1
00001020:EA000001 B EXIT
00001024: POS:
00001024:E3A01002 MOV R1,#2
00001028:EAFFFFFF B EXIT
0000102C:EF000011 EXIT: SWI 0x011
00001030:00001034 .END
MemoryView0
00001034
Word Size
8Bit 16Bit 32Bit
00001034 00000000 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
0000106C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000010A4 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000010DC 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
OutputView
Console Stdin/Stdout/Stderr
Execution ending, Instruction Count:7 Elasped Time:00:00:00.0101205
Instructions per second:691
OutputView WatchView
StackView


ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :159437
R1 :2
R2 :0
R3 :0
R4 :0
R5 :0
R6 :0
R7 :0
R8 :0
R9 :0
R10(sl):0
R11(fp):0
R12(ip):0
R13(sp):21504
R14(lr):0
R15(pc):4140
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :Sy
0x200000df
1.s
00001034: .DATA
NUM: .WORD 06052005
.TEXT
00001000:E59F0028 LDR R0,=NUM
00001004:E5900000 LDR R0,[R0]
00001008:E3500000 CMP R0,#0
0000100C:0A000002 BEQ ZERO
00001010:CA000003 BGT POS
00001014:E3A01003 MOV R1,#3
00001018:EA000003 B EXIT
0000101C: ZERO:
0000101C:E3A01001 MOV R1,#1
00001020:EA000001 B EXIT
00001024: POS:
00001024:E3A01002 MOV R1,#2
00001028:EAFFFFFF B EXIT
0000102C:EF000011 EXIT: SWI 0x011
00001030:00001034 .END
MemoryView0
00001034
Word Size
8Bit 16Bit 32Bit
00001034 00185405 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
0000106C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000010A4 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000010DC 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
OutputView
Console Stdin/Stdout/Stderr
Execution ending, Instruction Count:8 Elasped Time:00:00:00.0162608
Instructions per second:491
OutputView WatchView
StackView



Microprocessor and Computer Architecture

UE24CS251B

4th Semester, Academic Year 2025-26

Date:

Name: Harshit Chandak	SRN: PES2UG24CS185	Section C

LAB #____2_____ Program Number: ____2___

Title of the Program

Write an ARM program that generates 75 × R0 using shift and add/subtract operations (no MUL instruction).

I. ARM Assembly Code

II. Output Screen Shots

(One Screenshot including Register Window,Output Window and Code Window)

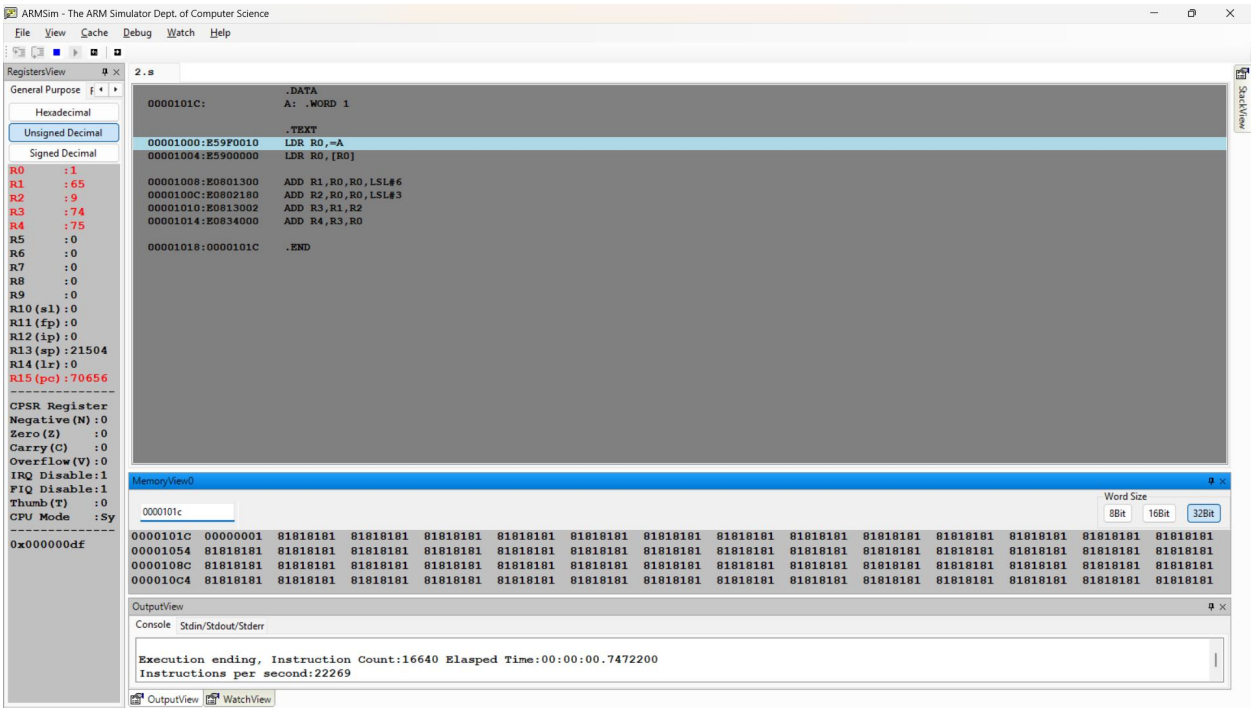
```
.DATA
A: .WORD 1


.TEXT
```

```
LDR R0,=A
LDR R0,[R0]
```

```
ADD R1,R0,R0,LSL#6
ADD R2,R0,R0,LSL#3
ADD R3,R1,R2
ADD R4,R3,R0
```

```
SWI 0x011
```

```
.END
```



Microprocessor and Computer Architecture

UE24CS251B

4th Semester, Academic Year 2025-26

Date:

Name: Harshit Chandak	SRN:PES2UG24CS185	Section C

LAB #____2_____ Program Number: ____3___

Title of the Program

To find GCD of two numbers using conditional instructions only.

I. ARM Assembly Code

II. Output Screen Shots

(One Screenshot including Register Window,Memory Window and Code Window)

```
.DATA


NUM1: .WORD 38

NUM2: .WORD 95
```

```
.TEXT
```

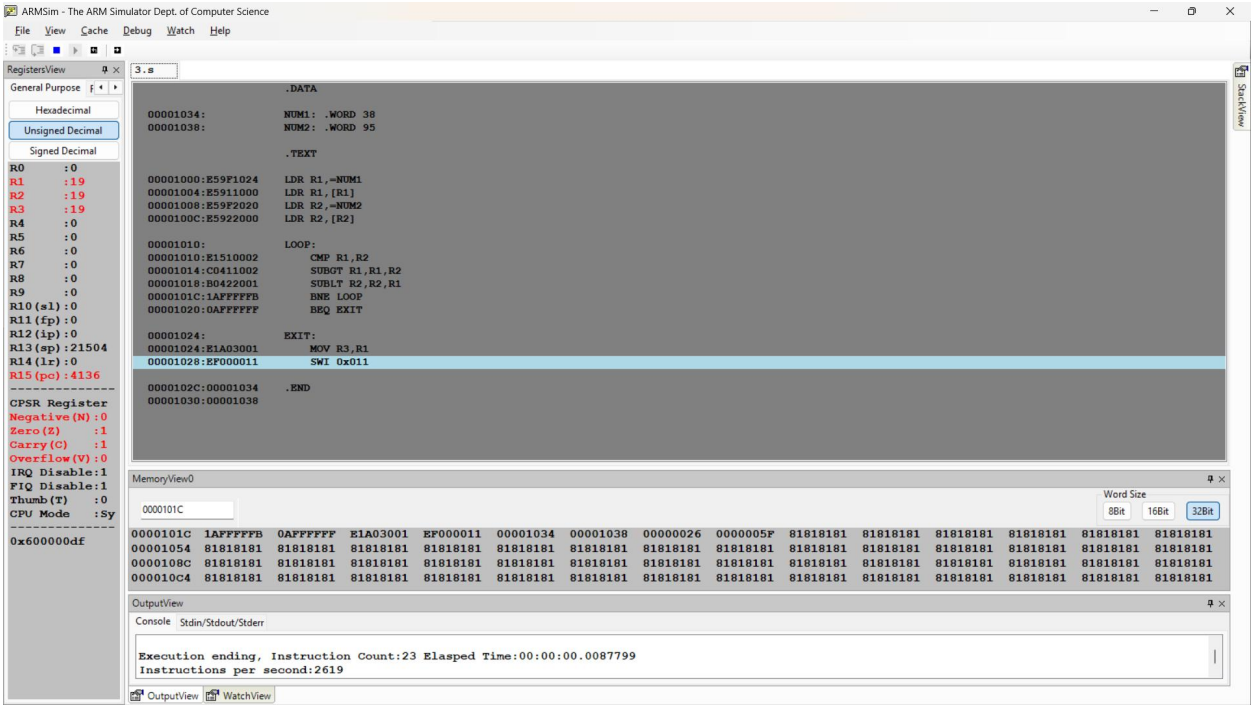
```
LDR R1,=NUM1

LDR R1,[R1]

LDR R2,=NUM2

LDR R2,[R2]
```

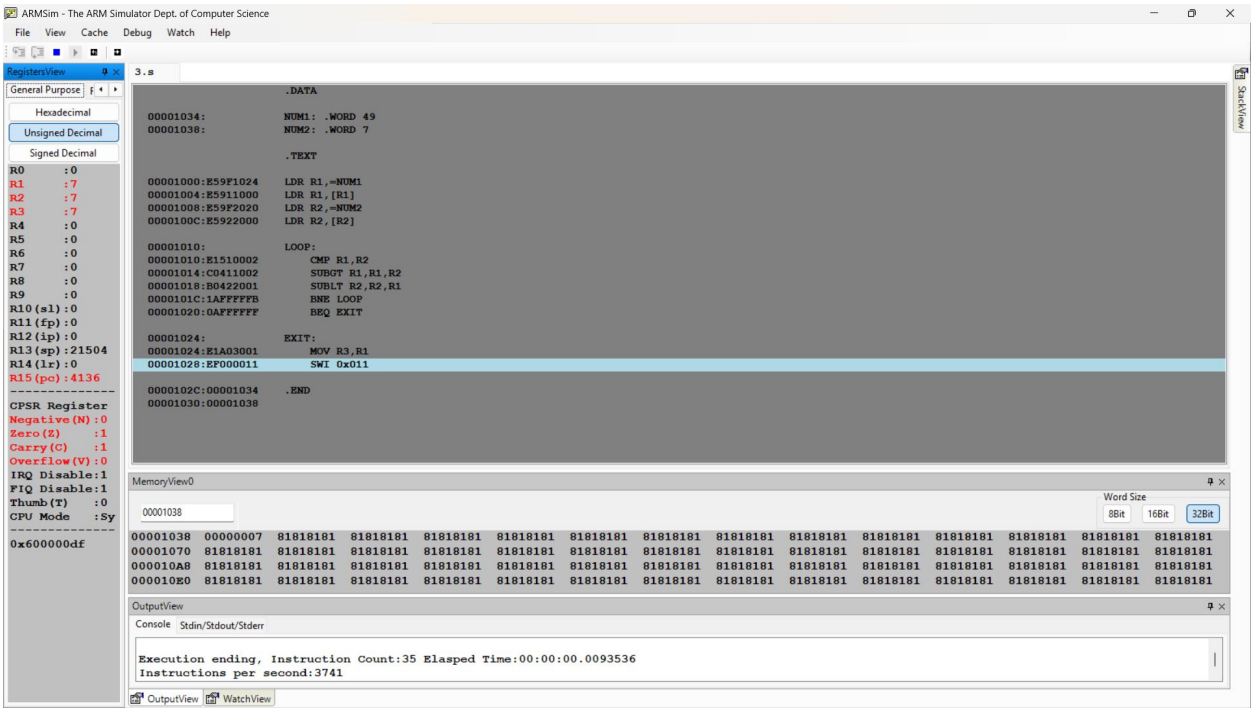
```
LOOP:

    CMP R1,R2

    SUBGT R1,R1,R2
```

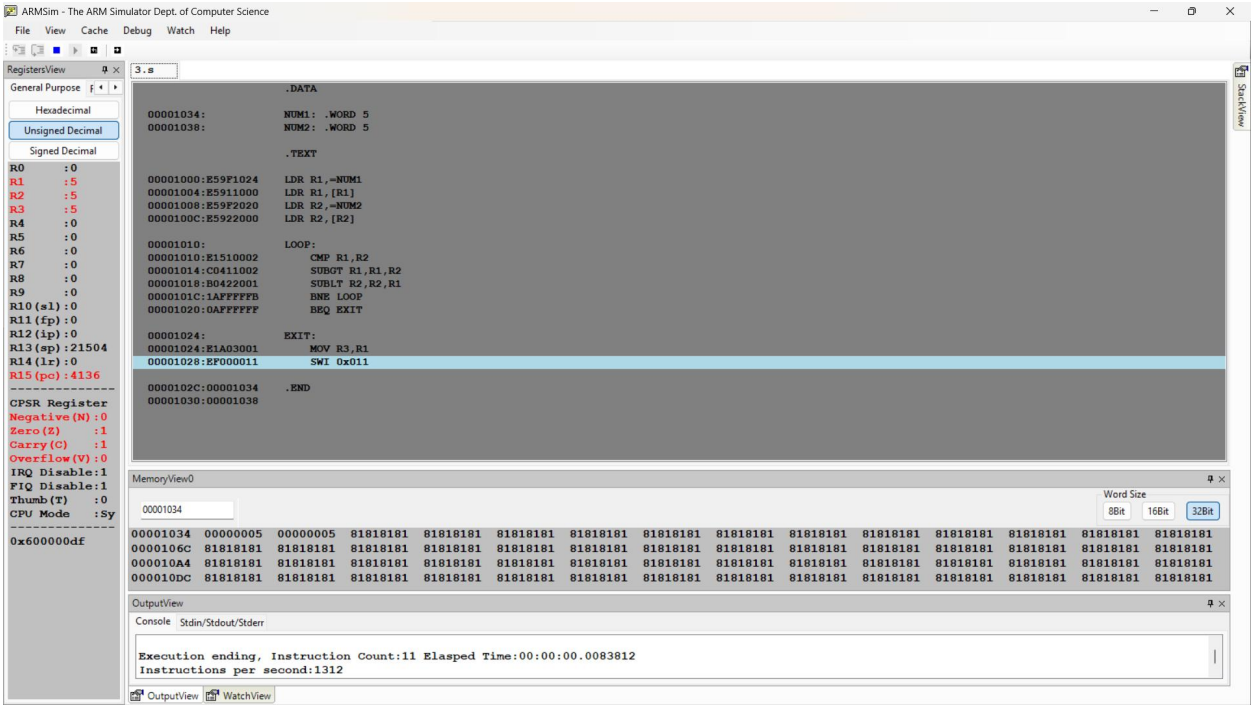
```
    SUBLT R2,R2,R1

    BNE LOOP

    BEQ EXIT
```

```
EXIT:

    MOV R3,R1

    SWI 0x011
```

```
.END
```




ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :0
R1 :7
R2 :7
R3 :7
R4 :0
R5 :0
R6 :0
R7 :0
R8 :0
R9 :0
R10(sl) :0
R11(fp) :0
R12(ip) :0
R13(sp) :21504
R14(lr) :0
R15(pc) :4136
CPSR Register
Negative(N) :0
Zero(Z) :1
Carry(C) :1
Overflow(V) :0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :Sy
0x600000df
3.s
.DATA
00001034: NUM1: .WORD 49
00001038: NUM2: .WORD 7
.TEXT
00001000:E59F1024 LDR R1,=NUM1
00001004:E5911000 LDR R1,[R1]
00001008:E59F2020 LDR R2,=NUM2
0000100C:E5922000 LDR R2,[R2]
00001010: LOOP:
00001010:E1510002 CMP R1,R2
00001014:C0411002 SUBGT R1,R1,R2
00001018:B0422001 SUBLT R2,R2,R1
0000101C:1AFFFFFB BNE LOOP
00001020:0AFFFFFF BEQ EXIT
00001024: EXIT:
00001024:E1A03001 MOV R3,R1
00001028:EF000011 SWI 0x011
0000102C:00001034 .END
00001030:00001038
MemoryView0
00001038
Word Size
8Bit 16Bit 32Bit
00001038 00000007 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
00001070 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000010A8 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000010E0 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
OutputView
Console Stdin/Stdout/Stderr
Execution ending, Instruction Count:35 Elasped Time:00:00:00.0093536
Instructions per second:3741
OutputView WatchView
StackView


ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
RegistersView
General Purpose
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :0
R1 :5
R2 :5
R3 :5
R4 :0
R5 :0
R6 :0
R7 :0
R8 :0
R9 :0
R10(sl) :0
R11(fp) :0
R12(ip) :0
R13(sp) :21504
R14(lr) :0
R15(pc) :4136
CPSR Register
Negative(N) :0
Zero(Z) :1
Carry(C) :1
Overflow(V) :0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :Sy
0x600000df
3.s
.DATA
00001034: NUM1: .WORD 5
00001038: NUM2: .WORD 5
.TEXT
00001000:E59F1024 LDR R1,=NUM1
00001004:E5911000 LDR R1,[R1]
00001008:E59F2020 LDR R2,=NUM2
0000100C:E5922000 LDR R2,[R2]
00001010: LOOP:
00001010:E1510002 CMP R1,R2
00001014:C0411002 SUBGT R1,R1,R2
00001018:B0422001 SUBLT R2,R2,R1
0000101C:1AFFFFFB BNE LOOP
00001020:0AFFFFFF BEQ EXIT
00001024: EXIT:
00001024:E1A03001 MOV R3,R1
00001028:EF000011 SWI 0x011
0000102C:00001034 .END
00001030:00001038
MemoryView0
00001034
Word Size
8Bit 16Bit 32Bit
00001034 00000005 00000005 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
0000106C 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000010A4 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
000010DC 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181 81818181
OutputView
Console Stdin/Stdout/Stderr
Execution ending, Instruction Count:11 Elasped Time:00:00:00.0083812
Instructions per second:1312
OutputView WatchView
StackView

Microprocessor and Computer Architecture

UE22CS251B

4th Semester, Academic Year 2023-24

Date:

Name: Harshit Chandak	SRN: PES2U24CS185	Section

LAB #____2_____ Program Number: ____4___

Title of the Program

Add 2 numbers from memory and store result in memory using byte addition

I. ARM Assembly Code

II. Output Screen Shots

(One Screenshot including Register Window,Memory Window and Code Window)

```
.DATA


NUM1: .BYTE 5
```

```
NUM2: .BYTE 30

NUM3: .BYTE 0
```

```
.TEXT
```

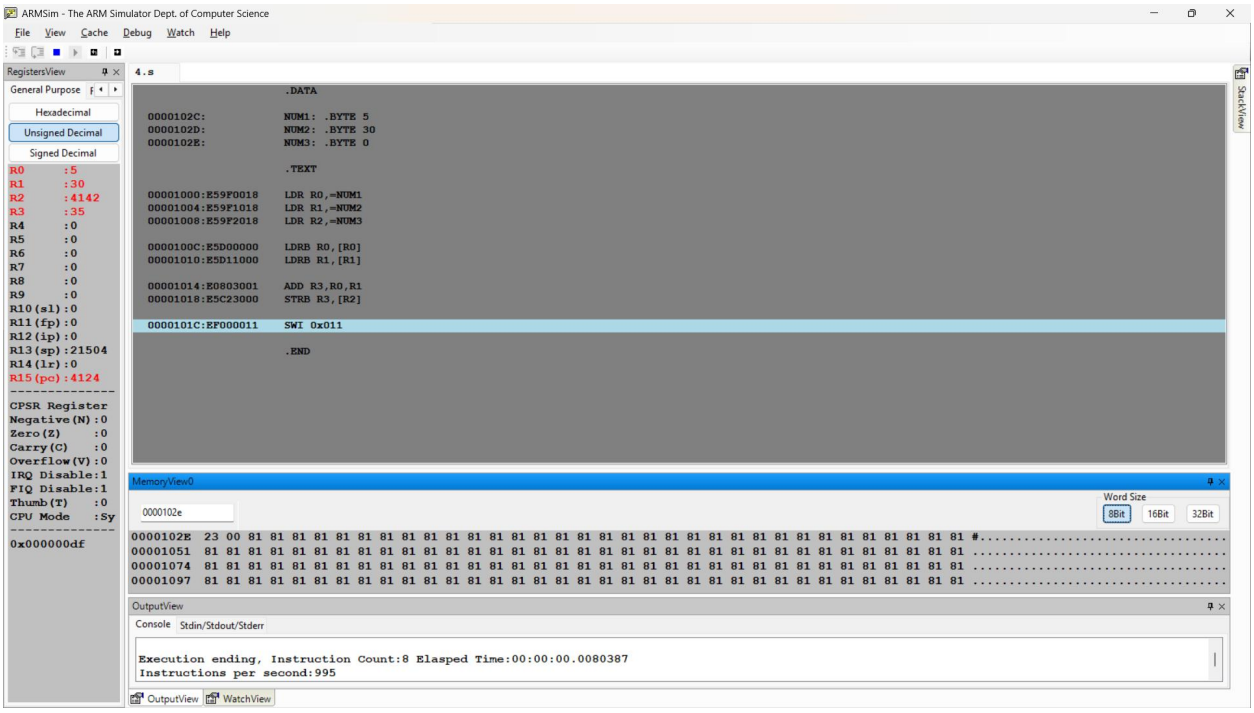
```
LDR R0,=NUM1

LDR R1,=NUM2

LDR R2,=NUM3
```

```
LDRB R0,[R0]

LDRB R1,[R1]
```

```
ADD R3,R0,R1

STRB R3,[R2]
```

```
SWI 0x011
```

```
.END
```



Microprocessor and Computer Architecture

UE22CS251B

4th Semester, Academic Year 2023-24

Date:

Name: Harshit Chandak	SRN: PES2UG24CS185	Section C

LAB #____2_____ Assignment Question 1

Title of the Program

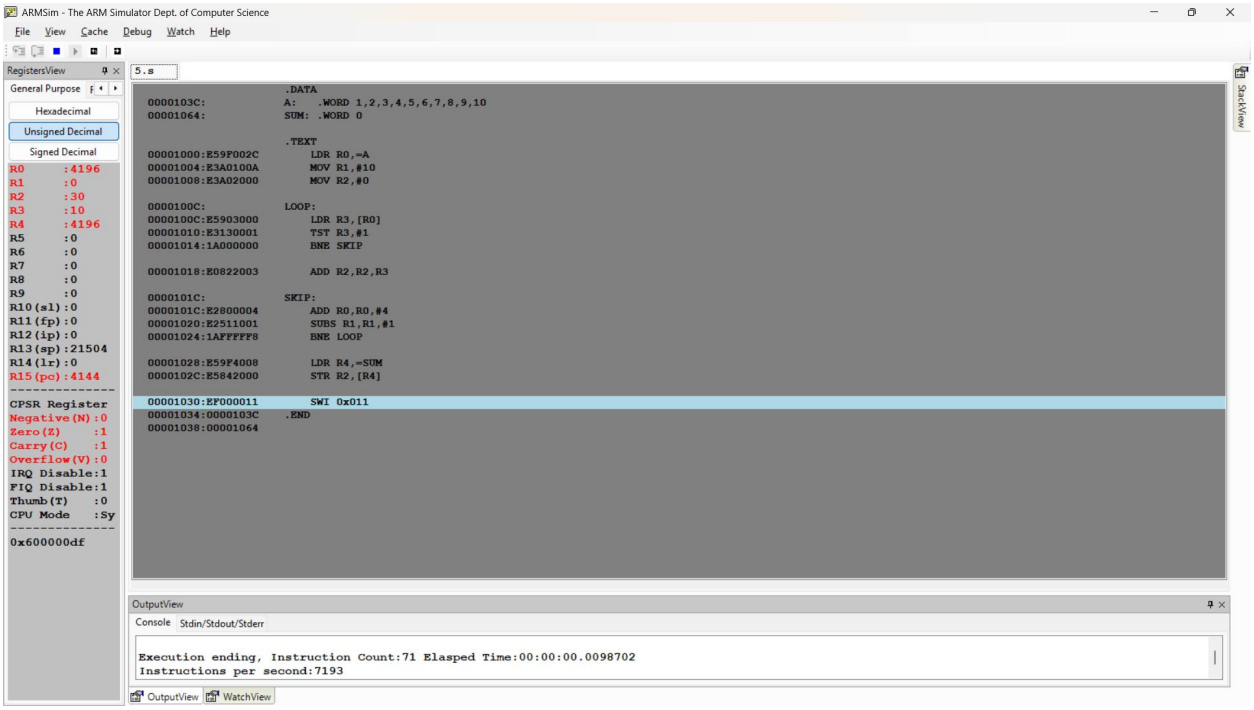
Write an ALP using ARM7TDMI to add only even numbers stored in memory location for a given set of numbers and store the sum in the memory location.

I. ARM Assembly Code

II. Output Screen Shots

(One Screenshot including Register Window,Memory Window and Code Window)

```
.DATA
A:   .WORD 1,2,3,4,5,6,7,8,9,10
SUM: .WORD 0

.TEXT
    LDR R0,=A
    MOV R1,#10
    MOV R2,#0

LOOP:
    LDR R3,[R0]
    TST R3,#1
    BNE SKIP

    ADD R2,R2,R3

SKIP:
    ADD R0,R0,#4
    SUBS R1,R1,#1
    BNE LOOP

    LDR R4,=SUM
    STR R2,[R4]

    SWI 0x011
.END
```



Microprocessor and Computer Architecture

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LAB #____2_____

Assignment Question 2

Title of the Program

Write an ALP to evaluate the expression (A+B) + (13*B), where A and B are available in memory location. Store the final result in memory Location C

* Use LSL instruction for multiplication

I. ARM Assembly Code

II. Output Screen Shots

(One Screenshot including Register Window,Memory Window and Code Window)

```
.DATA


A: .WORD 9

B: .WORD 6

C: .WORD 0
```

```
.TEXT
```

```
LDR R0,=A

LDR R1,=B

LDR R6,=C
```

```
LDR R0,[R0]

LDR R1,[R1]
```

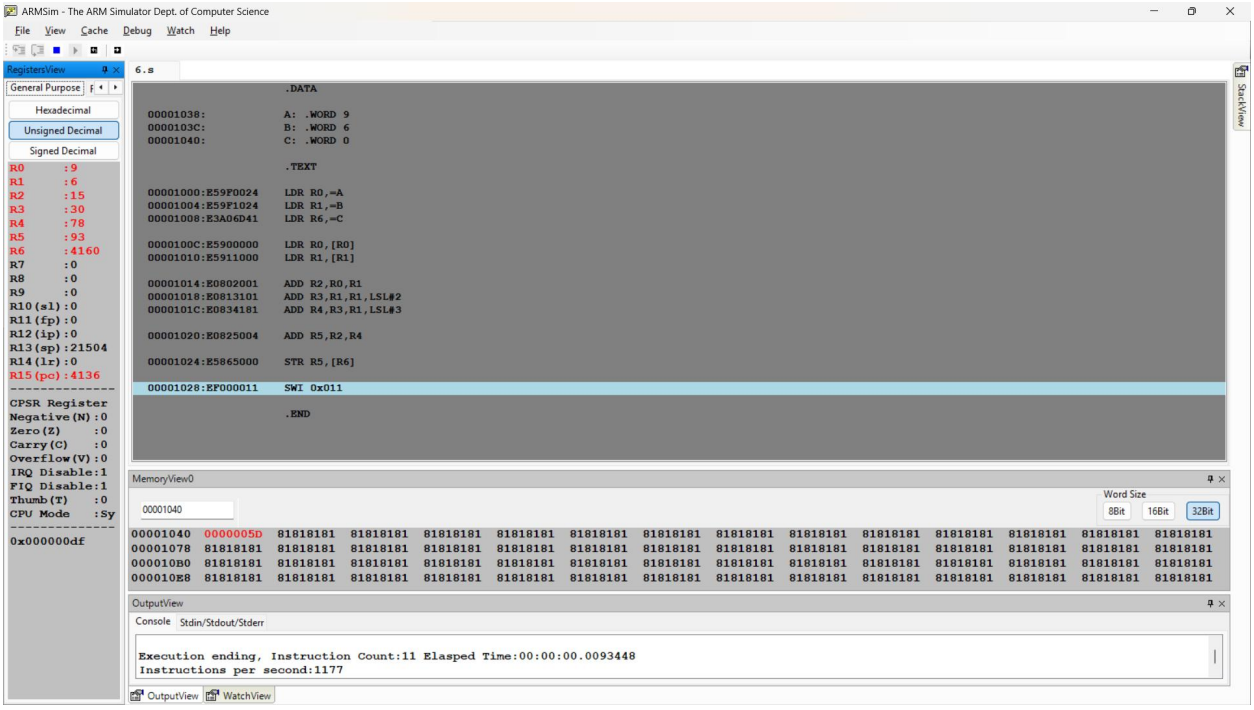
```
ADD R2,R0,R1

ADD R3,R1,R1,LSL#2

ADD R4,R3,R1,LSL#3
```

```
ADD R5,R2,R4
```

```
STR R5,[R6]
```

```
SWI 0x011
```

```
.END
```



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:
Name:
SRN:
Section:
Date: