**Microprocessor and Computer Architecture**

**UE24CS251B**

**4th Semester, Academic Year 2025-26**

Date:

| Name: Harshit Chandak | SRN: PES2UG24CS185 | Section C |
|---|---|---|

LAB #____4_____ Program Number: ____1___

Title of the Program

**Write an ALP to perform Convolution using MLA instruction (Addition of multiplication of respective numbers of loc A and loc B).**

I. Typed ARM Assembly Code

II. Output Screen Shot

***( Screenshot including Register Window,Output Window and Code Window)***

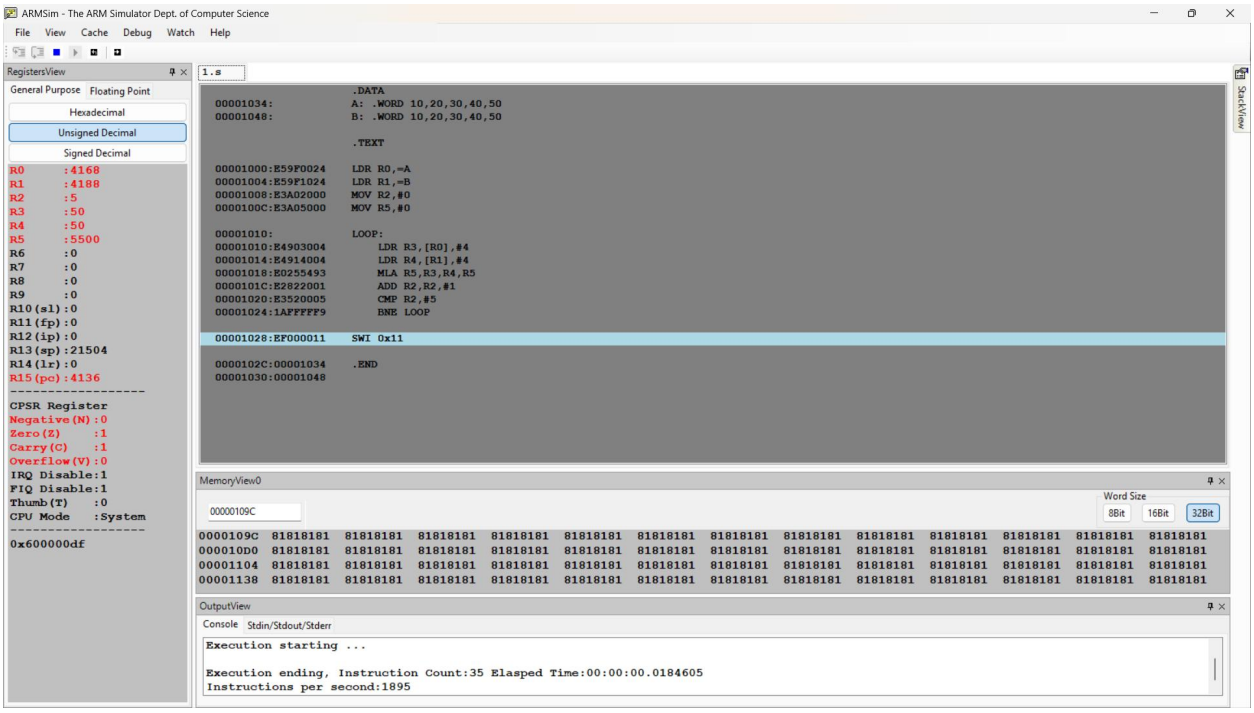
```
.DATA
A: .WORD 10,20,30,40,50
B: .WORD 10,20,30,40,50

.TEXT
```

```
LDR R0,=A
LDR R1,=B
MOV R2,#0
MOV R5,#0
```

```
LOOP:
    LDR R3,[R0],#4
    LDR R4,[R1],#4
    MLA R5,R3,R4,R5
    ADD R2,R2,#1
    CMP R2,#5
    BNE LOOP
```

```
SWI 0x11
```

```
.END
```




# Microprocessor and Computer Architecture

## UE24CS251B

## 4th Semester, Academic Year 2025-26

Date:

| Name: Harshit Chandak | SRN: PES2UG24CS185 | Section C |
|---|---|---|

LAB #____4_____ Program Number: ____2___

Title of the Program

**Write a program in ARM7TDMI-ISA to generate a diagonal matrix.**

**; Note: do not read the matrix elements.**

**Let the Diagonal Value be 2**

I. Typed ARM Assembly Code
II. Output Screen Shot

***(One Screenshot including Register Window,Output Window and Code Window,Memory Window)***

```
.DATA
A: .WORD 0,0,0,0,0,0,0,0,0

.TEXT
```

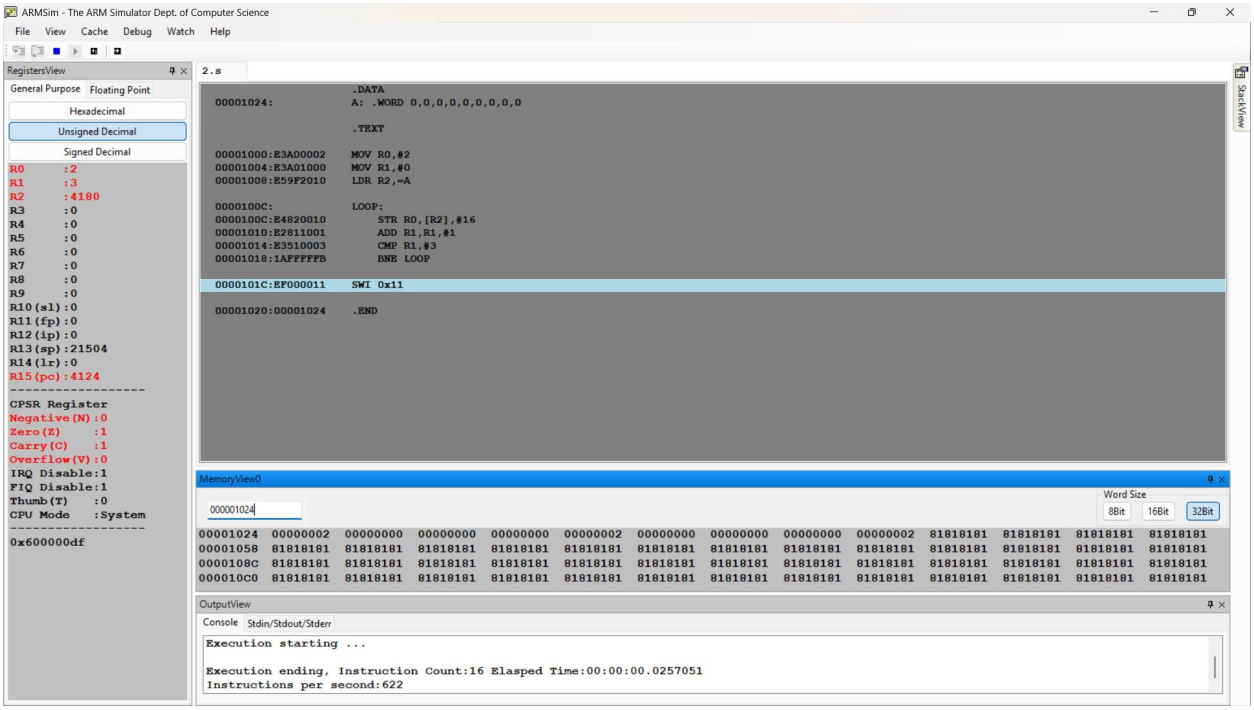
```
MOV R0,#2
MOV R1,#0
LDR R2,=A
```

```
LOOP:
    STR R0,[R2],#16
    ADD R1,R1,#1
    CMP R1,#3
```

```
    BNE LOOP
```

```
SWI 0x11
```

```
.END
```




# Microprocessor and Computer Architecture

## UE24CS251B

## 4th Semester, Academic Year 2025-26

Date:

| Name: Harshit Chandak | SRN: PES2UG24CS185 | Section C |
|---|---|---|

LAB #____4_____ Program Number: ____3___

Title of the Program

**Write a program in ARM7TDMI-ISA to transfer a block of 16 words stored at memory location X to memory location Y using Load Multiple and Store Multiple instructions. The rate of transfer is 24 bytes**

I. ARM Assembly Code

II. Output Screen Shot

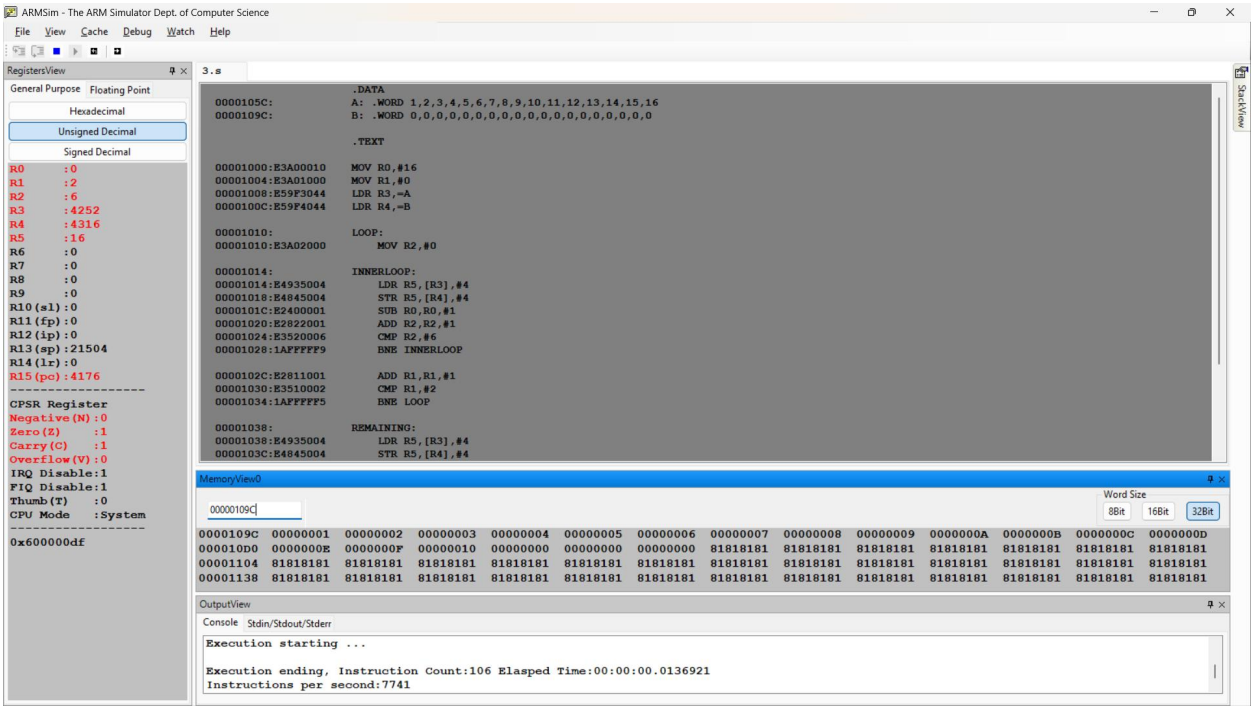
***(One Screenshot including Register Window,Memory Window and Code Window)***

```
.DATA
A:  .WORD
1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16
B:  .WORD
0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0

.TEXT
```

```
MOV R0,#16
MOV R1,#0
```

```
LDR R3,=A
LDR R4,=B

LOOP:
    MOV R2,#0

INNERLOOP:
    LDR R5,[R3],#4
    STR R5,[R4],#4
    SUB R0,R0,#1
    ADD R2,R2,#1
    CMP R2,#6
   BNE INNERLOOP

    ADD R1,R1,#1
    CMP R1,#2
    BNE LOOP

REMAINING:
    LDR R5,[R3],#4
    STR R5,[R4],#4
    SUB R0,R0,#1
    CMP R0,#0
    BNE REMAINING
    BEQ EXIT
EXIT:
    SWI 0x11
```

```
.END
```



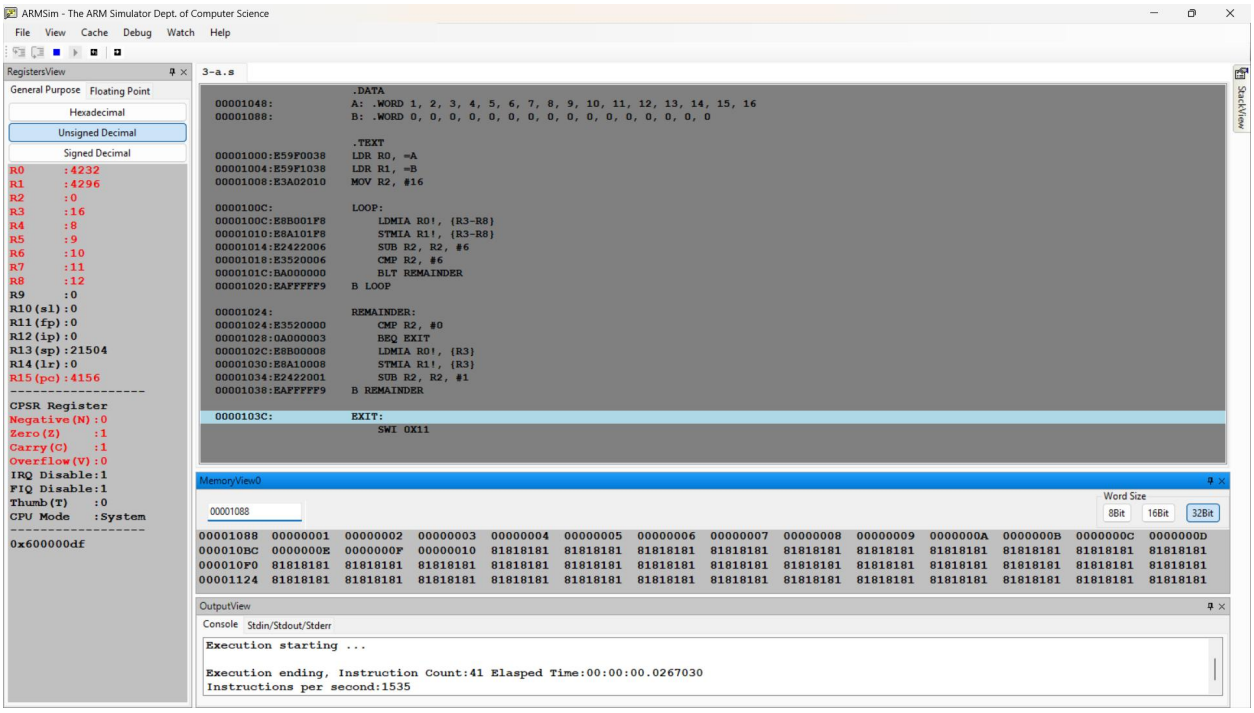

2 ND WAY

```
.DATA
A: .WORD 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
12, 13, 14, 15, 16
B: .WORD 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
0, 0, 0, 0, 0

.TEXT
LDR R0, =A
LDR R1, =B
MOV R2, #16
```

```
LOOP:
    LDMIA R0!, {R3-R8}
    STMIA R1!, {R3-R8}
    SUB R2, R2, #6
    CMP R2, #6
    BLT REMAINDER
B LOOP
```

```
REMAINDER:
    CMP R2, #0
    BEQ EXIT
    LDMIA R0!, {R3}
    STMIA R1!, {R3}
    SUB R2, R2, #1
B REMAINDER
```

```
EXIT:
    SWI 0X11
```




# Microprocessor and Computer Architecture

## UE22CS251B

## 4th Semester, Academic Year 2023-24

Date:

| Name:Harshit Chandak | SRN:PES2UG24CS185 | Section C |
|---|---|---|

LAB #____4_____ Program Number: ____4___

Title of the Program

**Write an ARM ALP to perform element-wise addition of two 3×3 matrices using indexed addressing and nested loops.**

## Requirements

a. **Matrices A and B each contain 9 elements (3 rows × 3 columns)**
b. **Matrix C should store the sum of corresponding elements**
c. **Use nested loops to traverse rows and columns**
d. **Use the MLA (Multiply Accumulate) instruction to compute the memory offset**
e. **Each matrix element is a 32-bit word**

I. ARM Assembly Code

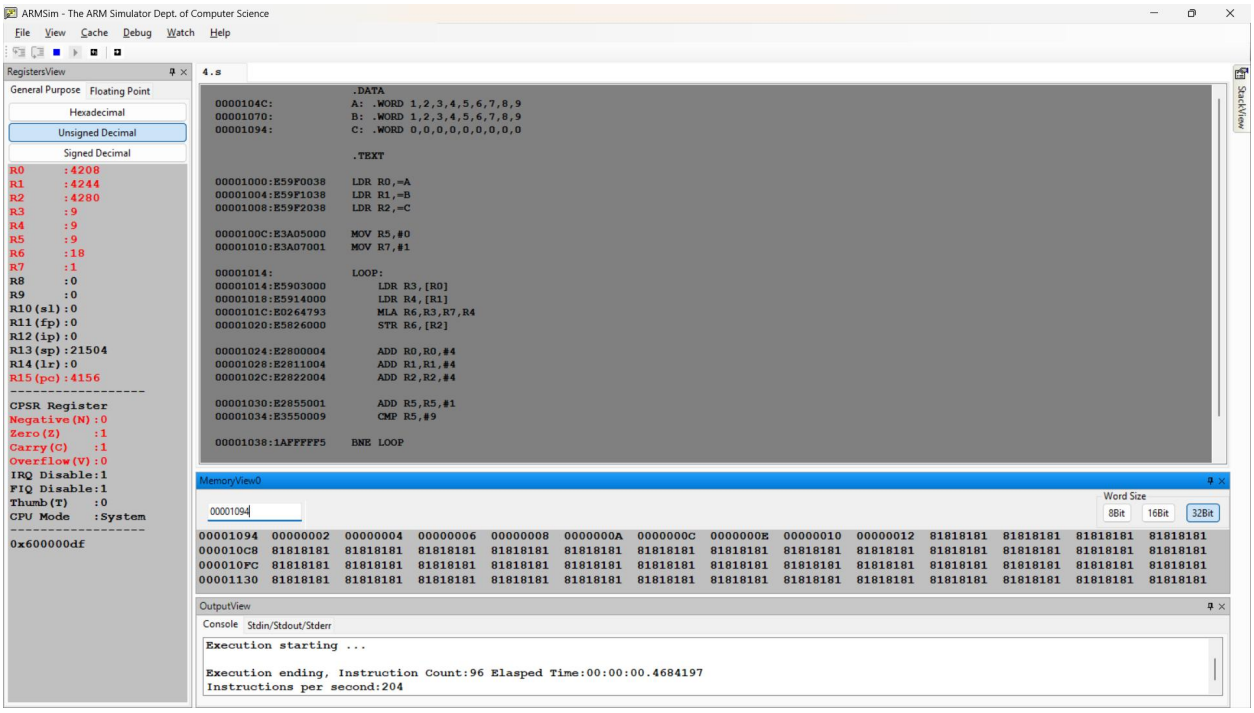
II. Output Screen Shot

***(One Screenshot including Register Window,Memory Window and Code Window)***

```
.DATA
A: .WORD 1,2,3,4,5,6,7,8,9
B: .WORD 1,2,3,4,5,6,7,8,9
C: .WORD 0,0,0,0,0,0,0,0,0

.TEXT
```

```
LDR R0,=A
LDR R1,=B
```

```
LDR R2,=C

MOV R5,#0
MOV R7,#1

LOOP:
    LDR R3,[R0]
    LDR R4,[R1]
    MLA R6,R3,R7,R4
    STR R6,[R2]

    ADD R0,R0,#4
    ADD R1,R1,#4
    ADD R2,R2,#4

    ADD R5,R5,#1
    CMP R5,#9

BNE LOOP

SWI 0x11

.END
```




# Microprocessor and Computer Architecture

## UE22CS251B

## 4th Semester, Academic Year 2023-24

Date:

| Name: Harshit Chandak | SRN: PES2UG24CS185 | Section C |
|---|---|---|

LAB #____4_____ Assignment Question 1

Title of the Program

**Write an ARM7TDMI ALP to check whether a given 32-bit number has odd or even parity (number of 1s).**
**It stores 00 in R7 if parity is EVEN and 01 in R7 if parity is ODD**

I. ARM Assembly Code

II. Output Screen Shots

***(Two Screenshot for each case including Register Window,Memory Window and Code Window)***

```
.DATA
NUM: .WORD 4
PARITY: .WORD 0

.TEXT
```

```
LDR R0,=NUM
LDR R1,[R0]
LDR R7,=PARITY
MOV R8,#00
MOV R9,#01
```

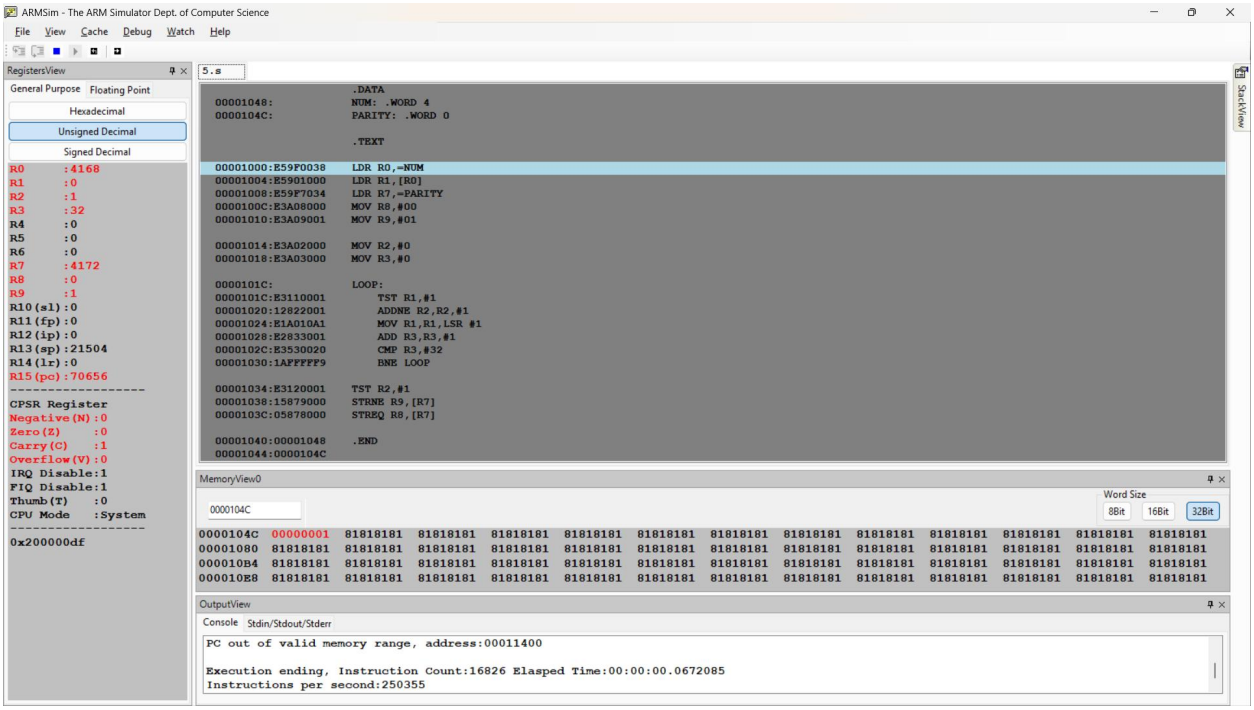
```
MOV R2,#0
MOV R3,#0
```

```
LOOP:
    TST R1,#1
    ADDNE R2,R2,#1
```

```
    MOV R1,R1,LSR #1
    ADD R3,R3,#1
    CMP R3,#32
    BNE LOOP
```

```
TST R2,#1
STRNE R9,[R7]
STREQ R8,[R7]
```

```
.END
```




## Microprocessor and Computer Architecture

## UE22CS251B

**4th Semester, Academic Year 2023-24**

Date:

| Name: Harshit Chandak | SRN: PES2UG24CS185 | Section C |
|---|---|---|

LAB #____3_____

Assignment Question 2

Title of the Program

**Write an ALP to perform Convolution using MUL instruction (Addition of multiplication of respective numbers of loc A and loc B)**

I. ARM Assembly Code

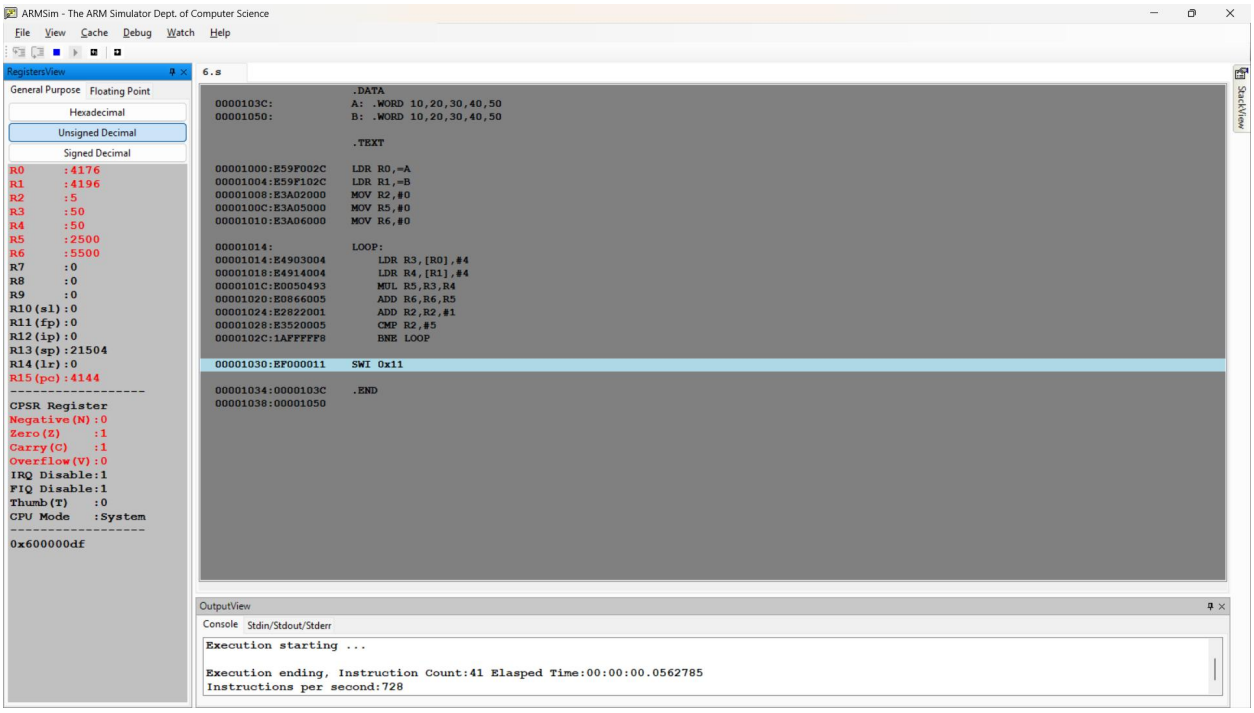
II. Output Screen Shots

***(One Screenshot including Register Window,Memory Window and Code Window)***

```
.DATA
A: .WORD 10,20,30,40,50
B: .WORD 10,20,30,40,50

.TEXT
```

```
LDR R0,=A
LDR R1,=B
```

```
MOV R2,#0
MOV R5,#0
MOV R6,#0

LOOP:
    LDR R3,[R0],#4
    LDR R4,[R1],#4
    MUL R5,R3,R4
    ADD R6,R6,R5
    ADD R2,R2,#1
    CMP R2,#5
    BNE LOOP

SWI 0x11

.END
```




## Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

Name:

SRN:

Section:

Date: