Comparative Analysis of Decoders using Static & Dynamic CMOS Logic.

Chandan Srinivas
Department of Electronics and Communication Engineering
Dayananda Sagar College of Engineering
Bengaluru, India
chandansrinivas55@gmail.com

Bhargav G S
Department of Electronics and Communication Engineering
Dayananda Sagar College of Engineering
Bengaluru, India
bhargavgs47@gmail.com

Chandan S P
Department of Electronics and Communication Engineering
Dayananda Sagar College of Engineering
Bengaluru, India
spchandan@gmail.com

Kuber Eshwar A
Department of Electronics and Communication Engineering
Dayananda Sagar College of Engineering
Bengaluru, India
kubereshwar62666@gmail.com

P Vimala
Department of Electronics and Communication Engineering
Dayananda Sagar College of Engineering
Bengaluru, India
ervimala@gmail.com

***Abstract*— Address Decoders are trivial yet essential element of a digital block, that can consume considerable amount of area on an IC and power during the read and write cycle. These facilitates reduction in number of interconnects by a factor of log2N, where N is independent address locations. Huge blocks of SRAM memory having various banks of SRAM cell, have multiple stages of decoder that are hierarchically linked. The MSB (Most significant bits) is decoded(pre-decoded) at the first stage, leading to selection of array that is to be accessed by providing enable signals for the subsequent decoder stages that further helps in enabling the world lines. These word lines turn on the access transistors (in the case of SRAM block) or any other element connected to it when required input is given. This paper aims at designing, comparing and analyzing the performance of 3:8 Static logic based and Dynamic logic-based decoder. The designed and analyzed decoder displayed an intuitively legible differences which allows a designer to choose based on the application requirements. The static decoder has very low power consumption of 74.1007µW (micro-Watt 10e-6). while dynamic decoder has a about 98 times more at 5.746mW (milli watt 10e-3). Similarly, in terms of delay static decoder has both, rise time and fall time delay in terms of ps (pico second 10e-12) while dynamic decoder had more delay (in units of ns 10e-9) in comparison. The main advantage of a decoder is area, which plays a vital role in modern designs where researchers are in the pursuit of new technologies to have more transistors in the same unit area. The dynamic decoders top this aspect where they require merely 46 transistors while static decoder requires 70 and consumes about 57% more area on silicon when fabricated. All the simulations were performed after drawing layouts in order to obtain accurate results of delay and power consumption by considering parasitic capacitance and resistances offered by the interconnects and the transistor itself. The design of the digital circuit is carried out using technology node 180nm (gpdk180) and Cadence Virtuoso Tool Suite.**

Keywords— static decoder, dynamic decoder, Cadence virtuoso, gpdk180, rise and fall time.

I. INTRODUCTION

Due to their low power consumption, broad dynamic range, excellent reliability, compact design, and low price, CMOS circuits are now the industry standard for digital design [1-4]. It is crucial for the circuit designer to consider speed, power consumption, and area into account while choosing digital components for a design. Decoders are an essential component in digital circuit design, and play a crucial role in converting encoded information into a form that can be easily understood and processed by a system [5-8]. Two commonly used types of decoders are static and dynamic decoders[9-12].

In this paper, we will provide a comprehensive comparison of 3:8 static and dynamic decoders, highlighting their key differences and similarities, as well as their respective advantages and disadvantages. We will examine the design and implementation of 3:8 static and dynamic decoders, as well as their performance characteristics such as speed, power consumption, and area requirements. Furthermore, we will discuss the various applications of static and dynamic decoders and provide insights into the trade-offs between these two types of decoders. Our goal is to provide a comprehensive understanding of the pros and cons of static and dynamic decoders, and to help digital circuit designers make informed decisions when choosing between these two types of decoders.

II. LITERATURE REVIEW

Research [5] suggests an efficient architecture where a 2:4 static address decoder using hybrid CMOS logic, although this research is performed using 22nm logic, it provides an efficient way of reducing the area consumed by the design when implemented on the chip. In [6], the detailed analysis of pseudo-NMOS logic is explained which describes the impact of ratios of pMOS and nMOS while designing. It also details the variation of parameters such as power, delay and noise margin of the logic design when pseudo-NMOS logic is utilized. According to [6] the VOL i.e., output low voltage is increased when pseudo-MNOS is used and in turn the lowers the noise margin of the logic element. This in turn creates a problem i.e., when the noise margin is reduced the probability of output being don't care (X) condition increases, which is undesirable in digital circuits. In order to mitigate this risk of having don't care designer must implement a pMOS with larger aspect ratio, which helps in increasing the VOL in turn increases the noise margin of the circuit. Increasing the size of pMOS transistor has other repercussions such as increase in power consumption than before. Research [7] utilizing 65nm CMOS process technology, has proposed schemes for reducing the effect of noise on dynamic circuits/logic which

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displays improvement of 2.6% with respect to noise when a delay technique is used and while using the mirror scheme achieved 25.2% improvement.

III. TYPES OF CMOS LOGIC

A. Static CMOS Circuit

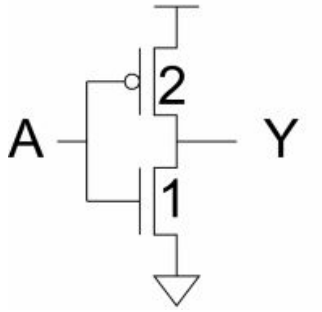

Fig. 1. Static CMOS logic

Static CMOS circuit Figure [1] use complementary nMOS pulldown and pMOS pullup networks to implement logic gates or logic functions in integrated circuits. In comparison to dynamic logic static logic style consumes relatively less power and is robust against the noise the normally tends to corrupt the bit values. The transistor sizing in static logic is fairly simple, generally, 2:1 ratio of pMOS to nMOS is adopted.

Number of transistors required = 2*N

Where, N is number of inputs or fan-in of static logic.

B. Dynamic CMOS Logic

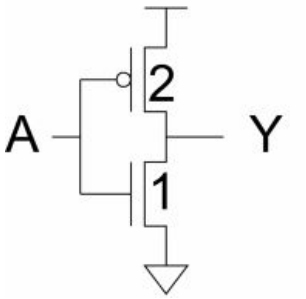

Fig. 2. Static CMOS logic

Dynamic gates Figure [2] use a clocked pMOS pullup. The implemented logic function or the logic gate is achieved through 2 modes of operation: Precharge and Evaluate. Dynamic CMOS is further categorized such as pseudo-NMOS, Ratioed logic, Domino logic in which pseudo-NMOS is the focus of paper.

A. Pseudo-NMOS Logic

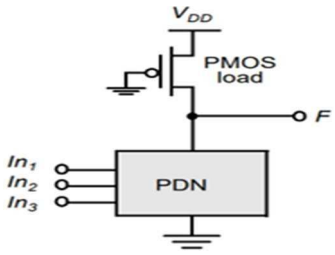

Fig. 3. Pseudo-NMOS logic

Pseudo-NMOS Figure [3] comprises of only PDN (Pull-Down Network) network with a single PMOS transistor which acts as a simple load. The single PMOS is always grounded leading the output F to be always high (V_{DD}). Consequently, the nominal output high voltage $V_{OH} = V_{DD}$. Nominal output low voltage is no equal to 0 as in conventional CMOS due to the fight between PDN and the grounded PMOS and acting as load device. As the V_{OL} is not equal to 0, this reduces the Noise Margin and leads to increase in static power dissipation. Gate complexity is reduced but at the expense of static power consumption, asymmetrical response and reduced Noise Margin.

Number of transistors required = N + 1

Where, N is number of inputs or fan-in of dynamic logic. The VOL i.e., output low voltage is given by the formula below

$$V_{OL} = \frac{\mu p * Wp}{\mu n * Wn} * V_{DSAT}$$

Where, μp μn is mobility and Wp and Wn is the aspect ratios of the pMOS and nMOS respectively. VDSAT is the saturation voltage.

The main disadvantage of the dynamic logic style is power consumption which is explained using the formula below.

$$P_{low} = V_{DD} * I_{low}$$

Where, P_{low} is static power dissipated when the output is low through direct current path between V_{DD} and GND, V_{DD} is the supply voltage.

IV. METHODOLOGY

The implementation flow for the decoders is given in Figure [4]. First, the schematics of 3:8 static and dynamic decoders are designed using 180nm transistor technology in cadence virtuoso tool. The pre-layout simulation is carried out in spectre platform to verify the functionality and measure the performance of the decoder circuits. After simulation is successful, the physical implementation of the decoders is designed in the Cadence Layout XL tool. Once the layout of the decoders is completed and DRC\LVS is checked, the simulation is carried out again to consider parasitic resistances & capacitances and their functionality is verified. After post layout simulation their parameters are extracted and compared.

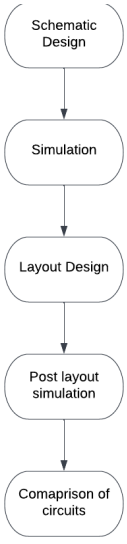

Fig. 4. Workflow of the research undertaken

V. WORKING

Although the outputs of both decoders are same for any particular input, they are designed differently where one utilizes conventional static logic implementation and another doesn't. And also, one uses clock (control) signal and another doesn't. The truth table of 3:8 decoder is shown in Fig [5].

Their designing depends on the Boolean expressions for each output because of which truth table is necessary. Their working can be explained using their schematic design which was designed using the Boolean expressions.

A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Fig. 5. Truth table of 3:8 decoder

The boolean expression of the above truth table is given as

D0 = A2'.A1'.A0' D1 = A2'.A1'.A0 D2 = A2'.A1.A0'

D3 = A2'.A1.A0 D4 = A2.A1'.A0' D5 = A2.A1'.A0

D6 = A2.A1.A0' D7 = A2.A1.A0

A. *Static Decoder*

Static decoder is designed with standard CMOS technology, where number of PMOS (pull-up) transistors are equal to number of NMOS (pull-down) transistors in the circuit. Here, decoder is designed using the Boolean expression for every output in the truth table. And there is no clock signal involved in the design which makes the decoder static i.e. output is dependent on only input.

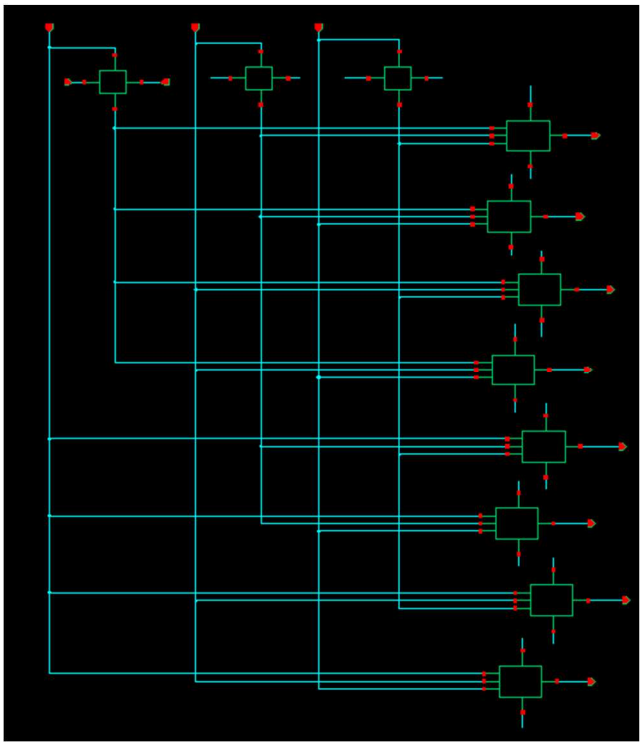

Fig. 6. Static decoder schematic view

From Figure [6], We see that every output pins of decoder are connected to the output of an AND gate with its input pins connected to decoder input pins according to the Boolean expression of each output. To satisfy the negations of inputs in any Boolean equation, each input is inverted using an inverter as shown in Figure [6].

B. *Dynamic Decoder*

Dynamic decoder is designed prominently with NMOS transistors according to the Boolean expressions from the truth table with only one PMOS transistor connected to the NMOS (pull-down) network & a clock signal controlling the circuit operations. This decoder is dynamic because the outputs depend on both the inputs & the clock signal.

From Figure [7]. We see that for every output there is single PMOS transistor where their gate terminals are connected to clock signal to control decoder output. And every output of decoder is designed prominently using NMOS transistors according to the Boolean expression of outputs & inverters are used to negate the input signals to satisfy the Boolean equations.

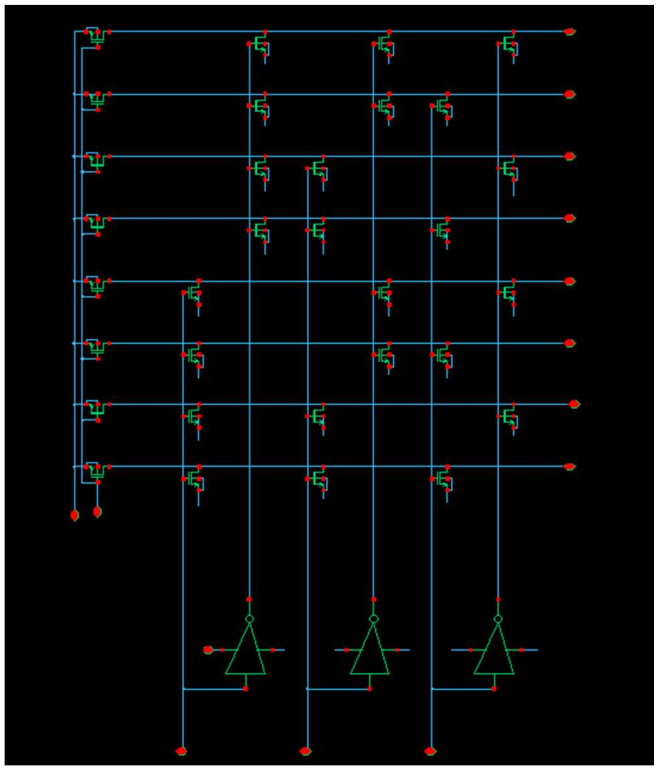

Fig. 7. Dynamic decoder schematic view

VI. RESULTS AND DISCUSSION

As discussed in the methodology, the implementation was carried using Cadence virtuoso tool. Figure [8] and Figure[12] shows the transient analysis and power dissipation of static decoder and dynamic decoder respectively. The transient analysis is verified using the truth table shown in Figure [5]. The biggest issues with high-performance transistor technology are power dissipation and delay time. The frequency of operation is directly related to the power dissipation and delay time. Therefore, a chip shouldn't operate at a higher speed than is required. For the design to work effectively, it is essential to select low power consumption and less delay as design component.

To calculate the actual delay time and power consumption of the digital component the pre and post layout simulation need to be performed. The pre-layout and post-layout simulation for static decoder Figure [9] and Figure [10]. Similarly, for the dynamic decoder pre-layout and post- layout simulation is shown in Figure [13] and Figure [14] respectively. To determine the actual performance of the digital component, back annotation is important which is performed considering the parasitic capacitances and resistances of the transistors and the interconnecting nets used. Back annotated graph for Static decoder depicted in Figure [11] and dynamic decoder is given in Figure [15] where the green & brown waves represent the pre-layout & post-layout graphs respectively. From Figure [11] and [15] it is quite evident that a delay is introduced after post-layout simulation due to parasitics.

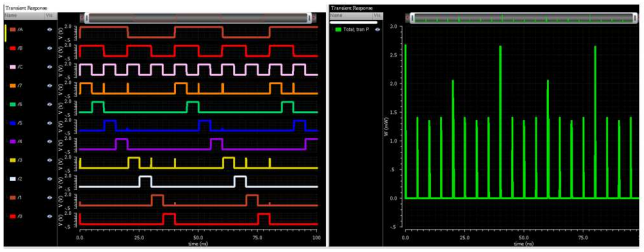

Fig. 8. 3:8 Static decoder transient analysis and power dissipation.

13	Avg_power	45.8716u	✓
14	rise_time	42.2661p	✓
15	fall_time	20.3896p	✓

Fig. 9. Pre-layout simulation of static decoder

13	Avg_power	74.1007u	✓
14	rise_time	52.6836p	✓
15	fall_time	29.5499p	✓

Fig. 10. Post-layout simulation of static decoder

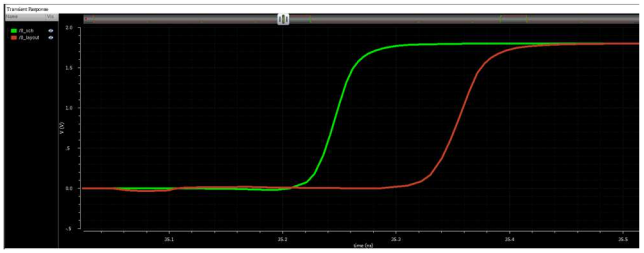

Fig. 11. Back annotated graph of Static decoder

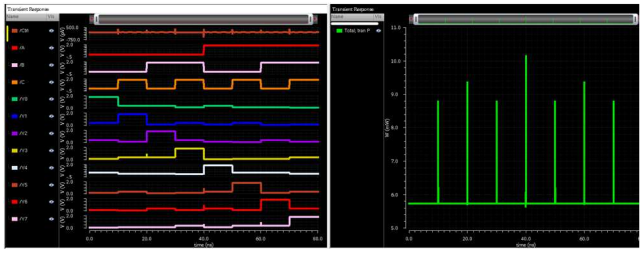

Fig. 12. 3:8 Dynamic decoder transient analysis & power analysis

10	Avg_power	5.7426m	✓
11	rise_time	50.5834p	✓
12	fall_time	10.0458n	✓

Fig. 13. Pre-layout simulation of dynamic decoder

10	Avg_power	5.74648m	✓
11	rise_time	93.9734p	✓
12	fall_time	10.0779n	✓

Fig. 14. Post-layout simulation of dynamic decoder

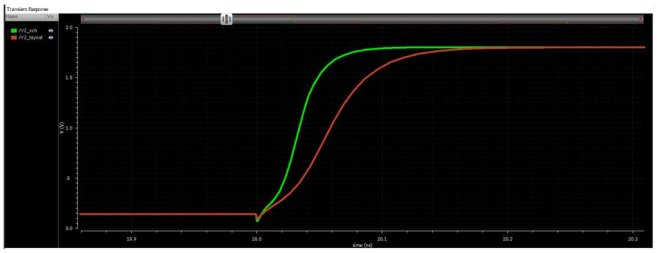

Fig. 15. Back annotated graph of Dynamic decoder

TABLE I. STATIC & DYNAMIC DECODER COMPARISON

Parameters Considered	**Post-Layout Simulation Results**	
	Static Decoder	***Dynamic Decoder***
Dynamic Power	74.1007uW	5.746mW
Rise Time Delay	52.6836ps	93.9734ps
Fall Time Delay	29.5499ps	10.077ns
No. of transistors	70	46
Area Consumed	14,825.67 μm^2	6,258.96 μm^2

The designed decoders are simulated using the ADE L environment of the cadence tool suite and the obtained values are tabulated in Table [I]. Table [I] depicts various performance parameters such as dynamic power, delays and area consumed after performing post layout simulation and based on the values of number of transistors and area consumed, dynamic decoder has an upper hand but when delay and power consumption is considered static decoder is found to be better.

VII. CONCLUSION

Trade-offs between various parameters are made while designing an integrated circuit. These trade-offs are made based on the design requirements such as area reduction, power consumption reduction or delay reduction. Similarly, static and dynamic decoders are designed and compared based on essential parameters namely, average power consumption, delay time, number of transistors and area consumed. A detailed post-layout simulation is carried out considering the parasitic resistances and capacitances of the various metal and polysilicon layers involved. Based on the simulation result the static decoder consumes less power about 98% less power in comparison, and the rise time about 40ps lesser. Similarly, the fall time is reduced by about 10ns. The area consumed by dynamic decoder is 57% less than that of static decoder and in terms of transistors static decoder requires 46 and dynamic decoder requires 70.

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