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A
UG PROJECT REPORT
on

Design of Peripheral Circuitry for SRAM Array Architecture

Submitted in partial fulfillment of the requirement for the degree of

Bachelor of Engineering
in
Electronics & Communications Engineering - ECE
by

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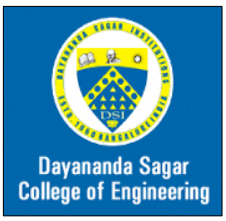

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Certificate

Certified that the project work entitled "Design of Peripheral Circuitry for SRAM Array Architecture" carried out by **Bhargav G S** (1DS19EC023), **Chandan S P** (1DS19EC032), **Chandan Srinivas** (1DS19EC033), **Kuber Eshwar** Name (1DS19EC067) are bonafide students of the ECE Dept. of Dayananda Sagar College of Engineering, Bangalore, Karnataka, India in partial fulfillment for the award of Bachelor of Engineering in Electronics & Communication Engineering of the Visvesvaraya Technological University, Belagavi, Karnataka during the academic year 2022-23. It is certified that all corrections / suggestions indicated for project work have been incorporated in the report deposited to the ECE department, the college central library & to the university. This final year project report **(Course Code : 19EC8ICPR2)** Phase-II has been approved as it satisfies the academic requirement in respect of project work prescribed for the said degree.

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Declaration

Certified that the project work entitled, "Design of Peripheral Circuitry for SRAM Array Architecture." with the project work course code **19EC8ICPR2** is a bonafide work that was carried out by ourselves in partial fulfillment for the award of degree of Bachelor of Engineering in Electronics & Communication Engg. of the Visvesvaraya Technological University, Belagavi, Karnataka during the academic year 2022-23. We, the students of the project group/batch no.R-31 do hereby declare that the entire project work has been done on our own & we have not copied or duplicated any other's work or may be the extension of the works done by the earlier students. The results embedded in this UG project report has not been submitted elsewhere for the award of any type of undergraduate degree.

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Table of Contents

List of Figures

List of Tables

Nomenclature and Acronyms

Abbreviations (Alphabetical Order) :

SRAM : Static Random Access Memory

SNM : Static Noise Margin

CPU : Central Processing Unit

RAM : Random Access Memory

DRAM : Dynamic Random Access Memory

CMOS : Complementary Metal-oxide Semiconductor

R/W : Read Write

ADE L : Analog Design Environment L

WL : Wordline

BL : Bitline

BLB : Bitline Bar

GUI : Graphics User Interface

DRC : Design Rule Check

LVS : Layout versus Schematic

Abstract

The final year project work undertaken by us involves the design of a peripheral circuitry for 6T SRAM Array architecture and evaluation of performance of the SRAM Array. The main aim of our project is to compare various types of sense amplifiers and precharge circuits available and select the appropriate circuit among them along with decoder, to design the SRAM array architecture. After the design of SRAM array architecture with peripheral circuitry, the functionality of the design is verified and the performance parameters such as Read/Write SNM (Signal Noise Margin), Power dissipation and delay time. The designs and simulations is carried out using Cadence virtuoso and Hspice software.

Keywords : *SRAM, Cadence virtuoso, SNM*

Chapter-1

Introduction

In computer system design, Memory hierarchy is an enhancement to organize the memory such that it can minimize the access time. The memory hierarchy was developed based on locality of references. The figure below clearly demonstrates the different levels of memory hierarchy.

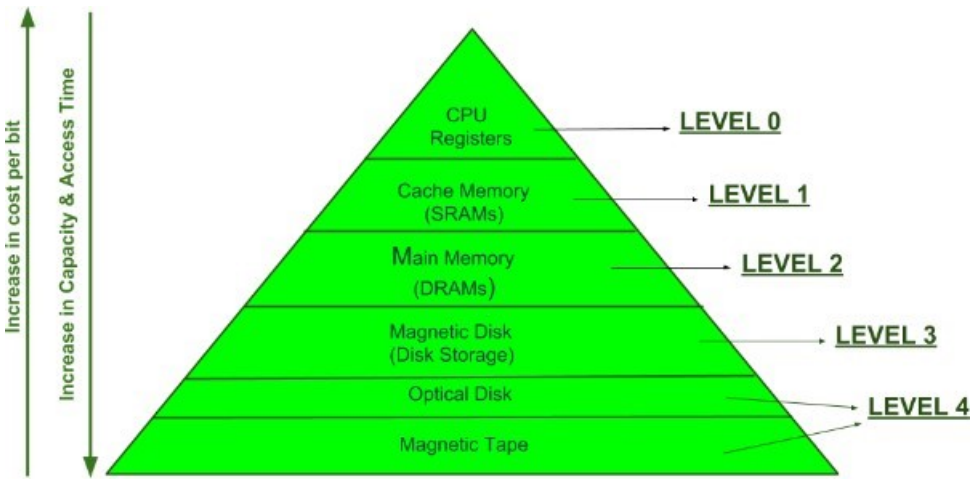


Fig 1. Memory hierarchy

Design The memory hierarchy is mainly divided into 2 types:

- External memory or Secondary memory: This comprises of magnetic disk, magnetic tape and optical disk. These are storage devices which are accessible by the processor via I/O module.
- Internal memory or Primary memory: This contains main memory, cache memory and CPU registers. These are directly accessible by the processor.

Memory arrays are mainly classified into 3 types:

- Random access memory: It is accessed with an address
- Serial access memory: Memory is accessed sequentially so no address is necessary.
- Content addressable memory: It determines which address contain data that matches a specified key.

Detailed memory array classification is given below

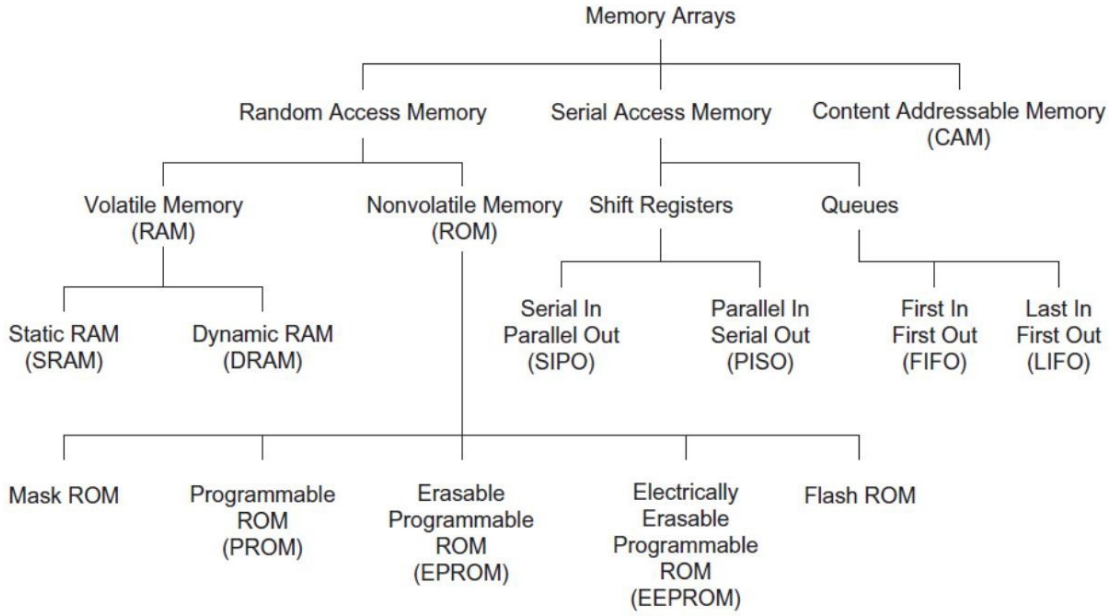


Fig 2. Classification of memory array

Random access memory (RAM) is volatile memory. RAM consumes significant amount of power and is mainly responsible for the performance of the system. So, the delay of the RAM is crucial for system performance. So, we chose SRAM, which is one of the types of RAM, and it is much preferred due to its ability to retain data, ease of implementation, low power consumption and low standby leakage compared to DRAM. Dynamic power dissipation helps to determine the battery life of portable devices, where SRAM is better as the power dissipation is less than DRAM. Therefore, we implement the SRAM array using the peripheral circuitry.

1.1 Overview of the project work

This project explores the design and analysis of peripheral circuitry for Static Random-Access Memories (SRAMs) which focusses on optimizing delay and power. CMOS SRAM cell consumes very less power and have less read and write time. In this project, 6T SRAM cell is implemented with reduced read and write time, delay, and power consumption. It has been noticed often that increased memory capacity increases the bit-line parasitic capacitance which in turn slows down voltage sensing, to avoid this problem use optimized scaling techniques and further, get improve performance of the design.

1.2 Background information about the project work

The project aims to design the peripheral circuitry for a Static Random Access Memory (SRAM) array architecture. The peripheral circuitry is responsible for providing essential support functions to the SRAM array, such as row and column decoders, sense amplifiers, precharge circuits, and write drivers. The design focuses on optimizing speed, power consumption, and area efficiency while ensuring reliable and robust operation. It involves careful consideration of transistor sizing, signal routing, and timing constraints. Through meticulous design and simulation, the project aims to achieve a well-balanced SRAM architecture that meets the performance requirements of modern memory systems.

1.3 Motivation obtained to take up the project work

To design Peripheral Circuitry for SRAM Array Architecture and to measure the performance parameters of the design.

The proposed project was chosen to implement as we were keen to learn and understand the physical design flow of an integrated circuit design. Also study about RAM memory excited us to pursue the project.

And currently, there is an immense demand for integrated chips in the global market because of which there is demand for the human resource in IC design industry, for which our country has taken some measures to bring investments in this industry specifically which further motivated us.

1.4 Problem statement of the project work

The problem statement for the project is to design the peripheral circuitry of an SRAM array architecture. The peripheral circuitry is responsible for providing necessary control signals and functionalities to ensure the proper operation of the SRAM array. The design needs to address various aspects such as read and write operations, row and column decoding, wordline and bitline drivers, sense amplifiers, and timing considerations. The goal is to create an efficient and reliable peripheral circuitry design that maximizes the performance, minimizes power consumption, and ensures the stability and integrity of data storage and retrieval in the SRAM array.

1.5 Objectives of the project work

The main objective of the project work that is undertaken by us under the guidance of our project guide is aimed to design a peripheral circuitry of SRAM array architecture. There are mainly 3 objectives, which is stated below. This objective is achieved by using virtuoso cadence software and Hspice simulator.

The Main objective of the undertaken project is to compare various available Sense Amplifiers and Pre-charge circuits and their effects on the performance of the SRAM.

After selection of the components based on the result, a complete SRAM Block is built by designing the schematic and layout of peripheral circuits namely Row & Column Decoder, Pre- charge Circuit, Sense Amplifier and 6T SRAM Cell.

Consequently, the designed components are analyzed based on their parameters such as R/W, SNM (static noise margin), power dissipated etc.

1.6 Scope of the project work

The project focuses on the design of peripheral circuitry for an SRAM array architecture. This involves developing the necessary support circuitry to enable proper functioning of the SRAM array. The scope includes designing control logic circuits for read and write operations, sense amplifiers for data retrieval, row and column decoders for address decoding, and power supply circuits for reliable operation. Additionally, the project may involve optimizing circuit performance in terms of speed, power consumption, and area utilization. The goal is to create a robust and efficient peripheral circuitry design that enhances the overall functionality and performance of the SRAM array.

1.7 Organization of the project report

The project work undertaken by us is organized in the following sequence as follows.

A brief introduction to the work was presented in the introductory chapter in chapter-1. An exhaustive summary of the relevant works done by the researchers & other authors is presented in the chapter 2 along with the drawbacks of the works done by them. Block diagram and working principle of project work undertaken by us is presented in the chapter – 3. Hardware/ Software tools /Description/Interfacing employed in our project work is depicted in the chapter - 4. Results of the projects is discussed in chapter 5 with detailed analysis.

Finally, the report concludes with the conclusion and future work in chapter –6.

Paper presentations in conferences during the tenure of the Project Work, Paper publications in journals during the tenure of the Project Work, Hard copy of the presented conference paper / published journal paper, Awards, Recognitions in Project Fests, Photographs & any other certificates, Plagiarism Report, CO PO Mapping Sheet, Budget Estimations are presented at the end of the project report one after the other in succession.

Chapter 2

Literature Survey

- Amulya. S, Mr. Manohar B. S, Dr. P M Shivakumara Swamy presented "Low Power, High Performance PMOS Biased Sense Amplifier" in 2022 [1]. In this Journal we could find the analysis and comparison of various sense amplifiers mainly Voltage Sense Amplifier, Current Sense Amplifier and Charge Transfer Sense Amplifier, finally the suitable one was chosen based on the results obtained after simulation.
- Sampath Kumar, Sanjay Kr Singh, Arti Noor, D. S. Chauhan & B.K. Kaushik, "Comparative Study of Different Sense Amplifiers in CMOS Technology" in 2011 [2]. In this paper published at International Journal of Advances in Engineering & Technology the presenters have performed extensive comparison of various available sense amplifiers such as voltage and current controlled sense amplifiers based on their advantages and disadvantages.
- Arvind Kumar Mishra, "Design of Novel Address Decoders and Sense Amplifiers for SRAM Based Memory" in 2014. In this Master's thesis we could see the detailed comparison of hardware implementation of decoders and their performance dependency on this implementation. This enables us to decide which implementation must be followed in order to achieve maximum performance.
- Brandon Hilgers, "SRAM Compiler for Automated Memory Layout Supporting Multiple Transistor Process Technologies" in 2015. This master's thesis has detailed information about various sense amplifier and precharge circuits and how to implement them in the Cadence Layout Tool Suite.

Chapter 3

Project Details

In this chapter, the block diagram, circuit diagram, working principle, software tools utilized, the flow-charts & proposed methodology is presented along with the brief explanations.

3.1 Block diagram of the proposed system

The SRAM Array architecture overview is given in the below block diagrams.

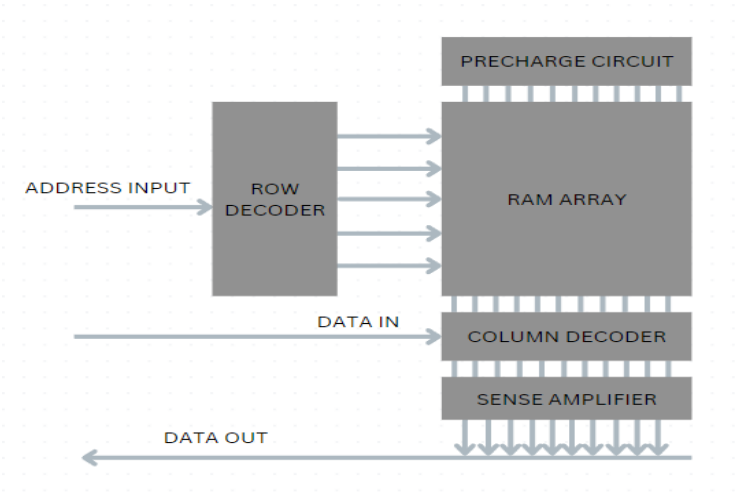


Fig 3. SRAM array architecture

- RAM array: Includes SRAM bit cells which should occupy minimum area to achieve cell density i.e. number of 1bit SRAM cells per unit area should be as high as possible.
- Decoder: Memory cell matrix consists of rows and columns. Each row is accessed through word line while each column is accessed through bit line. Data lines are responsible for transferring data to and from bit lines depending upon write and read operation respectively. Generally, by making word line high entire word is obtained. So, column decoder is used to distinguish among columns.
- Sense Amplifiers: Bit stored in a memory cell is determined by the voltage across bit lines. However, due to large number of cells connected to a column circuitry, it is difficult to get a proper output. Therefore, sense amplifiers are used as it gives stability and reliability to circuitry.

- Pre-charge circuit: Before every read and write operation, pre-charge becomes high and both bit lines are charged to a value Vdd/2. During pre-charge and equalizer cycle, both bit lines are shorted so that voltage difference across them is zero. When pre-charge is off and sense amplifier turns on, it senses small voltage difference between two bit lines and accordingly stores a bit in memory cell.

3.2 Flow-chart / Data Flow Diagram

In this section, methodology that is going to be used in our proposed project work is presented. The memory array is constructed with SRAM cells due to its advantages such as

- Faster than DRAM
- Medium power consumption
- To create speed sensitive cache memory
- Good reliability
- Do not require periodical refreshment circuit

The flow of project work is as follows

Fig 4. Flow-chart of the methodology used

- Comparison - The design flow starts with comparison of various available Sense amplifiers and Precharge circuits. Some of the parameters considered are common mode noise, stability and power consumption.
- Schematic Design – The schematic of single SRAM cell and schematic of 8x8 SRAM 6T memory array at the transistor level will be constructed using cadence virtuoso software.

- Simulation – The design is verified for accuracy by the process of simulation. The outputs of the design in a GUI for ease of verification will be viewed and the operation will be verified.
- Layout Design – The layout of the peripheral circuits and memory cell will be developed from the schematic obtained in the schematic design.
- Post layout Design Verification – DRC verifies whether the given layout satisfies the design rules provided by the fabrication team. DRC checks are nothing but physical checks of spacing rules between metals, minimum width rules, via rules etc. LVS is major check in the physical verification stage. Layout is compared with the schematic for verifying whether their functionality match or not. If matched, the LVS report is clean.

3.3 Software used

The software tools that are going to be used for the project work is

- Cadence
- Hspice

Implementation process

- Cadence Virtuoso Layout Suite is used to implement the steps involved in the process.
- Circuits are implemented using Schematics L Editor.
- Analysis of the schematics are performed using ADE L and HSpice environment.
- Verified schematics are then converted into their layout counterpart using Layout XL Editor.

3.4 Working principle of the proposed system

In this section overall working is explained in detail.

3.4.1 Sense Amplifier designs:

There are two main categories of sense amplifiers Differential sense amplifiers, also known as voltage mode sense amplifiers, and non-differential amplifiers, also known as current mode sense amplifiers. Within the category of voltage sense amplifiers there are both static designs, which are latch based and read the difference between the bitlines

once and hold that output, and dynamic designs, which constantly watch the difference between the bitlines and adjust their output accordingly.

Voltage mode sense amplifiers are connected directly to the bitlines. At the beginning of a read cycle, the bitlines are precharged. As one bitline begins to discharge, the difference between the bitline voltages determines the output logic value that is seen at the output. The performance of voltage mode sense amplifiers depends on the bitline capacitances. The larger the bitline capacitance, the larger the RC time constant of the system, and the larger the delay between enabling the cells and having a large enough difference between the bitlines for a voltage mode sense amplifier to detect the value and show it at the output. If the bitline capacitance is too large and the bitlines cannot be discharged in a reasonable amount of time, current mode amplifiers are sometimes cascaded and used as a buffering stage to disconnect the excessively capacitive bitlines and voltage mode sense amplifier inputs. Because of this, current mode sense amplifiers are often found in large memory arrays that have significantly larger bitline capacitances. Current mode sense amplifiers may also be used independently. The amplifier inputs are connected to the bitlines, and after precharge, the discharging bitline causes a decrease in current flow which is used to determine the output voltage level.

Below are examples of some amplifier types, along with their pros, cons and characteristics.

Types of sense amplifiers:

- Differential voltage sense amplifier
- Basic latched voltage sense amplifier
- Latch based amplifier with pass transistors
- Current controlled latched sense amplifier

1. Differential voltage sense amplifier

The differential sense amplifier is a dynamic voltage mode amplifier. Allegro Microsystems also currently uses this design in their SRAM chips. Below figure shows an example circuit diagram for the differential sense amplifier. The amplifier is composed of a differential pair (Transistors N1 and N2) with an active current mirror load (P1 and P2) and a biasing current source (N3).

The bitlines are connected to the gates of the differential pair transistors and the output is taken from the same side as BL.

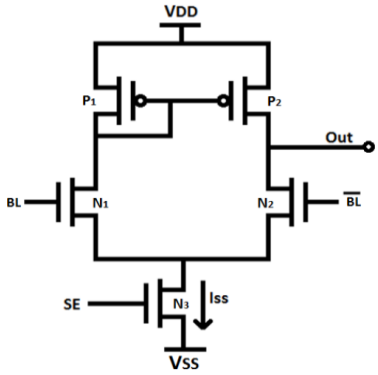


Fig 5. Differential voltage sense amplifier

The differential sense amplifier is commonly used because it is simple and reliable. The sense amplifier may be enabled at the same time as the wordline during a read cycle, making timing requirements for this amplifier very easy. The differential amplifier is resistant to supply noise variations due to its ability to reject common mode voltages; only differences between the inputs are amplified. Any noise that appears on both inputs of the amplifier will not affect the output.

In addition to this, the differential sense amplifier will almost never misread the cell because the output is constantly adjusted depending on the input voltage. A read cycle begins when the signal SE is brought high. This causes a constant biasing current, ISS, to flow through the biasing current source (N3). If both input voltages are exactly equal, this will cause a current equal to ISS/2 to flow through both halves of the amplifier. To ensure that the current is divided equally, the PMOS devices P1 and P2 must be sized identically. The NMOS devices N1 and N2 must also be sized identically.

When the amplifier is first enabled, the input voltages are approximately equal because the bitlines are precharged. After the SRAM cells are enabled, one bitline will begin to discharge. As the bitline discharges, the voltage supplied to the gate of the transistor on that side of the amplifier will decrease, causing the drain current to decrease as the transistor begins to turn off. Because the current source is supplying a total current to the amplifier equal to ISS, the decrease in drain current on one side will cause the current in the opposite side of the amplifier to increase. As the transistor continues to turn off, the output voltage will rise to equal the supply voltage, VDD. A relatively small difference between the bitlines will produce a large difference in output voltages.

In order for the sense amplifier to work properly, the biasing current source must remain on throughout the entire read cycle. If the biasing current stops flowing, a valid value will no longer appear at the output and the amplifier will not function. This constant

current flow causes the device to consume a significant amount of power throughout the entire read cycle.

2. Basic latched sense amplifier

The basic latch based sense amplifier is a static voltage mode sense amplifier. An example schematic for the basic latch based sense amplifier may be seen in Figure 5. There are many variations of the basic latched sense amplifier, but this original design is one of the simplest and reliable choices. The latch mechanism for the sense amplifier is composed of two cross coupled inverters (N1, P1 and N2, P2) which use positive feedback to cause latching behavior. The latched sense amplifiers voltage transfer characteristic curve may be seen in Figure 6. This plot shows that the amplifier has two stable points where VOUT and VOUT are at opposite rails and one metastable state in the middle of the transition region where VOUT and VOUT are at the same voltage.

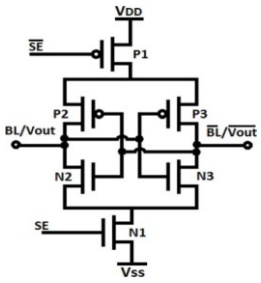


Fig 6. Basic latched sense amplifier

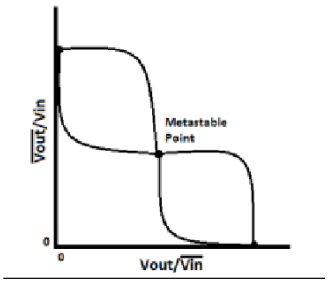


Fig 7. Latch based amplifier VTC

Before a read cycle, the bitlines which are connected to the amplifier inputs are precharged to the supply voltage. If the amplifier were to be turned on right after the precharge stage, there would not be a sufficient voltage difference between the bitlines,

which could cause the amplifier to stay at its metastable point or latch incorrectly. To solve this issue, the bitlines are allowed to discharge until they have created a large enough voltage difference for the sense amplifier to correctly identify the value stored in the memory cell. The discharging bitlines are connected to the inverter inputs, allowing a small bias to develop on the MOSFET gates before the sense amplifier is enabled and the inverters are turned on. To turn on the amplifier, the signal SE is brought high, which turns on the NMOS current source (N3) and the PMOS access transistor (P3). After being enabled, the bias allows the sense amplifier to latch the correct output value.

3. Basic Latch based sense amplifier with pass transistor:

One common variation of the basic latch based sense amplifier includes the addition of pass transistors. Figure 7 This addition effectively decouples the amplifier inputs and outputs from the bitlines. Because the inputs and outputs of the sense amplifier are the same physical node, the sense amplifier will attempt to further discharge the bitlines while it's reading the value stored in the SRAM cell. The pass transistors connect the input and output of the sense amplifier to the bitlines and are active when the sense amplifier is disabled. This allows the bias to still develop on the gates while the sense amplifier is off and the bitlines are discharging.

Once the sense amplifier is enabled, the pass transistors turn off and the bitlines are decoupled from the sense amplifier inputs. Once the amplifier is enabled, the bitlines can no longer discharge. Unlike the amplifier without the pass transistors, this amplifier must account for the voltage drop over the pass transistors. This may lead to issues if one pass transistor is fabricated with a slight sizing error, as it may potentially bias the amplifier towards one logic value.

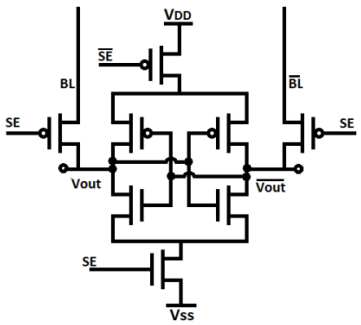


Fig 8. Latch based amplifier with pass transistors

4. Current controlled latched sense amplifier:

Another common voltage sense amplifier is the Current Controlled Latched Sense Amplifier. This design combines aspects from the latch based voltage mode sense amplifier and the differential pair amplifier. An example schematic may be seen below in Figure 8. This design was introduced in 1993 by T. Kobayashi, and is a popular choice in SRAM memory. The amplifier uses the same latch based design as the basic latch based amplifier that was described above in basic latched sense amplifier section, but has the bitlines attached to the gates of transistors N3 and N4. This causes an extremely high impedance to be seen at the input, and the bitlines to be decoupled from the output . The two inverters are made from the MOSFET pairs N1,P1 and N2,P2. When the amplifier is off, the signal SE is at a logic low. This turns on the reset transistors P3 and P4, clearing the previous latched value and holding the latch at its metastable point. The bitline inputs are connected to the gates of MOSFETS N3 and N4.

When the sense amplifier is enabled, the reset transistors turn off, and the current source N5 turns on, causing an even current to flow through each half of the amplifier. The bitline that is discharging causes the gate voltage to drop, which decreases the current flowing through that side of the amplifier and causes the voltage to rise. This will cause the amplifier to latch, which will stop the static flow of current and display a valid value at the output.

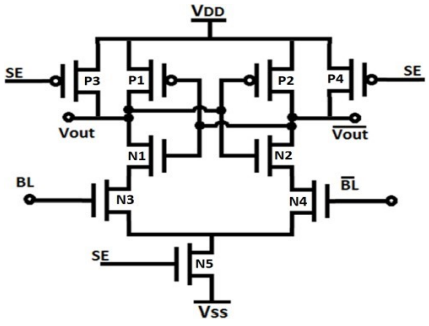


Fig 9. Current controlled latched sense amplifier

3.4.2 Precharge circuits:

Precharge circuits play a crucial role in the operation of Static Random-Access Memory (SRAM) arrays. These circuits are responsible for preparing the bitlines and storage nodes of the SRAM cells before read or write operations. The precharge operation ensures that the memory cells are in a stable state and ready to receive or transmit data.

In an SRAM array, the bitlines are connected to the storage nodes of the memory cells. During the precharge phase, the bitlines are precharged to a predetermined voltage level, typically VDD/2 (half the supply voltage). This voltage level ensures that the bitlines are balanced and ready for subsequent read or write operations.

There are two common types of precharge circuits used in SRAM designs: single-ended precharge and differential precharge.

In a single-ended precharge circuit, a single precharge transistor is used to connect the bitlines to the power supply during the precharge phase. This transistor is controlled by a precharge signal. When the precharge signal is active, the bitlines are connected to the power supply, charging them to the desired voltage level.

In a differential precharge circuit, two precharge transistors are used, one for each bitline. These transistors are controlled by complementary precharge signals. When one precharge signal is active, the corresponding bitline is connected to the power supply, while the other bitline is disconnected or grounded. This approach helps to further enhance the noise margin and improve the stability of the bitlines during precharge.

The precharge circuits should be carefully designed to achieve fast and reliable precharge operations while minimizing power consumption. Additionally, timing considerations must be taken into account to ensure proper coordination with other control signals in the SRAM array. Overall, the efficient design and implementation of precharge circuits are essential for the proper functioning of SRAM arrays in modern digital systems.

Types of pre-charge circuit:

- Diode-connected NMOS pair
- Diode-connected NMOS pair with equalizer
- Diode-connected equalizer with pass transistors
- Equalizer with pass transistors

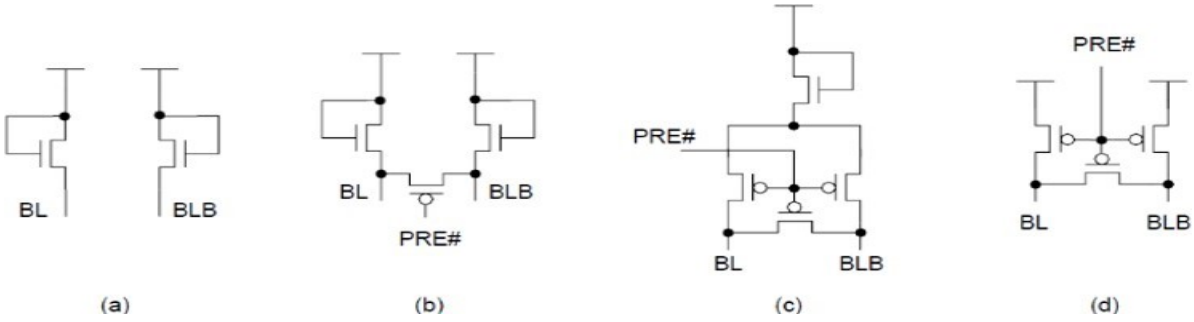


Fig 10. Types of precharge circuits

3.4.3 Static Logic and Dynamic Logic

Types of Logic

1. **Static Logic**

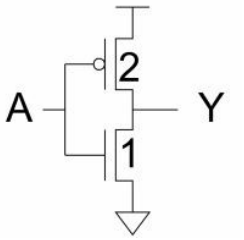


Fig 11. Static Logic Style

- It is one of the most trivial and widely used CMOS logic because of the combination of pull-up and pull-down network and due to its simplicity and the advantages it has.

It is widely used due to following reasons

- Performance is a strong function of fan-in and techniques such as transistor sizing , input reordering and partitioning are implemented to deal with it.
- The speed is linear function of the fan-out.
- Easy implementation using automation tools at logic level
- Robustness against Noise.(High Noise Margin)

2. **Dynamic Logic**

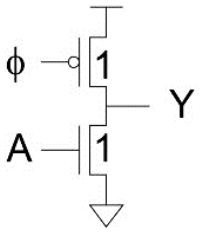


Fig 12. Dynamic Logic Style

- Various types under this category are Ratioed logic, pseudo-NMOS, Domino logic, pass-transistor, DCVSL(Differential Cascode Voltage Switch Logic).
- In our project we are extensively focusing on pseudo-NMOS logic
- The common advantages and disadvantages are
- Substantial reduction in gate complexity.
- But at the expense of static power consumption, asymmetrical response and reduced Noise Margin.

The major differences between Dynamic and static logic style of CMOS implementation is noted below.

Static Logic Style	Dynamic Logic Style
• Robustness against Noise making it trouble free to automate • Relatively consume less power • One of the main disadvantage is, in high-fan-in circuits it turns out to be expensive in terms of are and performance • Number of Transistor required = 2*N • Where n is fan-in	• Simple and fast but at the expense of Reduced Noise Margin Static Power Dissipation • Number of Transistor = N+1 (for pseudo-NMOS)

Table 1 : Difference between static and dynamic logic style

pseudo-NMOS Logic

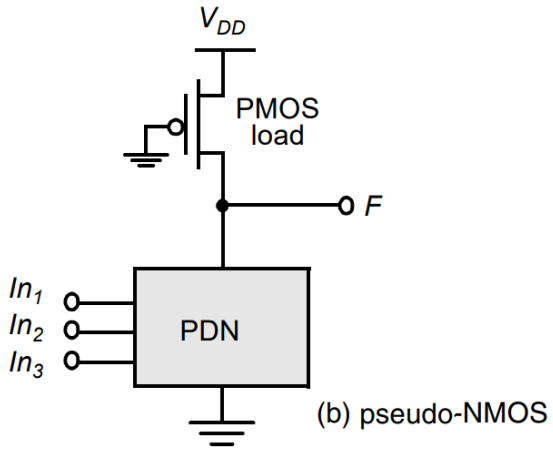


Fig 13. Pseudo-NMOS Logic

- Conventional/static logic is made of both PUN and PDN network, in contrast pseudo-NMOS comprises of only PDN network with a single PMOS transistor.

- The single PMOS is always grounded leading the output F to be always high(VDD). Consequently, the Nominal output high voltage $V_{OH} = V_{DD.}$
- Nominal output low voltage is no equal to 0 as in conventional CMOS due to the fight between PDN and the grounded PMOS and acting as load device.
- As the V_{OL} is not equal to 0, this reduces the Noise Margin and leads to increase in static power dissipation.
- The major disadvantage is, static power dissipation when the output is low because of the direct path between V_{DD} and ground.
- Like in static logic sizing of transistor plays a vital role in determination of the V_{OL} in turn Noise Margin.

$$V_{OL} = \frac{\mu p * Wp}{\mu n * Wn} * V_{DSAT}$$

- The power when the output is 0 is given by

$$P_{low} = V_{DD} * I_{low}$$

- To reduce the V_{OL} as much as possible PMOS should be smaller than NMOS.
- This in turn has negative impact on propagation delay t_{plh} i.e. charging up the node due to less number of holes.

1. Static row decoder:

This type of decoder(circuit) is the traditional type of circuit which is constructed using pull-up network (PMOS) and pull-down network (NMOS) which is called the CMOS technology. And also, in this type of circuits no control signals are used.

2. Dynamic row decoder:

This type of decoder is constructed using only pull-down (NMOS) network with a control signal. Because of this the area consumed by a circuit is reduced by a large extent compared to the Static type of circuits

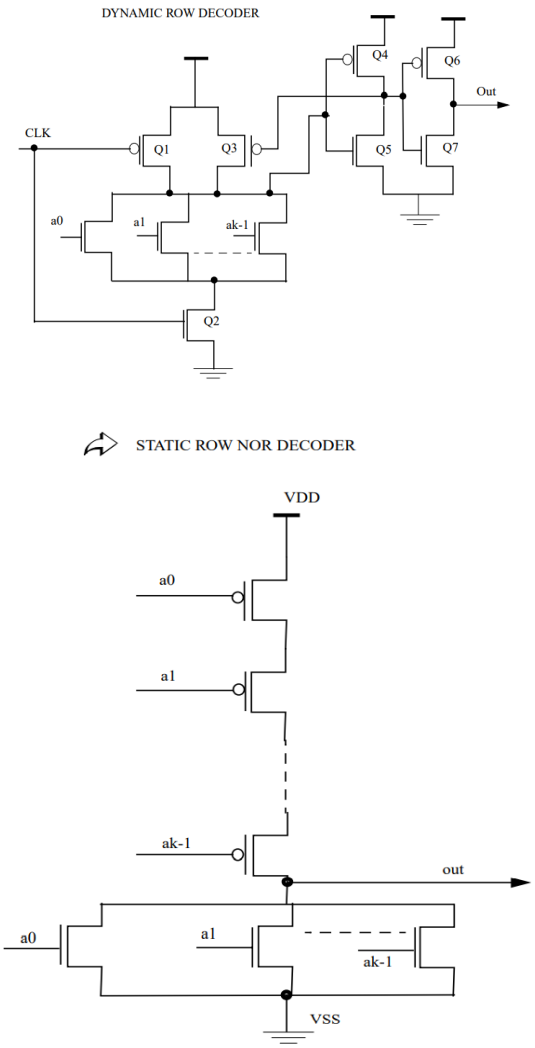


Fig 14. Types of decoders

3.4.4. 6T SRAM

A 6T SRAM cell is a type of static random access memory cell that is widely used in integrated circuits for data storage. It consists of six transistors arranged in a specific configuration to store a single bit of data. Here's an overview of the 6T SRAM cell and its advantages:

Structure of the 6T SRAM Cell:

- Two cross-coupled inverters: The heart of the 6T SRAM cell is formed by two cross-coupled inverters. The state of these inverters represents the stored data (0 or 1).
- Access transistors: The inverters are connected to the bitlines (BL and BL-bar) through two access transistors. These transistors allow read and write operations by controlling the flow of data between the cell and the bitlines.

Advantages of the 6T SRAM Cell:

- Volatile Memory: The 6T SRAM cell is a volatile memory technology, meaning it requires a continuous power supply to retain data. However, it offers several advantages over other types of volatile memory, such as dynamic random access memory (DRAM).
- Fast Access and High Speed: The 6T SRAM cell provides fast access times and high-speed operation. It allows for rapid reading and writing of data due to the direct access path provided by the access transistors, resulting in efficient memory access.
- Non-Destructive Read Operation: One significant advantage of the 6T SRAM cell is its non-destructive read operation. The stored data can be read without altering or destroying the information, allowing for repeated access to the same data without the need for a refresh cycle.
- Bit-level Read and Write: The 6T SRAM cell enables bit-level read and write operations, allowing individual cells to be read or written independently. This flexibility is beneficial in applications where selective read or write operations are required.
- High Stability: The cross-coupled inverters in the 6T SRAM cell provide high stability for storing data. The stored value is maintained as long as power is supplied to the cell, making it suitable for applications where data integrity and reliability are critical.
- Low Power Standby: The 6T SRAM cell has the advantage of low power consumption during standby mode. When not actively accessed, the cell consumes minimal power, contributing to overall energy efficiency in systems.

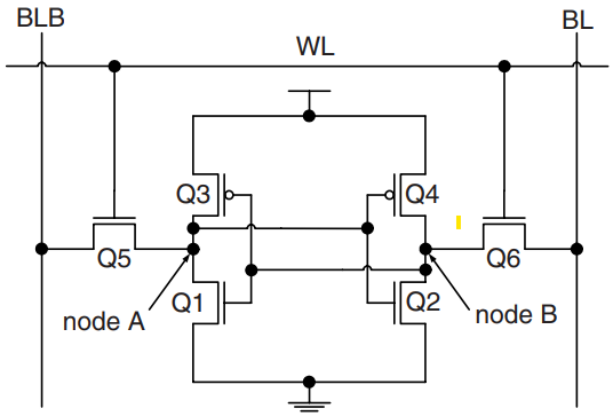


Fig 15. 6T SRAM cell

The 6T SRAM cell supports both read and write operations, allowing for the storage and retrieval of data. Here's a description of the read and write operations in a 6T SRAM cell:

Read Operation:

1. Precharging: Before the read operation, the bitlines (BL and BL-bar) connected to the 6T SRAM cell are precharged to a reference voltage level (typically VDD/2) to ensure a stable baseline voltage.
2. Wordline Activation: The wordline (WL) connected to the access transistors of the targeted SRAM cell is activated, enabling the access transistors to conduct.
3. Data Sensing: As the wordline is activated, the cross-coupled inverters in the SRAM cell start driving the bitlines. The voltage levels on the bitlines are then sensed and amplified by sense amplifiers to determine the stored data. A higher voltage on one bitline (BL) indicates a logic high (1), while a higher voltage on the other bitline (BL-bar) indicates a logic low (0).
4. Data Output: The sensed data is then latched and provided as an output for further processing or use.

Write Operation:

1. Wordline Activation: Similar to the read operation, the wordline (WL) connected to the access transistors of the targeted SRAM cell is activated.
2. Data Input: The desired data (either logic high or logic low) is applied to the bitlines (BL and BL-bar) depending on the value to be written.
3. Bitline Differential: Applying the desired data to the bitlines creates a voltage differential between the bitlines. For example, if the desired data is a logic high, the BL voltage is increased, while the BL-bar voltage is decreased, or vice versa for a logic low.
4. Wordline Transistor Control: The voltage differential on the bitlines controls the conduction of the access transistors connected to the SRAM cell. The access transistors allow the data to be written into the cross-coupled inverters of the cell.
5. Data Storage: The voltage differential on the bitlines causes one of the inverters in the cell to dominate and overwrite the other, storing the new data in the cell.
6. Wordline Deactivation: After the data is written, the wordline is deactivated, isolating the SRAM cell from the bitlines.

Static noise margin:

The stability of SRAM cell is mainly defined by the use of SNM which is the maximum value of DC noise voltage that can be tolerated without changing/flipping the internal storage state of the SRAM. In this paper the graphical approach was used and the value of the SNM will be the length of side of the largest embedded square on the butterfly (VTC) curve.

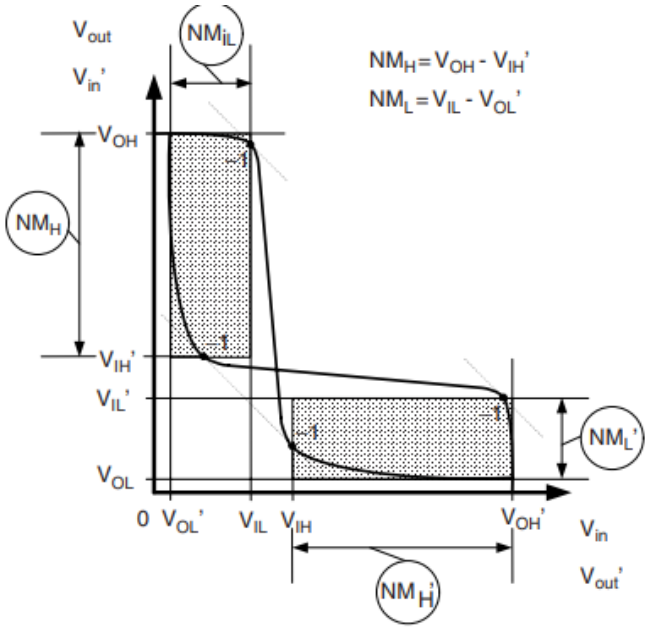


Fig 16. Graphical representation of SNM with V_{OH}, V_{OL}, V_{IH} and V_{IL}.

1) Hold Static Noise Margin
   1. To determine the Hold SNM, the following steps were taking:
   2. Connecting BL and BLB to Vdd.
   3. Connecting WL to gnd.
   4. Plotting both VTCs of the inverter 1 and inverter 2 on the same graph.
   5. Finding the maximum square SRAM that can fit into the VTC lobe.
   6. The SNM is the side of the maximum square.

2) Read Static Noise Margin (RSNM)
   1. Connecting BL and BLB to Vdd;
   2. Connecting WL to Vdd;
   3. Using graphical method, the SNM is the side of the maximum square.

3) Write Static Noise Margin (WSNM)
   1. Connecting BL to gnd and BLB to Vdd ;
   2. Connecting WL to Vdd ;
   3. Using graphical method, the SNM is the side of the minimum square.

Overall Conclusions of the Chapter 3

Types of peripheral circuits and the standard 6T SRAM cell structures are explained in detail and their schematics and layouts has been implemented in the cadence Virtuoso tool suite to proceed with the simulations and verification.

Chapter-4

Tools used & Methodology

4.1 Tools used

Cadence, Hspice

4.2 Methodology

The flow of project work is as follows

Fig 17: Flow chart of the methodology used

- **Comparison –** The design flow starts with comparison of various available Sense amplifiers and precharge circuits.
- **Schematic design –** The schematic of single SRAM cell and schematic of 8×8 SRAM 6T memory array at the transistor level will be constructed using Cadence virtuoso software.
- **Simulation -** The design is verified for accuracy by the process of simulation. The outputs of the design in a GUI for ease of verification will be viewed and the operation will be verified.
- **Layout design -** The layout of the peripheral circuits and memory cell will be developed from the schematic obtained in the schematic design.
- **Post layout design verification -** DRC verifies whether the given layout satisfies the design rules provided by the fabrication team. DRC checks are nothing but physical checks of spacing rules between metals, minimum width rules, via rules etc. LVS is a major check in the physical verification stage. Layout is co mpared with the schematic for verifying whether their functionally match or not. If match, then the LVS reports clean.

4.3 Implementation process

- Cadence Virtuoso Layout Suite is used to implement the steps involved in the process.
- Circuits are implemented using Schematics L Editor.
- Analysis of the schematics are performed using ADE L and HSpice environment.
- Verified schematics are then converted into their layout counterpart using Layout XL Editor.
- Finally signoff checks like DRC and LVS are accomplished.

Chapter-5

Results and Discussions

5.1 Simulation Results

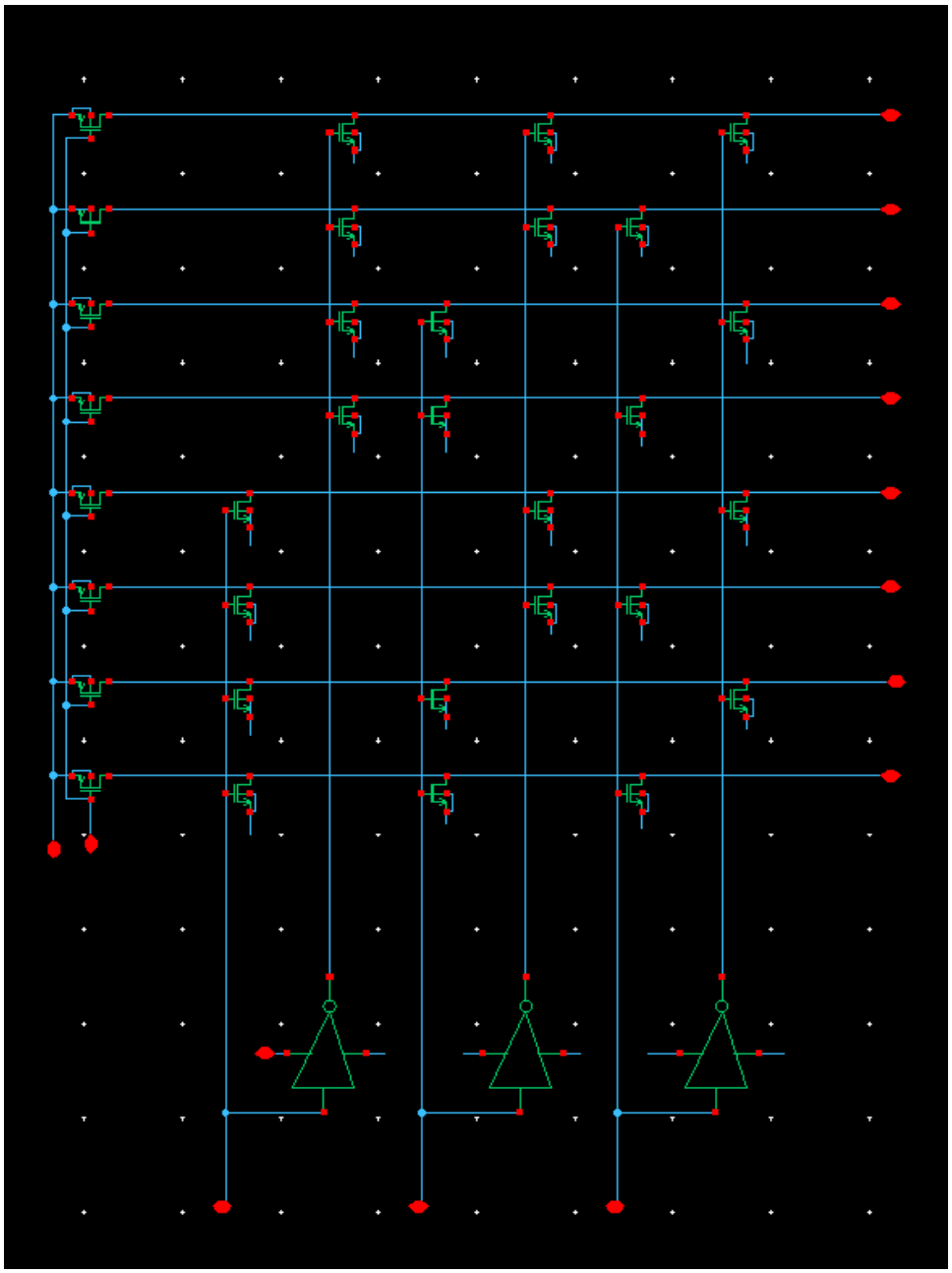


Fig 18: Dynamic decoder schematic

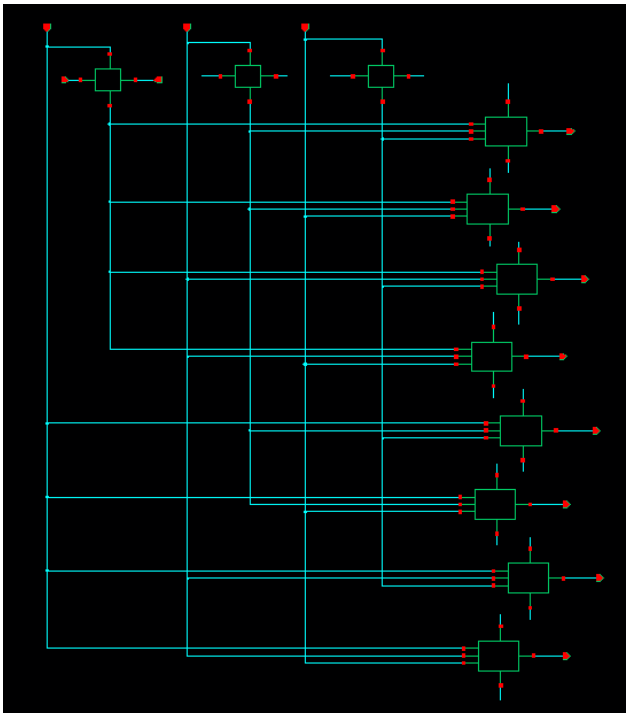


Fig 19: Static decoder schematic

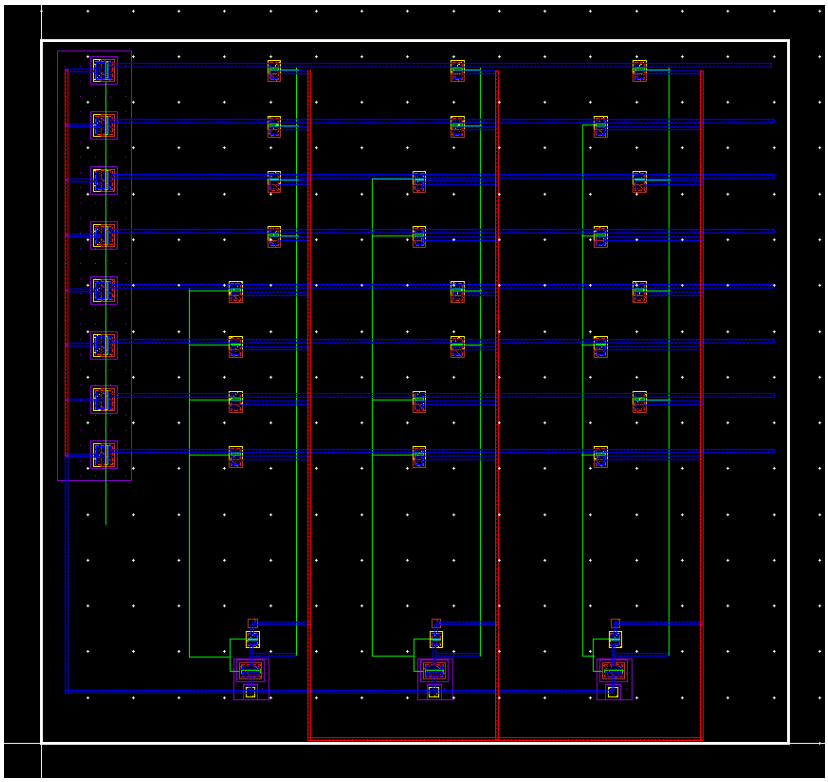


Fig 20: Dynamic decoder layout

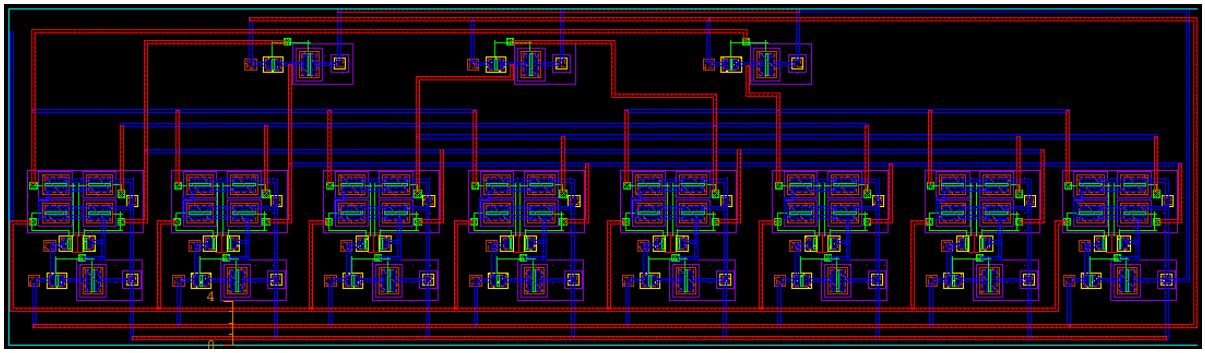
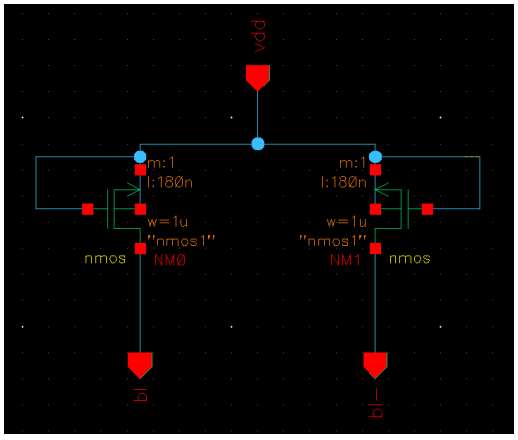


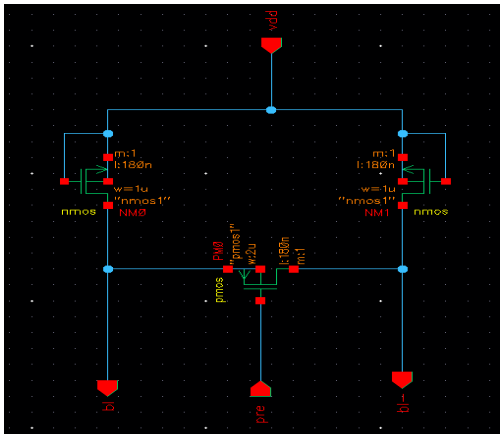
Fig 21: Static decoder layout

Parameter	Static Decoder	Dynamic Decoder
Average power consumption	93.6697µW	5.74449mW
Rise time	53.8395ps	10.0589ns
Fall time	27.5493ps	61.3406ps
Number of transistors	70	46
Area	3236.709 µm²	6,258.96 µm ²

Table 2: Simulation results of Static & Dynamic decoders



(a)



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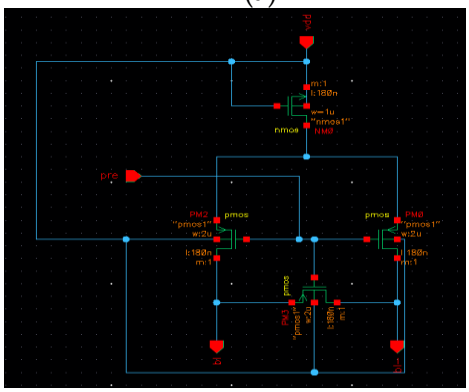

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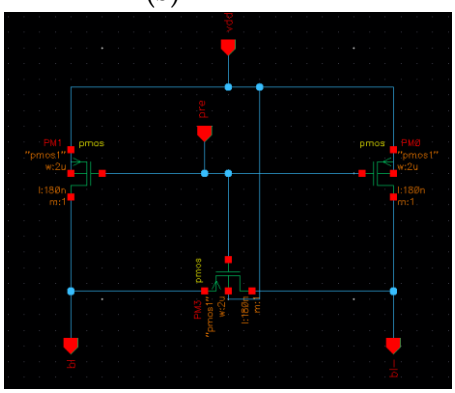


(d)

Fig 22: Schematics of (a) Diode-connected NMOS pair (b) Diode-connected NMOS pair with equalizer (c) Diode-connected equalizer with pass transistors (d) Equalizer with pass transistors

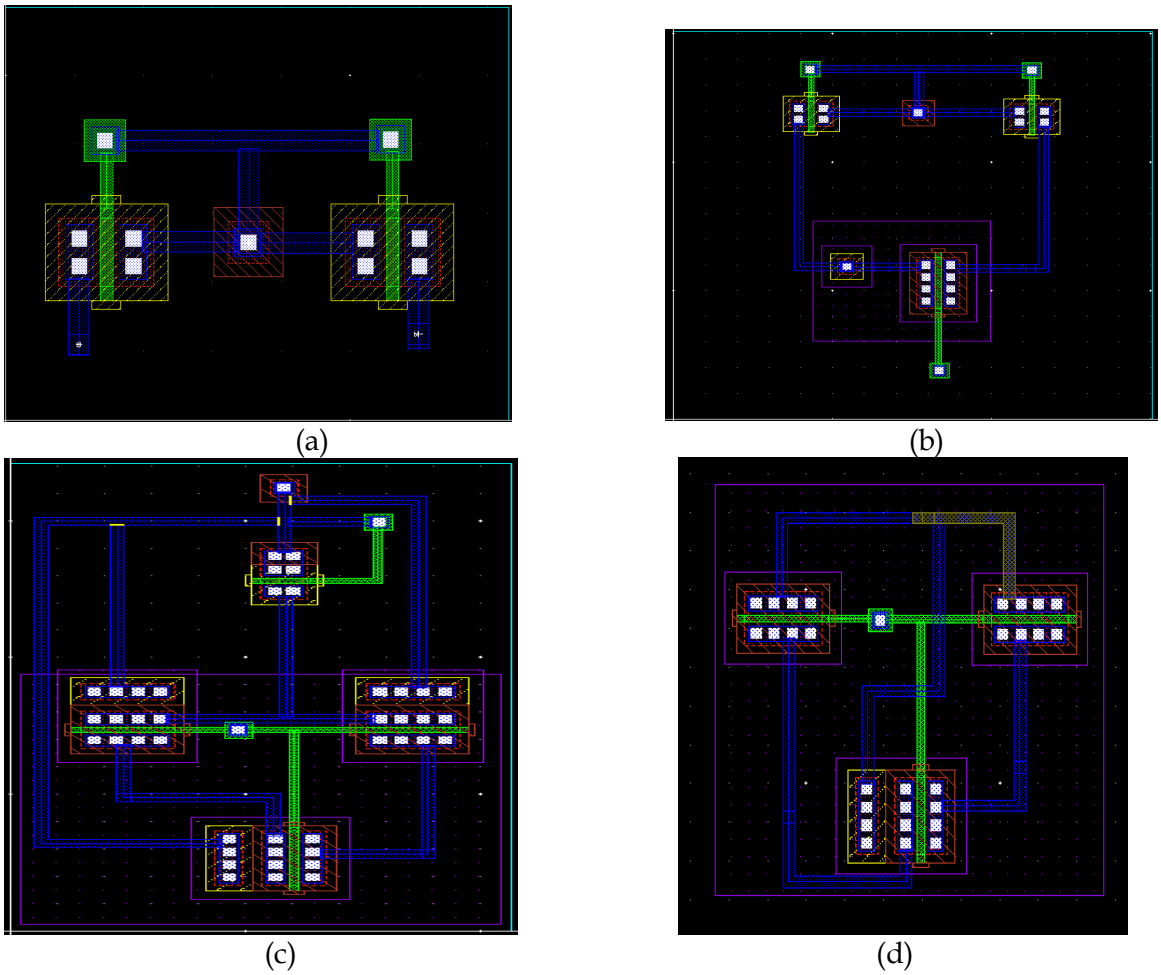
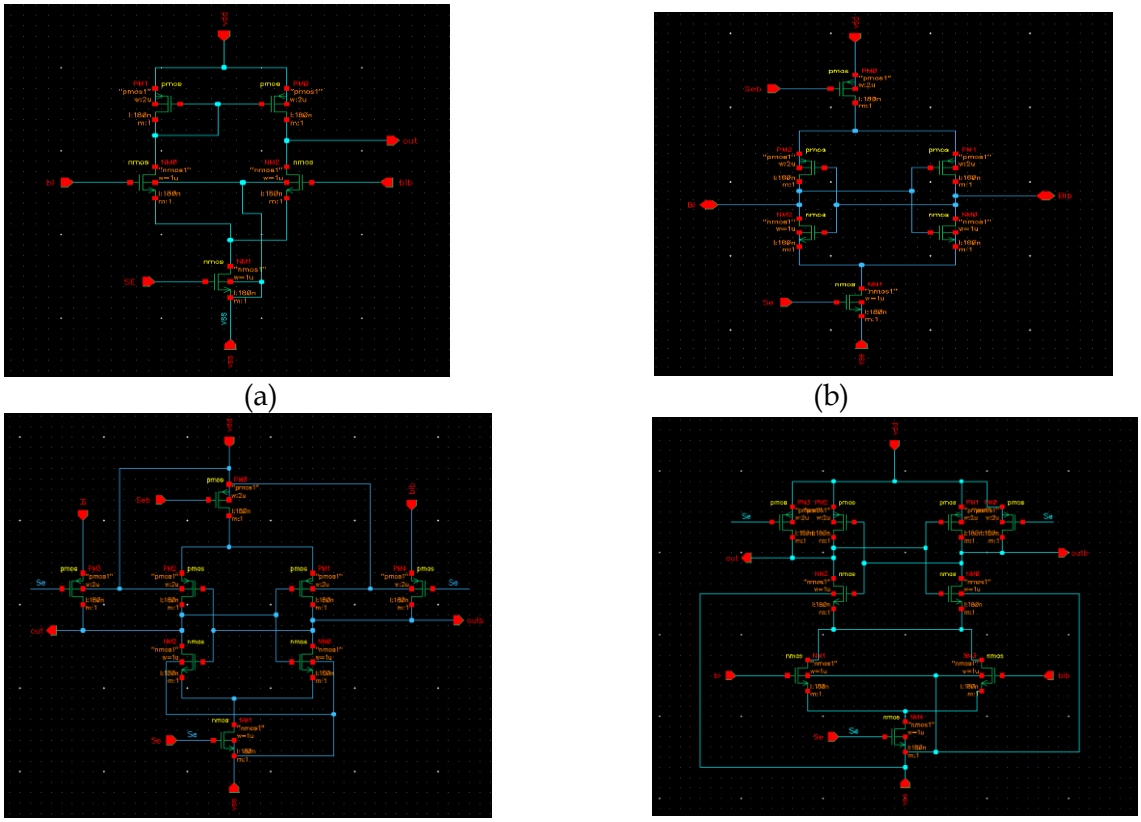


Fig 23: Layouts of (a) Diode-connected NMOS pair (b) Diode-connected NMOS pair with equalizer (c) Diode-connected equalizer with pass transistors (d) Equalizer with pass transistors

Parameter	Diode-connected MOS pair	Diode-connected NMOS pair with equalizer	Diode-connected equalizer with pass transistors	Equalizer with pass transistors
Average power consumption	3.2873×10^{-27} W	4.709pW	48.844nW	87.94pnW
Rise time	80ps	72.015ps	13.576ps	62.296ps
Fall time	80ps	72.084ps	153.752ps	23.707ps
Number of transistors	2	3	4	3

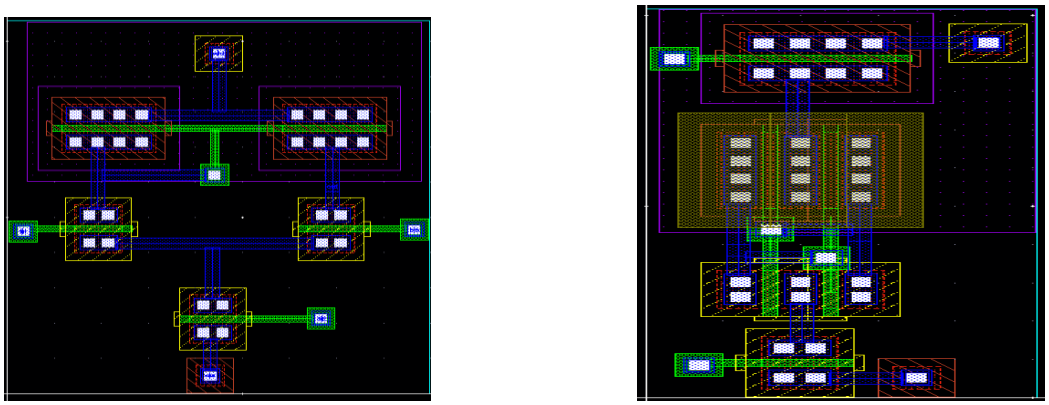
Table 3: Simulation results of Pre-charge circuits



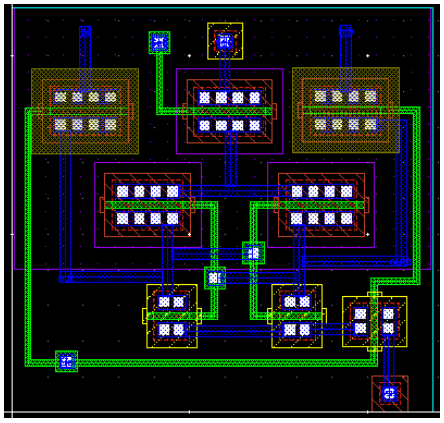
(a) (b)

(c) (d)

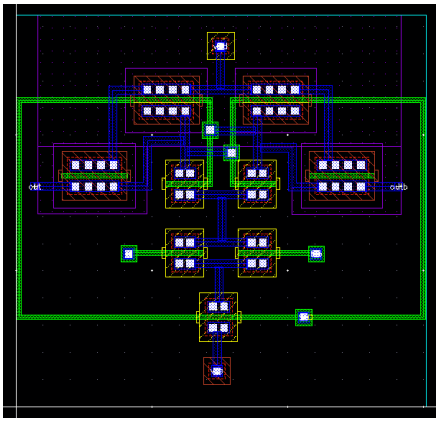
Fig 24: Schematics of (a) Differential voltage sense (b) Basic latched voltage sense amplifier (c) Latch based amplifier with pass transistors (d) Current controlled latched sense amplifier



(a) (b)



(c)

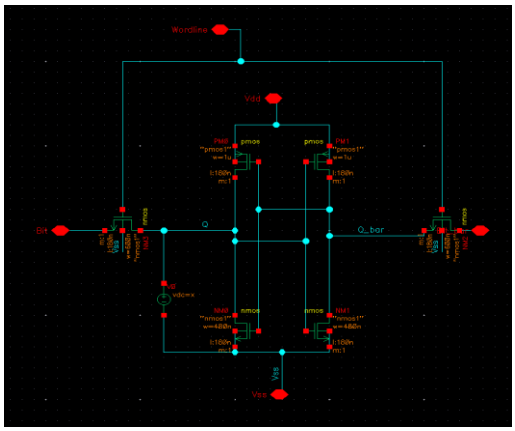


(d)

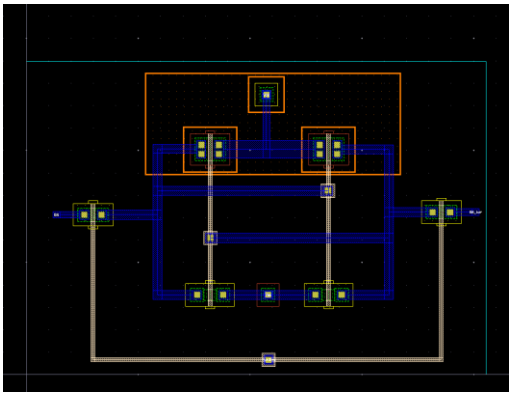
Fig 25: Layouts of (a) Differential voltage sense (b) Basic latched voltage sense amplifier (c) Latch based amplifier with pass transistors (d) Current controlled latched sense amplifier

Parameter	Differential sense amplifier	Latch based sense amplifier	Latch based sense amplifier pass	Current controlled voltage sense amplifier
Average power consumption	66.33 µW	162.52µW	24.356 µW	82.982 µW
Rise time	176.844ps	800fs	227.86ps	19.99ns
Fall time	203.62ps	800fs	91.572ps	448.614ps
Number of transistors	5	6	8	9
Area	64.955 µm²	71.345 µm²	134.5 µm²	217.66 µm²

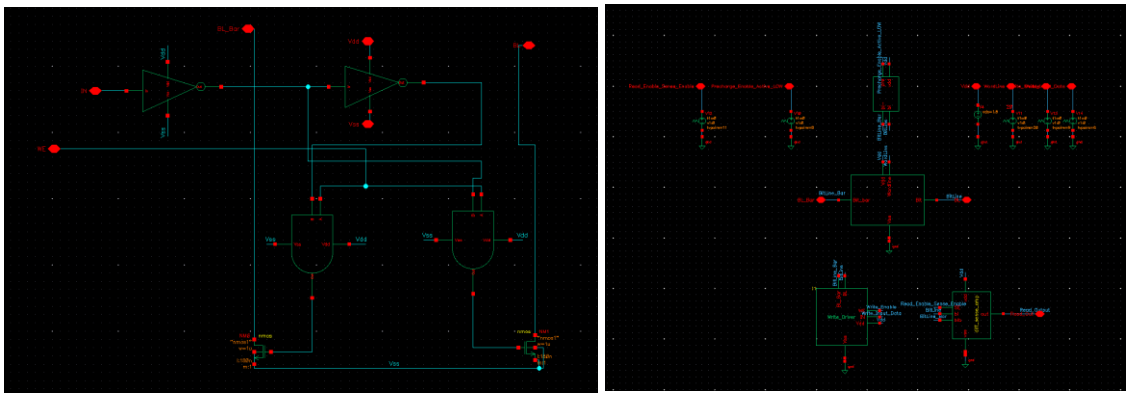
Table 4: Simulation results of sense amplifier circuits



(a)



(b)



(c) (d)

Fig 26: (a) Schematic of 6T SRAM cell (b) Layout of 6T SRAM cell (c) Schematic of write driver (d) Schematic of SRAM cell along with peripheral circuitry

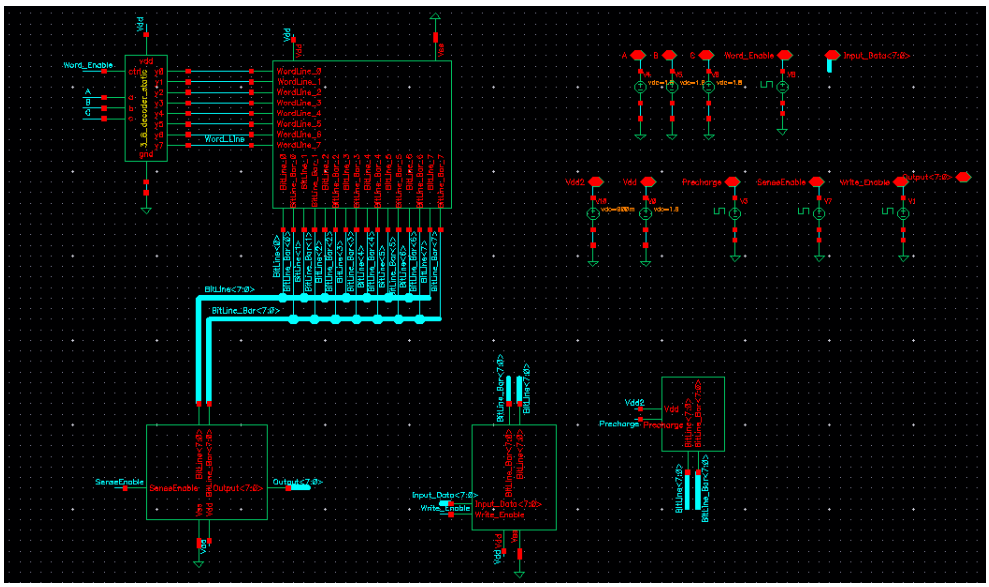


Fig 27: Schematic of 6T SRAM block with peripheral circuits

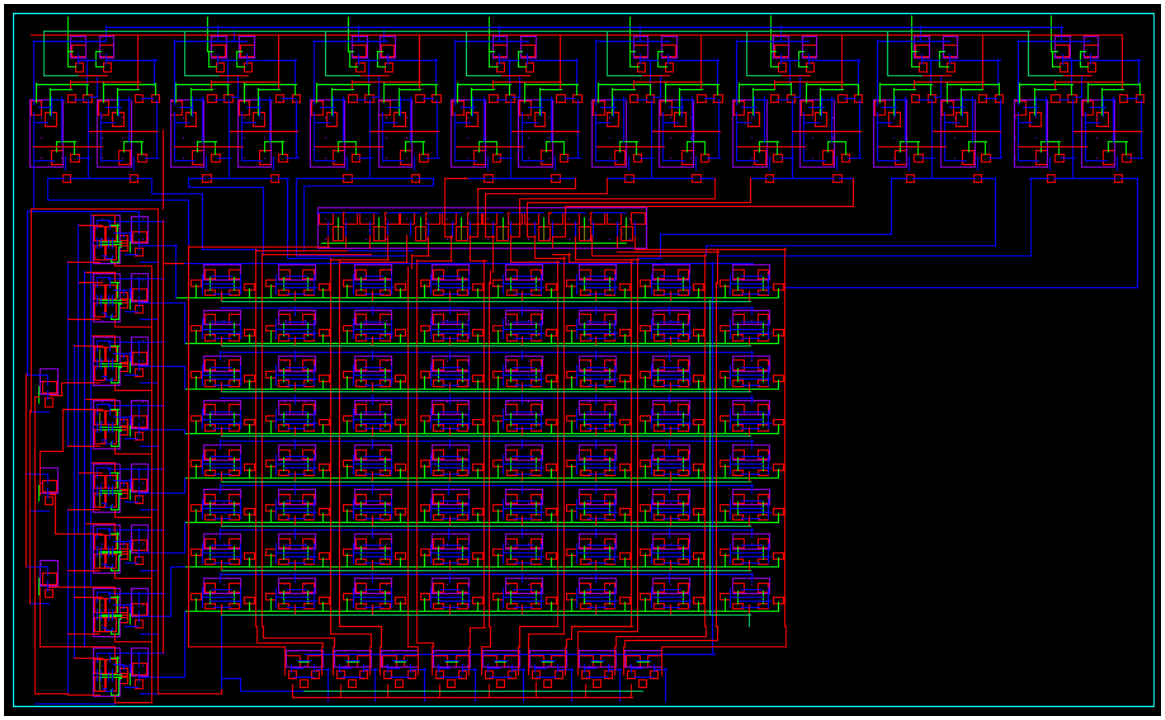


Fig 28: Layout of 6T SRAM block with peripheral circuits

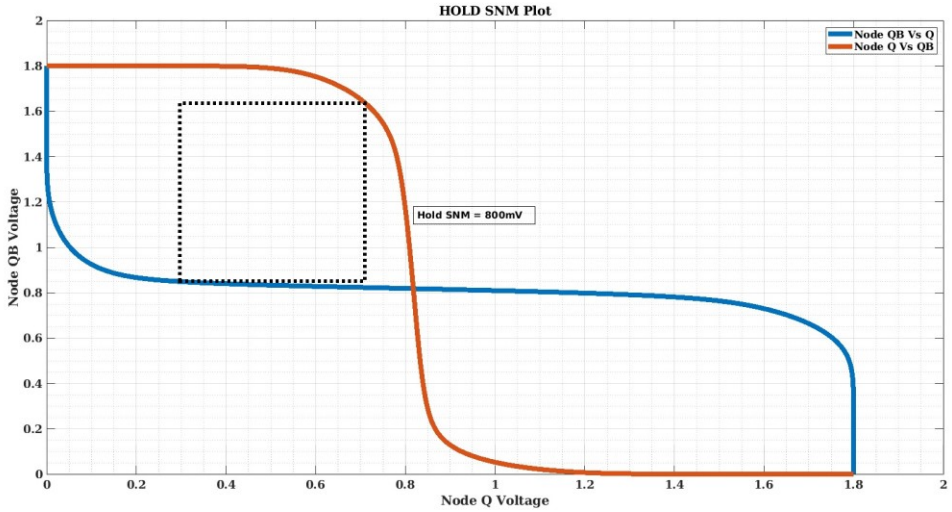


Fig 29. SRAM Hold SNM Plot

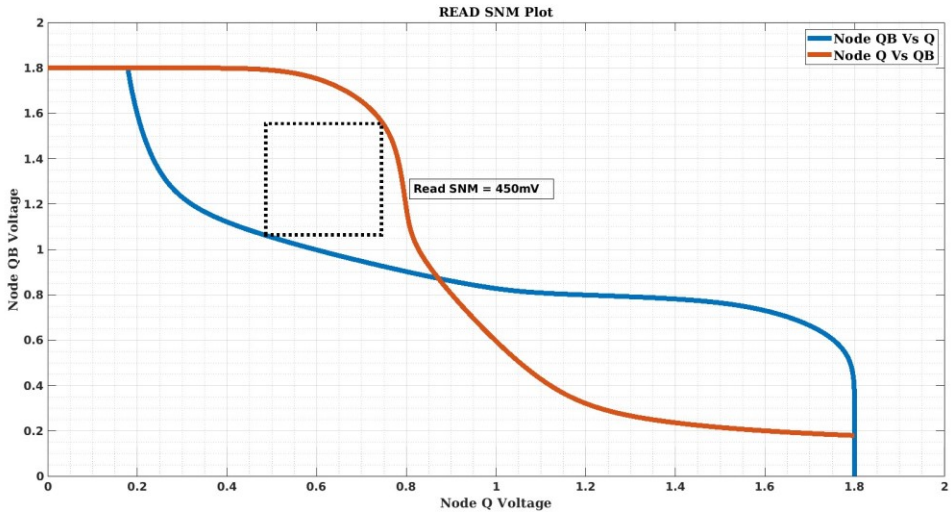


Fig 30. SRAM Read SNM Plot

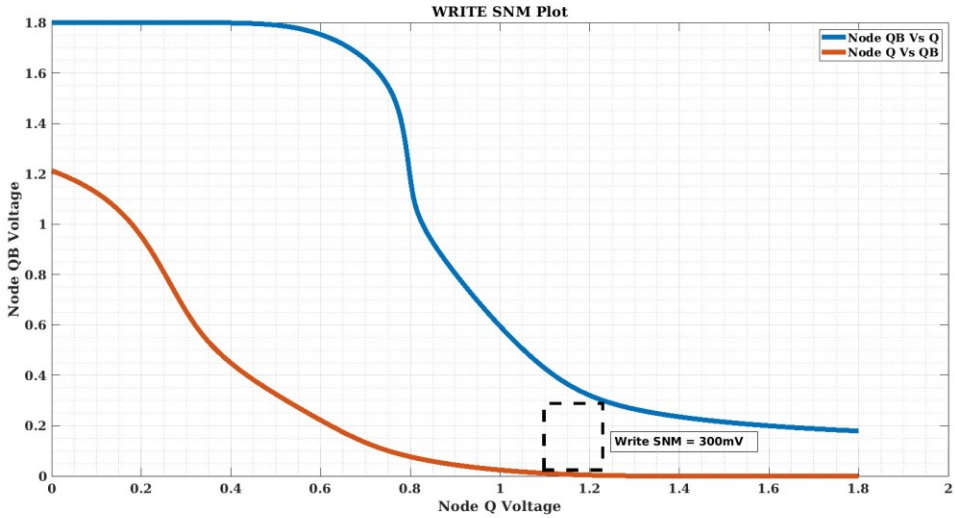


Fig 31. SRAM Write SNM Plot

5.2 Experimental Results

From the comparison of the peripheral circuits we were able to select appropriate circuits in designing the SRAM block such as static decoder which is better in all parameters, differential amplifier which is better in area, power and propagation delay, & equalizer with pass transistor precharge circuit is better in controlling and propagation delay.

5.3 Applications, Advantages, Limitations

Applications:

- Computer Cache Memory
- Microprocessors
- CPU register file
- Routers
- Digital Cameras
- Cell phones

Advantages:

- No require periodically refreshment circuit.
- Less power consumption than DRAM
- Great Performance to DRAM
- Good reliability compare to Dynamic RAM
- Less idle time during power consumption
- It is used as cache memory in computer systems

5.3 Conclusions of the chapter-5

Selection of the peripheral circuits based on the parameters considered have been selected for designing the SRAM block and the applications & advantages are mentioned.

Chapter-6

Conclusions, Future Work & Scope of Project

Conclusions

In conclusion, the design of peripheral circuitry for SRAM array architecture plays a crucial role in achieving optimal performance and reliability. Several performance parameters have been considered throughout the design process to ensure the efficient operation of the SRAM array.

Firstly, the read and write access times have been carefully optimized. By implementing appropriate read and write circuitry, the access times of the SRAM cells have been minimized, allowing for faster data retrieval and storage. This ensures that the SRAM array can operate at high speeds, meeting the requirements of modern computing systems.

Additionally, the power consumption of the peripheral circuitry has been taken into account. Low-power design techniques, such as voltage scaling and power gating, have been employed to reduce power dissipation without compromising the performance of the SRAM array. This enables energy-efficient operation, which is essential for portable devices and battery-powered applications.

Furthermore, the stability and robustness of the SRAM array have been addressed. Noise immunity measures, such as shielded interconnects and differential sensing techniques, have been implemented to minimize the impact of noise and interference on the stored data. Moreover, error detection and correction mechanisms, such as parity or ECC (Error Correction Code), have been integrated into the peripheral circuitry to enhance the reliability of the SRAM array.

Another critical aspect considered in the design is the area efficiency. By employing compact circuit layouts, utilizing shared resources, and optimizing the placement of components, the overall footprint of the peripheral circuitry has been minimized. This not only saves valuable chip area but also allows for higher memory density, enabling larger SRAM arrays in a given chip size.

Lastly, the manufacturability and yield of the SRAM array have been taken into consideration. Design for manufacturability (DFM) guidelines, such as proper spacing and layout rules, have been followed to ensure that the circuitry can be fabricated accurately and reliably. This helps in achieving high production yields and reduces the likelihood of manufacturing defects.

Scope for future works in this domain

The future scope of the project lies in further enhancing the performance, efficiency, and reliability of SRAM arrays. This can be achieved through various avenues, including:

- Advanced circuit techniques: Exploring and implementing novel circuit techniques such as assist circuits, voltage regulators, and advanced sensing schemes to improve access time, reduce power consumption, and enhance stability.
- Non-volatile SRAM: Investigating the integration of non-volatile memory elements, such as spintronic or resistive RAM, into the SRAM array architecture to combine the benefits of high-speed volatile memory with non-volatility.
- Emerging memory technologies: Exploring and adapting emerging memory technologies like phase-change memory (PCM), magnetic RAM (MRAM), or ferroelectric RAM (FeRAM) as potential alternatives to conventional SRAM, aiming for higher density, lower power, and increased scalability.
- Design optimization: Continuously optimizing the peripheral circuitry layout, interconnect design, and placement strategies to further improve area efficiency and reduce signal delay, enabling larger SRAM arrays with improved performance.
- Reliability enhancements: Developing robust error correction techniques, fault tolerance mechanisms, and mitigation strategies to address reliability challenges such as soft errors, aging effects, and process variations.
- System integration: Considering the integration of SRAM arrays with other system components, such as processors and cache hierarchies, to optimize the overall system performance, power efficiency, and memory hierarchy design.

Outcome of the project works

The outcome of the project focused on the design of peripheral circuitry for SRAM array architecture is a high-performance and reliable SRAM array that meets the demanding

requirements of modern computing systems. Through careful optimization of access times, power consumption, stability, area efficiency, and manufacturability, the designed SRAM array demonstrates improved data retrieval and storage speeds, reduced power consumption, enhanced noise immunity, compact circuit layout, and high production yield. The project's outcome ensures that the SRAM array performs efficiently, providing reliable data storage and retrieval capabilities, making it suitable for a wide range of applications in the field of memory systems and computing.

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Paper Presented / Publications related to the Project Work in Conferences & in Journals

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G S, Bhargav*; S P, Chandan ; Srinivas, Chandan; Eshwar A, Kuber ; P, Vimala

for presenting the paper titled

Comparative Analysis of Decoder using Static & Dynamic CMOS Logic

at the ***IEEE International Conference on Advances in Electronics, Communication, Computing and Intelligent Information Systems (ICAECIS-23)***

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Hard copy of the presented conference paper / published journal paper

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Comparative Analysis of Decoder using Static & Dynamic CMOS Logic

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***Abstract*— Address Decoders are trivial yet essential element of a digital block, that can consume considerable amount of area on an IC and power during the read and write cycle. The undertaken project aims at designing, comparing and analyzing the performance of 3:8 Static and Dynamic decoder. The design of Static and Dynamic decoder is carried out using technology node 180nm (gpdk180) and Cadence Virtuoso Tool Suite. Furthermore, this paper will provide a detailed comparison of Static and Dynamic decoder including post-layout simulation. In conclusion, the most efficient decoder among the two is concluded based on the parameters such as power dissipation, delay (rise time and fall time) and area based on post-layout simulation results.**

Keywords*— static decoder, dynamic decoder, Cadence virtuoso, gpdk180, rise and fall time.

I. INTRODUCTION

Due to their low power consumption, broad dynamic range, excellent reliability, compact design, and low price, CMOS circuits are now the industry standard for digital design [1-4]. It is crucial for the circuit designer to consider speed, power consumption, and area into account while choosing digital components for a design. Decoders are an essential component in digital circuit design, and they play a crucial role in converting encoded information into a form that can be easily understood and processed by a system [5-8]. Two commonly used types of decoders are static and dynamic decoders[9-11].

In this paper, we will provide a comprehensive comparison of 3:8 static and dynamic decoders, highlighting their key differences and similarities, as well as their respective advantages and disadvantages. We will examine the design and implementation of 3:8 static and dynamic decoders, as well as their performance characteristics such as speed, power consumption, and area requirements. Furthermore, we will discuss the various applications of static and dynamic decoders and provide insights into the trade-offs between these two types of decoders. Our goal is to provide a comprehensive understanding of the pros and cons of static and dynamic decoders, and to help digital circuit designers make informed decisions when choosing between these two types of decoders.

II. TYPES OF CMOS LOGIC CIRCUITS

A. Static CMOS circuit

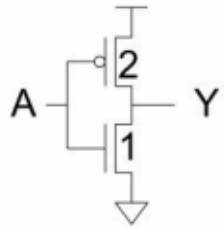

Fig. 1. Static CMOS circuit diagram

Static CMOS circuits use complementary nMOS pulldown and pMOS pullup networks to implement logic gates or logic functions in integrated circuits.

B. Dynamic CMOS circuit

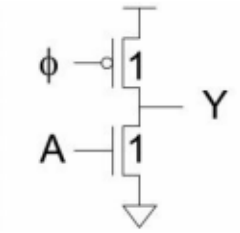

Fig. 2. Dynamic CMOS circuit diagram

Dynamic gates use a clocked pMOS pullup. The implemented logic function or the logic gate is achieved through 2 modes of operation: Precharge and Evaluate.

III. METHODOLOGY

The implementation flow for the decoders is given in fig.3. First, the schematics of 3:8 static and dynamic decoders are designed using 180nm transistor technology in cadence virtuoso tool. The pre layout simulation is carried out in spectre platform to verify the functionality and measure the performance of the decoder circuits. After simulation is

successful, the physical implementation of the decoders is designed in the Cadence layout XL tool. Once the layout of the decoders are completed, the simulation is carried out again with parasitic Resistances & Capacitances and functionality is verified. Once post layout simulation is completed, we would compare the power dissipation, delay time and area of both the decoders.

Fig. 3. Methodology flow of decoder designs

IV. WORKING

Even though the outputs of both decoders are same for any particular input, they are designed differently where one uses standard CMOS technology and another doesn't. And also, one uses clock(control) signal and another doesn't. The truth table of 3:8 decoder is shown in fig.4.

Their designing depends on the Boolean expressions for each output because of which truth table is necessary. Their working can be explained using their schematic designs which were designed using the Boolean expressions.

A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Fig. 4. Truth table of 3:8 decoder

A. Static Decoder

Static decoder is designed with standard CMOS technology, where number of PMOS(pull-up) transistors are equal to number of NMOS(pull-down) transistors in the circuit. Here, decoder is designed using the Boolean expression for every output in the truth table. And there is no clock signal involved in the design which makes the decoder static i.e. output is dependent on only input.

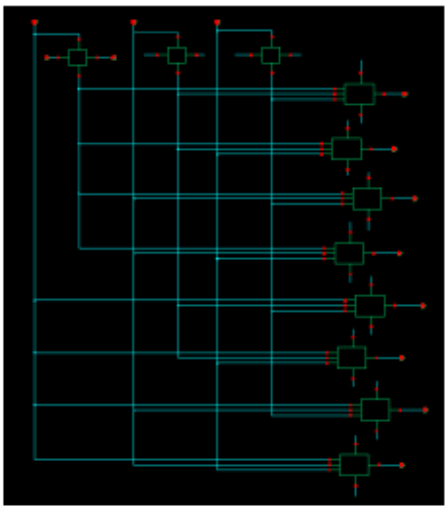

Fig. 5. 3:8 Static decoder schematic

From Fig. 3, We see that every output pins of decoder is connected to the output of an AND gate with its input pins connected to decoder input pins according to the Boolean expression of each output. To satisfy the negations of inputs in any Boolean equation, each input is inverted using an inverter as shown in Fig. 5.

B. Dynamic Decoder

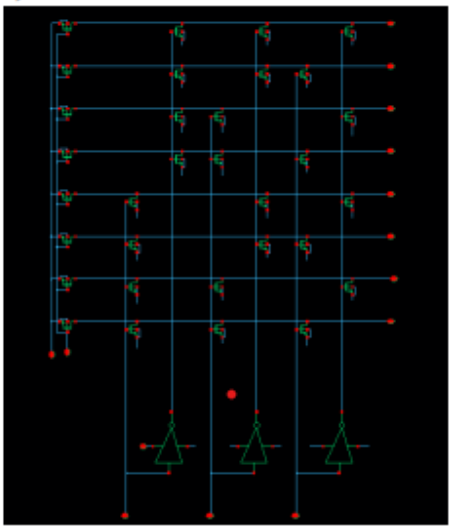

Fig. 6. 3:8 Dynamic decoder schematic

Dynamic decoder is designed prominently with NMOS transistors according to the Boolean expressions from the

truth table with only one PMOS transistor connected to the NMOS(pull-down) network & a clock signal controlling the circuit operations. This decoder is dynamic because the outputs depend on both the inputs & the clock signal.

From Fig. 6. We see that for every output there is single PMOS transistor where their gate terminals are connected to clock signal to control decoder output. And every output of decoder is designed prominently using NMOS transistors according to the Boolean expression of outputs & inverters are used to negate the input signals to satisfy the Boolean equations.

V. Results and Discussion

As discussed in the methodology, the implementation was carried using Cadence virtuoso tool. Fig.7 and fig.11 shows the power dissipation and transient analysis of static decoder and dynamic decoder respectively. The transient analysis is verified using the truth table shown in fig.3. The biggest issues with high-performance transistor technology are power dissipation and delay time. The frequency of operation is directly related to the power dissipation and delay time. Therefore, a chip shouldn't operate at a higher speed than is required. For the design to work effectively, it is essential to select low power consumption and less delay as design component.

To calculate the actual delay time and power consumption of the digital component the pre and post layout simulation need to be performed. The pre- layout and post - layout simulation for static decoder Fig.8 and Fig. 9. Similarly for the dynamic decoder pre- layout and post - layout simulation is shown in Fig.12 and Fig.13 respectively. To determine the actual performance of the digital component, back annotation is important. Back annotated graph for Static decoder is given in fig. 10 and dynamic decoder is given in fig.14.

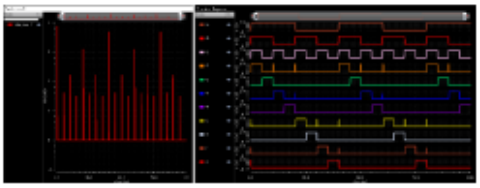

Fig. 7. 3:8 Static decoder power dissipation & transient analysis

10	Avg_power	61.3291u	✔
11	rise_time	42.2617p	✔
12	fall_time	17.2015p	✔

Fig. 8. Pre-layout simulation of static decoder

10	Avg_power	93.6697u	✔
11	rise_time	53.8395p	✔
12	fall_time	27.5493p	✔

Fig. 9. Post-layout simulation of static decoder

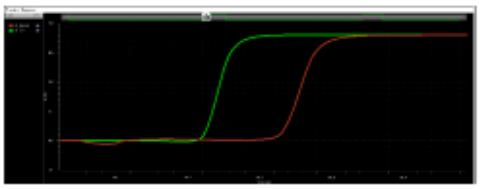

Fig. 10. Back annotated graph of Static decoder

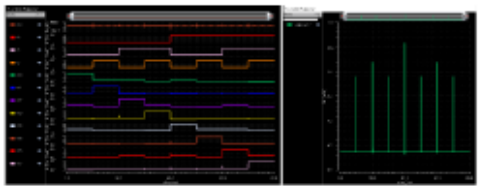

Fig. 11. 3:8 Dynamic decoder transient analysis & power dissipation

10	Avg_power	5.7426m	✔
11	rise_time	50.5834p	✔
12	fall_time	10.0458n	✔

Fig. 12. Pre-layout simulation of dynamic decoder

10	Avg_power	5.74648m	✔
11	rise_time	93.9734p	✔
12	fall_time	10.0779n	✔

Fig. 13. Post-layout simulation of dynamic decoder

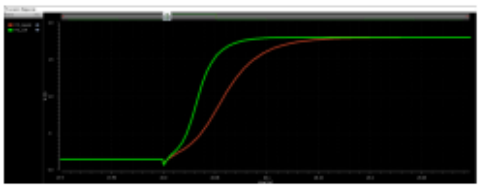

Fig. 14. Back annotated graph of Dynamic decoder

TABLE I. STATIC & DYNAMIC DECODER COMPARISON

Parameters Considered	Post-Layout Simulation Results	
	Static Decoder	*Dynamic Decoder*
Dynamic Power	93.669uW	5.746mW
Rise Time Delay	53.8395ps	93.9734ps
Fall Time Delay	27.5493ps	10.077ns
No. of transistors	70	46
Area Consumed	18,929.49 μm^2	6,258.96 μm^2

The designed decoders are simulated using the ADE L environment of the cadence tool suite and the obtained values are tabulated in table-1. The Table I depicts various performance parameters after performing post layout simulation and based on the values of number of transistors and area consumed, dynamic decoder has an upper hand but

when delay and area is considered static decoder is found to be better.

VI. CONCLUSION

Trade-offs between various parameters are made while designing an integrated circuit. These trade-offs are made based on the design requirements such as area reduction, power consumption reduction or delay reduction. Similarly static and dynamic decoders are designed and compared based on essential parameters namely, average power consumption, delay time, number of transistors and area consumed. A detailed post-layout simulation is carried out considering the parasitic resistances and capacitances of the various metal and polysilicon layers involved. Based on the simulation result the static decoder consumes less power about 90% less dynamic power and the rise time about 40ps lesser. Similarly, the fall time is reduced by about 90ns. But the area consumed is 3 times lesser and transistors used is about 40% less.

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CO-PO Mapping Justification Sheets

Justification of PO-PSO mapping

Project Title		Design of Peripheral Circuitry for SRAM Array Architecture
PO ↓	Levels 3/2/1	Justification
PO1	2	Application of the knowledge of mathematics, engineering fundamentals to the solution of complex engineering problems.
PO2	3	Identification, formulation and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics.
PO3	2	Designing of system components or processes that meet the specified needs with appropriate consideration for the public safety.
PO4	3	Use of research methods including design of experiments to provide valid conclusions.
PO5	3	Selection and application of appropriate techniques and modern IT tools understanding of the limitations
PO6	1	Application of reasoning to assess societal, health, safety issues and the consequent responsibilities relevant to the professional engineering practices.
PO7	1	Understanding the impact of the professional engineering solutions in societal and environmental contexts.
PO8	1	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	3	Functioning effectively as an individual, and as a member or leader in diverse team.
PO10	3	Communicated effectively on complex engineering activities with the engineering community and with society at large.
PO11	3	Demonstrating knowledge and understanding of the engineering and management principles and to manage projects and in multidisciplinary environments.
PO12	3	Recognizing the need for the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.
PSO1	3	Designing, developing, and integrating electronic circuits and systems using current practices and standards.
PSO2	1	Applying knowledge of hardware and software in designing embedded and communication systems.

CO-PO mapping:

Mapping of Course Outcomes to Program Outcomes and Program Specific Outcomes:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	3	2	3	3	1	1	1	3	3	3	3	3	1
CO2	2	3	2	3	3	1	1	1	3	3	3	3	3	1
CO3	2	3	2	3	3	1	1	1	3	3	3	3	3	1
CO4	2	3	2	3	3	1	1	1	3	3	3	3	3	1
CO5	2	3	2	3	3	1	1	1	3	3	3	3	3	1
CO6	2	3	2	3	3	1	1	1	3	3	3	3	3	1
CO AVG	2	2.5	2	3	3	0.4	0.4	0.4	3	3	3	3	3	0.4

*High=3, Medium=2, Low=1

Justification

CO1	Successfully understand the working of SRAM memory cell and the peripherals required to read and write the data.
CO2	Encountered problems while drawing layouts and schematics were resolved after referring to the design rule files of the technology node.
CO3	Development of read and write circuits were done based on comparison of various available alternatives which enabled us to have deep insights into the components involved.
CO4	Simulations were performed after drawing schematic of each circuit in order to verify its functionality.
CO5	As technology evolves, demand for low power consuming products increases. Considering this our goal is to come up with peripherals which consume less power, area and provide better performance compared to its counterparts.
CO6	The divide work among us were completed within the stipulated time in order to keep up with the schedule which was previously decided.

Budget Estimation Sheets

Sl. No.	Particulars	Estimated Cost in Rs.
1	Cadence(trial version)	Nill
2	HSpice(trial version)	Nill
3	Report	300
	Total	300