CHANDAN SRINIVAS

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PROFILE SUMMARY

- Knowledgeable, self-driven electronic engineer proficient in CMOS, ASIC Design and Firmware Development.
- Aim to use my technical, managerial and multi-tasking skills to solve engineering problems and contribute to a technology-driven society.

EDUCATION

Dayananda Sagar College of Engineering 2019 - 2023
B.E. in Electronics and Communication Engineering; **CGPA: 8.88/10** *Bangalore, India*
Relevant Coursework : Digital Electronics , Analog Electronics, Digital System Design using Verilog, Fundamentals of VLSI, ASIC Design, System Verilog for Verification, Embedded Systems Design, Micrcontrollers.

KMWA PU College 2017 - 2019
Grade 12; **94.67%** ***(Rank 8/200)*** *Bangalore, India*
- *Physics, Chemistry, Mathematics, Computer Science, Kannada and English*

Atreya Vidyaniketan 2008 - 2017
Grade 10; **CGPA: 9.6/10** ***(Rank 2/18)*** *Bangalore, India*
- *Physics, Chemistry, Mathematics, Computer Science, Social Sciences, Hindi, Kannada and English.*

WORK EXPERIENCE

MOOG Inc JuL 2023 -Present
Firmware Development Co-Op *Bangalore, India*
- In my role within a R&D-focused environment, I am currently engaged in developing firmware tailored for ARM-based processors.
- Coordinated closely with the Electronic hardware and Product development team to enhance and empower precision-controlled motors.
- Spearheading the development of simulink based models for TI's C2000 real-time microcontrollers, consequently reducing the development time to half.

PI Square Technologies Feb 2023 - May 2023
Linux Software Intern *Bangalore, India*
- Explored the architecture of the Ubuntu Linux distribution and designed a resilient chat application by applying my expertise in TCP/UDP protocols and socket programming, bridging networking concepts with system-level coding.
- Engineered a program adhering to industry-standard Software Development Life Cycles (SDLCs) including V&V and ASPICE methodologies; capable of Kernel communication through syscalls, simulating shell-like functionalities.
- Received recognition for exceptional performance and distinguished as a top performer.

Entuple Technologies Dec 2022 - Jan 2023
Physical Design & Verification Intern *Bangalore, India*
- Successfully understood and implemented Semi-Custom ASIC Design Flow using Cadence Innovus.
- Simulated and Synthesized the RTL code of UART using NCSim and Genus. The netlist was flushed through Physical Design steps using Cadence Innovus and GDS-II file was obtained after performing Physical Verification.

Maven Silicon Softech Ltd Aug 2022 - Sep 2022
Design Intern *Bangalore, India*
- Developed an AHB-APB bridge module using Verilog, implemented a master-slave interface for the AHB and APB buses and constructed a Finite State Machine of the APB Controller module.
- Concluded the project by successfully synthesizing, simulating and functionally verifying the design. The waveforms were verified against the design specifications.

LEADERSHIP EXPERIENCE

Aspire Leaders Program, Aspire Institute, Harvard University Jan 2023 - Jul 2023
Leadership Trainee *Virtual*
- Selected to be member of an exclusive cohort consisting of 800 out of 52,000 applicants, constituting to the diverse cohort from around the world.
- Engaged in immersive discussions with distinguished professors of Harvard University, delving into global issued faced by people around the world such as violence and harassment and exploring potential solutions.

Team ARCIS, AIAA 2022 Sep 2021 - Jun 2022
Vice Captain and Head of Avionics *Bangalore, India*
- Led a team of 15 to participate in the Design/Build/Fly Challenge organized by AIAA, USA.
- Developed a progressive plan of action for designing, developing, and fabricating a lightweight, high-strength UAV.
- Supervised team to ensure the successful completion of project goals.
- Enabled new recruits and showed enthusiasm to compute propulsion and communication systems' electrical and design requirements to maximize performance.
- Received an awarded positioning our team 19th globally for their Technical Design Report.

Team ARCIS, SAE Aero Design West 2020 and 2021 Sep 2019 - Jun 2021
Technical Engineer and Chief of Design *Bangalore, India*
- Executed a dynamic design life-cycle to create an optimized design.
- Analyzed constraints and used them as parameters for the optimization process.
- Assembled finalized components based on their test outcomes. Served as a manufacturer in a team-oriented environment.
- Conducted research and reviewed content for reports and presentations.
- Led the team to winning 2nd place internationally for Technical design report.

RESEARCH PUBLICATIONS

- **Comparative Analysis of Decoders using Static & Dynamic CMOS Logic:** **10.1109/ICAECIS58353.2023.10170322**:

CONFERENCES ATTENDED

- **International Conference on Advances in Electronics, Communication, Computing and Intelligent Information Systems (ICAECIS - 2023)**:
- **International Conference on Advances in Engineering and Technology for Intelligent Systems (ICAETIS-2023)**:

PROJECTS

- **Full Custom Design of Peripheral circuitry for 8x8 SRAM Block**:
  - Developed a Full-custom SRAM block and automated parts of the steps using Cadence SKILL reducing time consumed.
  - Designed and compare peripheral circuits such as decoder,sense amplifier and precharge circuits.(May '23)
- **Comparative-Analysis-of-Decoders-using-Static-Dynamic-CMOS-Logic**:
  - Designed and compared Decoders using static and dynamic CMOS logic
  - The results of the project i.e, power consumption,delay was interpreted and further published in a conference paper.(Aug '22)
- **PIOs on AXI and Light-weight AXI bus**:
  - Altera SoC's high computational power was unlocked by developing Embedded C and Verilog codes.
  - This enabled the mapping of virtual memory to physical memory, bridging FPGA fabric and ARM Cortex-A9 processor via AXI bus.(Jun '22)
- **Full Adder using Transmission Gates**:
  - The schematic and layout of a full adder were designed using transmission gates.
  - Timing curves were obtained by performing transient analysis, and the design was verified. The technology node involved is gpdk180. (Apr'22)

SKILLS

- **Languages**: Verilog, C++, Embedded C, Shell Scripting,TCL, Cadence SKILL.
- **Tools**: Matlab, Intel Quartus Prime, Proteus, Cadence Virtuoso Tool Suite(Quantus RC & PVS, Spectre, Virtuoso ADE), Cadence Innovus, Xcelium, Genus, Tempus.
- **Platform**: Windows, Linux.
- **Protocols**: SPI, I2C, UART, AHB/APB, CAN.
- **CAD Design Software**: CATIA V5 & SOLIDWORKS.
- **Other Skills**: Latex Editor, Microsoft PowerPoint, UAV Fabrication.

HONOURS AND AWARDS

- Awarded a National level scholarship throughout undergraduate years.
- Stood among the *Top 10%* of 220 students in the Electronics and Communication Department.
- My inventive team was shortlisted as one of the thirty participating teams for Zonal Round in AAKRUTI, 2021.
- Won a gold medal in the technical presentation category at SAE Aero West 2020.
- led the new recruits to achieve *2nd* place internationally under the SAE Aero Design Micro Class 2021.
- Achieved a major success by winning (*19/110*) under technical design report category hosted by AIAA-DBF in 2022
- Awarded *Best Cadence Award* and *Best Project Award* with a cash prize for Main project on a National stage.

CERTIFICATIONS

- **Cadence RTL-to-GDSII Flow, Cadence Design Systems** - Developed proficiency in RTL to GDS flow including RTL design, Synthesis and Formal verification. (2023)
- **SKILL Language Programming, Cadence Design Systems** - Developed proficiency in scripting and automation further reducing time in improving turn-aroung-time. (2023)
- **CMOS Digital VLSI Design, IIT Roorkee** - Studied CMOS Digital circuit design including low power design and expanding my knowledge in the field of Digital design (2023)
- **Microcontroller Embedded C Programming, Fastbit Embedded Brain Academy** - Understood the essential concepts of memory, registers accessing methods, and interpreted datasheets of an Integrated Circuit (IC).(2022)
- **Certified SOLIDWORKS Professional in Mechanical Design, Dassault Systemes**- Designed complex features using SOLIDWORKS, utilized design validation tools for accuracy, and assembled parts with ease and efficiency. (2021)

VOLUNTEERING & COMMUNITY SERVICE

Marshel, NGO -

- Volunteered and created awareness on Tourism in a rural areas and automated local activities to promote tourism.
- Conducted a survey in and around a school jurisdiction encompassing *50* houses to demystify female sanitation, menstruation, and hygiene.
- Analyzed the results to raise awareness about these topics among women and children living in this area.

Rotaract Bangalore West -

- Secured financial resources through crowdsourcing to support the vulnerable group of individuals (Blind Community).
- Assisted approximately *30* members by facilitating the use of Braille equipment and walking canes.

LANGUAGES

- Native Language - Kannada, Hindi.
- Others - English ***(IELTS BAND 8.0)***, German ***(Level B1)***