CHANDAN SRINIVAS

chandansrinivas.me ChandanS15 chandansrinivas55@gmail.com chandansrinivas Bangalore, India

WORK EXPERIENCE

MOOG Inc Jul 2023 -Present

Firmware Development Co-Op/Intern *Bangalore, India*

- Successfully developed firmware tailored for ARM-based processors to control SEMA actuator-motors and deployed it by integrating it to the legacy code.
- Coordinated closely with the electronic hardware and product development team of 10, ensuring that the firmware met all requirements and to optimize the performance of precision-controlled motors.
- Spearheading the development of simulink based models for TI's C2000 real-time microcontrollers, aiming to reduce the development time by ***50%***.

INTERNSHIPS

PI Square Technologies Feb 2023 - May 2023

Linux Software Intern *Bangalore, India*

- Explored the architecture of the Ubuntu Linux distribution and designed a resilient chat application using TCP/UDP protocols and socket programming, bridging networking concepts with system-level coding.
- Engineered a program adhering to industry-standard Software Development Life Cycles (SDLCs) including V&V and ASPICE methodologies, resulting in a program with zero defects.
- Recognized for exceptional performance in developing an efficient and robust application in less time, acknowledged as ***top*** performer/***65*** peers.

Entuple Technologies Dec 2022 - Jan 2023

Physical Design & Verification Intern *Bangalore, India*

- Successfully understood and implemented Semi-Custom ASIC Design Flow using Cadence Innovus, PVS, Genus and Tempus.
- Simulated and Synthesized the RTL code of Counter and UART using Xcelium and Genus, flushing the netlist through PnR flow and obtaining GDS-II file after performing physical verification.

Maven Silicon Softech Ltd Aug 2022 - Sep 2022

Design Intern *Bangalore, India*

- Developed an AHB-APB bridge module using Verilog, implementing a master-slave interface for the AHB and APB buses and constructing a Finite State Machine of the APB Controller module.
- The bridge module achieved a throughput of 100Mb/s working at 100 MHz and a latency of 10ns, meeting all performance requirements such as setup and hold time.

EDUCATION

Dayananda Sagar College of Engineering 2019 - 2023

B.E. in Electronics and Communication Engineering; **CGPA: 8.88/10** ***(Top 8%/250)*** Bangalore, India

Relevant Coursework : Digital Electronics, Digital System Design using Verilog, Fundamentals of VLSI, ASIC Design, System Verilog for Verification, Embedded Systems Design, Micrcontrollers.

KMWA PU College 2017 - 2019

Grade 12; **94.67%** ***(Rank 8/200)*** Bangalore, India

- *Physics, Chemistry, Mathematics, Computer Science, Kannada and English*

Atreya Vidyaniketan 2008 - 2017

Grade 10; **CGPA 9.6/10** ***(Rank 2/18)*** Bangalore, India

- *Physics, Chemistry, Mathematics, Computer Science, Social Sciences, Hindi, Kannada and English*

PROJECTS

Full Custom Design of Peripheral circuitry for 8x8 SRAM Block (Jan '23 - May '23) -

- Designed and implemented a full-custom 8x8 SRAM block, automating parts of the process using Cadence SKILL to reduce development time by ***50%***.
- Designed and compared peripheral circuits such as decoders, sense amplifiers, and precharge circuits, selecting the most efficient designs for the SRAM.

Comparative-Analysis-of-Decoders-using-Static-Dynamic-CMOS-Logic (Aug '22 - Oct '22) -

- Designed and compared decoders using static and dynamic CMOS logic, evaluating their power consumption and delay characteristics.
- Published the results of the project in a conference paper, demonstrating the feasibility of using dynamic CMOS logic to design low-power, high-performance decoders.

PIOs on AXI and Light-weight AXI bus (Apr '22 - Jun '22) -

- Developed Embedded C and Verilog codes to unlock the high computational power of Altera SoCs by bridging the FPGA fabric and ARM Cortex-A9 processor via the AXI bus.
- This enabled the mapping of virtual memory to physical memory, improving the performance and efficiency of applications running on the SoC.

Full Adder using Transmission Gates (Apr'22) -

- The schematic and layout of a full adder were designed using transmission gates.
- Performed transient analysis to obtain timing curves, ensuring that the design met all performance requirements.

CERTIFICATIONS

- **Cadence RTL-to-GDSII Flow, Cadence Design Systems (2023)** - Developed proficiency in RTL to GDS flow including RTL design, Synthesis and Formal verification.
- **SKILL Language Programming, Cadence Design Systems (2023)** - Developed proficiency in SKILL scripting and automation, reducing design turnaround time.
- **CMOS Digital VLSI Design, IIT Roorkee (2023)** - Studied CMOS digital circuit design, including low-power design, expanding my knowledge in digital design.
- **Microcontroller Embedded C Programming, Fastbit Embedded Brain Academy (2022)** - Developed proficiency in microcontroller embedded C programming, including memory management, register access, and IC datasheet interpretation.
- **Certified SOLIDWORKS Professional in Mechanical Design, Dassault Systemes (2021)**- Designed complex features using SOLIDWORKS, utilized design validation tools for accuracy, and assembled parts with ease and efficiency.

SKILLS

Programming Languages : Verilog, C++, Embedded C, Shell Scripting, TCL, Cadence SKILL.
Tools : Matlab/Simulink, Intel Quartus Prime, Proteus, Cadence Virtuoso Tool Suite(Quantus RC & PVS, Spectre, Virtuoso ADE), Cadence Innovus, Xcelium, Genus, Tempus.
Platform : Windows, Linux.
Protocols : SPI, I2C, UART, AHB/APB, CAN.
CAD Design Software : CATIA V5 & SOLIDWORKS.
Other Skills : Latex Editor, Microsoft PowerPoint, UAV Fabrication.

CONFERENCE PUBLICATION

Chandan Srinivas, B. G S, C. S P, K. E. A and P. Vimala, **"Comparative Analysis of Decoders using Static & Dynamic CMOS Logic,"** *2023 International Conference on Advances in Electronics, Communication, Computing and Intelligent Information Systems (ICAECIS)*, Bangalore, India, 2023, pp. 368-372, doi:10.1109/ICAECIS58353.2023.10170322.

LEADERSHIP EXPERIENCE

Aspire Leaders Program, Aspire Institute, Harvard University Jan 2023 - Jul 2023
Leadership Trainee *Virtual*

- Selected to be a member of an exclusive cohort of ***800/52,000*** applicants, representing ***160+*** countries.
- Participated in immersive discussions with distinguished Harvard University professors, delving into global issues such as violence and harassment and exploring potential solutions.

Team ARCIS, AIAA 2022 Sep 2021 - Jun 2022
Vice Captain and Head of Avionics *Bangalore, India*

- Led a team of 15 students to participate in the AIAA Design/Build/Fly Challenge, an international competition to design, build, and fly a lightweight, high-strength UAV.
- Developed a progressive plan of action that guided the team through the design, development, and fabrication process, resulting in a UAV that weighed under ***8,500 grams***, had a wingspan of ***2*** meters, and could fly for over ***4*** minutes at a top speed of *35 km/h*.
- Mentored new recruits and guided them in computing the electrical requirements for the propulsion and communication systems, and design requirements with a focus on maximizing performance and efficiency.
- Led the team to achieve a ***19th*** place finish in the competition for Technical Design Report.

Team ARCIS, SAE Aero Design West 2020 and 2021 Sep 2019 - Jun 2021
Technical Engineer and Chief of Design *Bangalore, India*

- Executed a iterative dynamic design life-cycle to create an optimized design, reducing the weight of the UAV by ***20%*** than expected.
- Conducted research, communicating complex technical information in a clear and concise manner.
- Led the team to secure ***2nd*** place internationally for Technical Design report, which was judged on criteria such as technical innovation, feasibility, clarity, and impact.

HONORS AND AWARDS

- Awarded ***B*est Cadence Award** and ***B*est Project Award (*INR 20,000*)** at SRISHTI 2023, a national competition.
- Awarded National level scholarship **(*INR 50,000*)** throughout undergraduate years waiving approximately ***15%*** of tuition.
- Top ***8%*** of 250 students in the Electronics and Communication Department.
- Team shortlisted for Zonal Round in AAKRUTI 2021, a national competition organised by *Dassault Systèmes.*
- Gold medal for technical presentation at SAE Aero Design West 2020.
- Led team of ***4*** to secure *2nd* place internationally in SAE Aero Design Micro Class 2021.
- Led team of ***15*** to secure ***19th*** place out of **110** teams in AIAA-DBF 2022 technical design report category.

VOLUNTEERING & COMMUNITY SERVICE

Marshel, NGO

- Created awareness on tourism in a rural part of Karnataka to promote eco-tourism increasing visitors number by ***15%***.
- Conducted a survey in a jurisdiction encompassing *50* houses to demystify female sanitation, menstruation, hygiene and raised awareness on these topics among children and women living in this area, reaching over *100* people.

Rotaract Bangalore West

- Secured financial resources through crowdsourcing to support the vulnerable group of people with disability (blind), raising over ***INR 40,000*** to purchase Braille equipment.
- Assisted approximately *30* members by facilitating the use of Braille equipment and walking canes, enabling their independent average walking distance by *20%*.

LANGUAGES AND HOBBIES

- Languages - Kannada, Hindi, English ***(IELTS BAND 8.0)***, German ***(Level B1)***
- Hobbies - Swimming, 3D-Modelling, Trekking.