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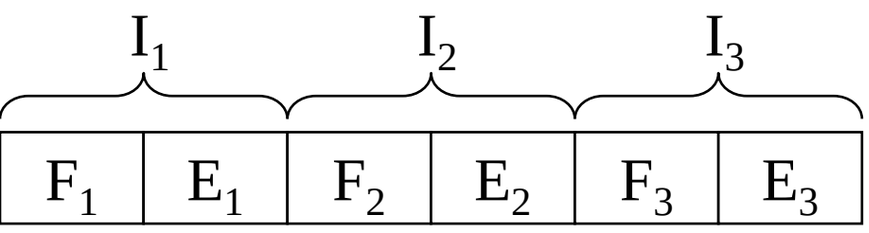
Celebrating 25 SILVER JUBILEE years of Alliance Education

Computer Organization and Architecture

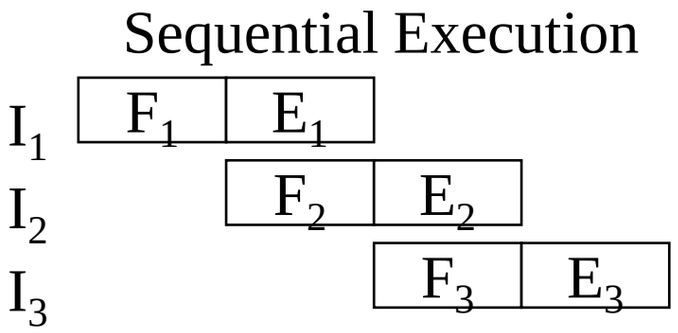
PIPELINING

What is Pipelining?

Pipelining is the process of accumulating instruction from the processor through a pipeline. It allows storing and executing instructions in an orderly process. It is also known as pipeline processing. Pipelining is a technique where multiple instructions are overlapped during execution. Pipeline is divided into stages and these stages are connected with one another to form a pipe like structure. Instructions enter from one end and exit from another end.

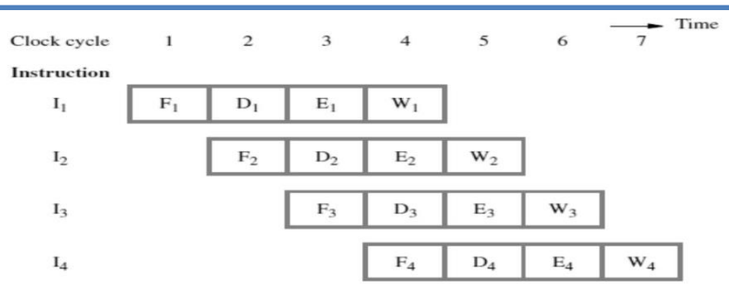


Sequential Execution

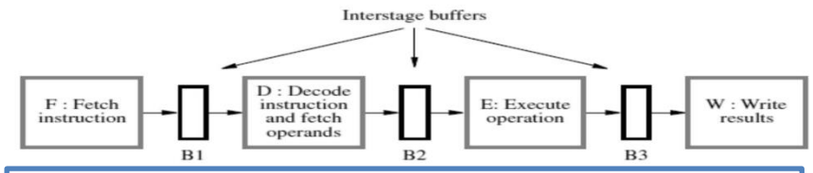


Pipelined Execution

A pipelined processor may process each instruction in four steps, as follows:
F Fetch: read the instruction from the memory.
D Decode: decode the instruction and fetch the source operand(s).
E Execute: perform the operation specified by the instruction.
W Write: store the result in the destination location



Pipelining increases the overall instruction throughput. In pipeline system, each segment consists of an input register followed by a combinational circuit. The register is used to hold data and combinational circuit performs operations on it. The output of combinational circuit is applied to the input register of the next segment.



Pipeline system is like the modern day assembly line setup in factories. For example in a car manufacturing industry, huge assembly lines are setup and at each point, there are robotic arms to perform a certain task, and then the car moves on ahead to the next arm.

Types of Pipeline

It is divided into 2 categories:
1.Arithmetic Pipeline
2.Instruction Pipeline

Instruction Pipeline:

In this a stream of instructions can be executed by overlapping fetch, decode and execute phases of an instruction cycle. This type of technique is used to increase the throughput of the computer system. An instruction pipeline reads instruction from the memory while previous instructions are being executed in other segments of the pipeline. Thus we can execute multiple instructions simultaneously. The pipeline will be more efficient if the instruction cycle is divided into segments of equal duration.

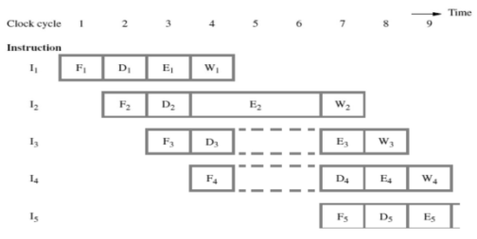
Pipeline Conflicts:

There are some factors that cause the pipeline to deviate its normal performance. Some of these factors are:

1. Timing Variations
2. Data Hazards
3. Branching
4. Interrupts
5. Data Dependency

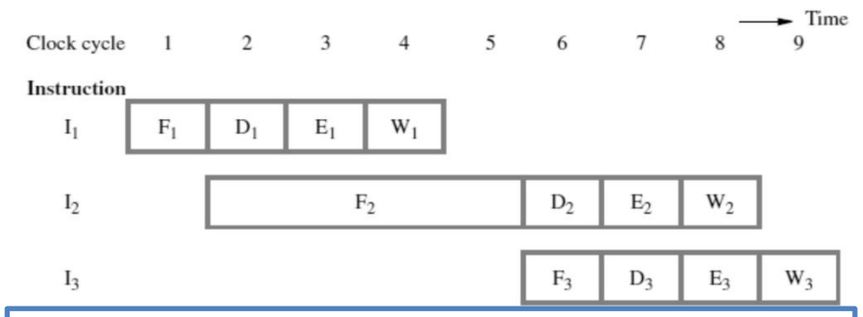
Timing Variations

All stages cannot take same amount of time. This problem generally occurs in instruction processing where different instructions have different operand requirements and thus different processing time.



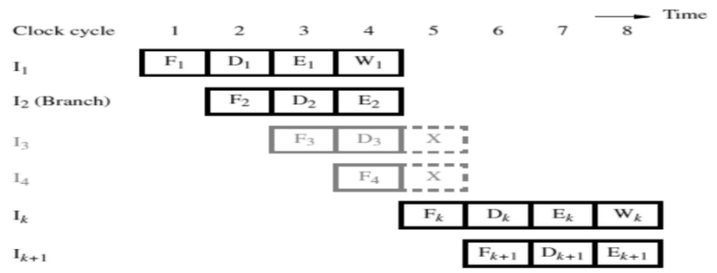
Data Hazards:

When several instructions are in partial execution, and if they reference same data then the problem arises. We must ensure that next instruction does not attempt to access data before the current instruction, because this will lead to incorrect results.



Branching:

In order to fetch and execute the next instruction, we must know what that instruction is. If the present instruction is a conditional branch, and its result will lead us to the next instruction, then the next instruction may not be known until the current one is processed.



Interrupts

Interrupts set unwanted instruction into the instruction stream. Interrupts effect the execution of instruction

Data Dependency

It arises when an instruction depends upon the result of a previous instruction but this result is not yet available.

Advantages

The cycle time of the processor is reduced.
2. It increases the throughput of the system 3. It makes the system reliable.

Disadvantages

1.The design of pipelined processor is complex and costly to manufacture.
2. The instruction latency is more.

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