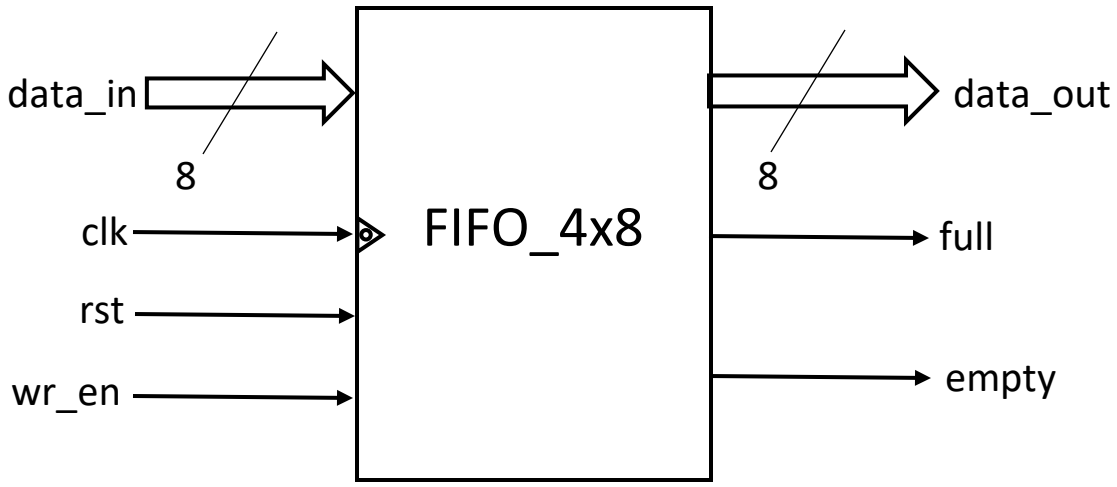
TITLE PAGE

Class	:	BE - 8
Roll. No	:	42428
Assignment No.	:	A. 3
Assignment Name	:	FIFO
Date Of Performance	:	3-10-2020 to 10-10-2020

Block Diagram:



Truth-Table :

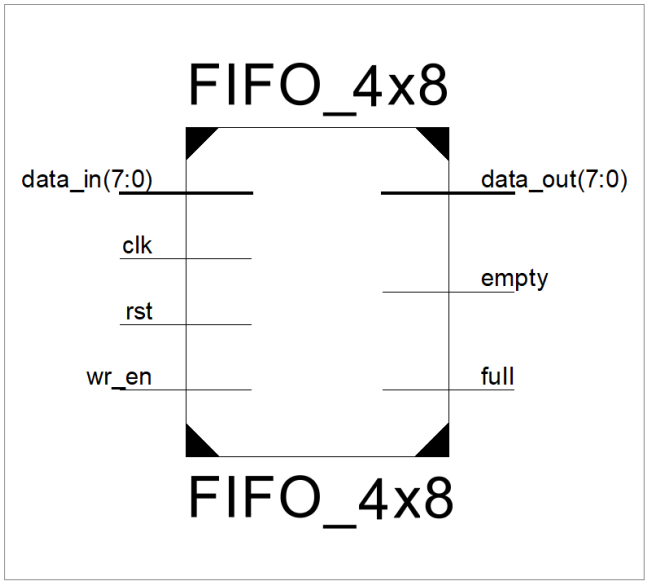
rst	clk	wr_en	data_out	full	empty
1	X	X	$(00)_{16}$	0	1
0	↓	0	N.A	0 -> 1	0
0	↓	1	data_in	1	0

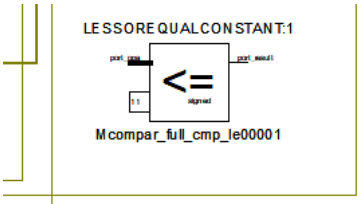
MAIN VHDL PROGRAM

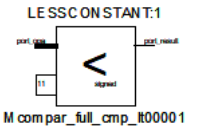
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

entity FIFO_4x8 is
   Port ( data_in : in  STD_LOGIC_VECTOR (7 downto 0);
          rst : in  STD_LOGIC;
          clk : in  STD_LOGIC;
          wr_en : in  STD_LOGIC;
          data_out : out  STD_LOGIC_VECTOR (7 downto 0);
          empty : inout  STD_LOGIC;
          full : inout  STD_LOGIC);
end FIFO_4x8;

architecture FIFO_4x8_ARCH of FIFO_4x8 is
TYPE MEMORY IS ARRAY(0 TO 3) OF STD_LOGIC_VECTOR(7 DOWNTO 0);
SIGNAL MEM : MEMORY:=(X"00",X"00",X"00",X"00");
SIGNAL FRONT : INTEGER:=0;
SIGNAL REAR : INTEGER:=0;
begin
PROCESS(data_in,rst,clk,wr_en,empty,full)
BEGIN

            IF rst='1' THEN
                        FRONT<=0;
                        REAR<=0;
                        data_out<=X"00";
                        MEM<=(X"00",X"00",X"00",X"00");
                        empty<='1';
                        full<='0';
            ELSIF FALLING_EDGE(clk) THEN
                        IF wr_en='0' THEN
                                    IF (REAR>3 OR full='1') THEN
```

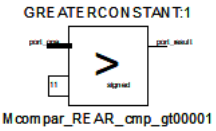
```
                    full<='1';
                ELSE
                    MEM(REAR)<=data_in;
                    REAR<=REAR+1;
                    empty<='0';
                    IF (REAR>=3) THEN
                        full<='1';
                    END IF;
                END IF;
            ELSE
                IF (empty='1') THEN
                    empty<='1';
                ELSIF (FRONT=3) THEN
                    data_out<=MEM(FRONT);
                ELSE
                    data_out<=MEM(FRONT);
                    FRONT<=FRONT+1;
                END IF;
            END IF;
        END IF;

END PROCESS;
end FIFO_4x8_ARCH;
```

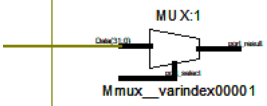
RTL SCHEMATIC

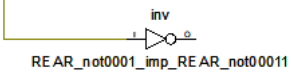


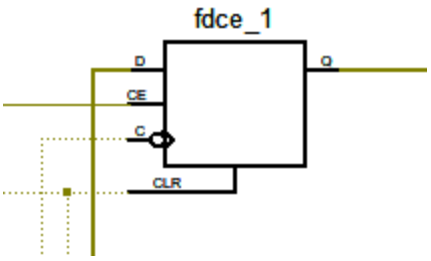


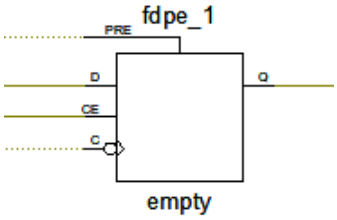


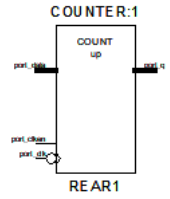


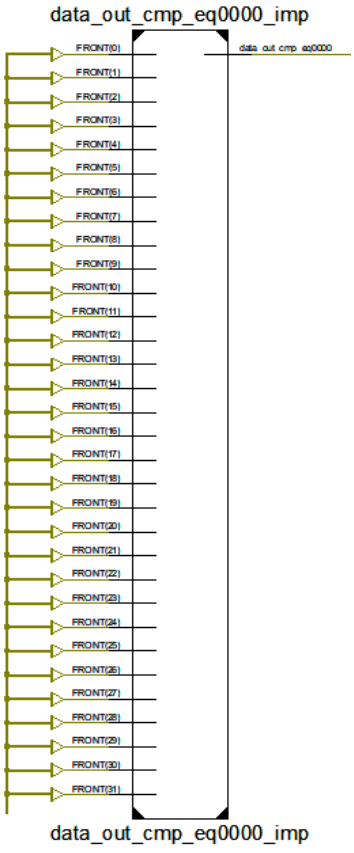


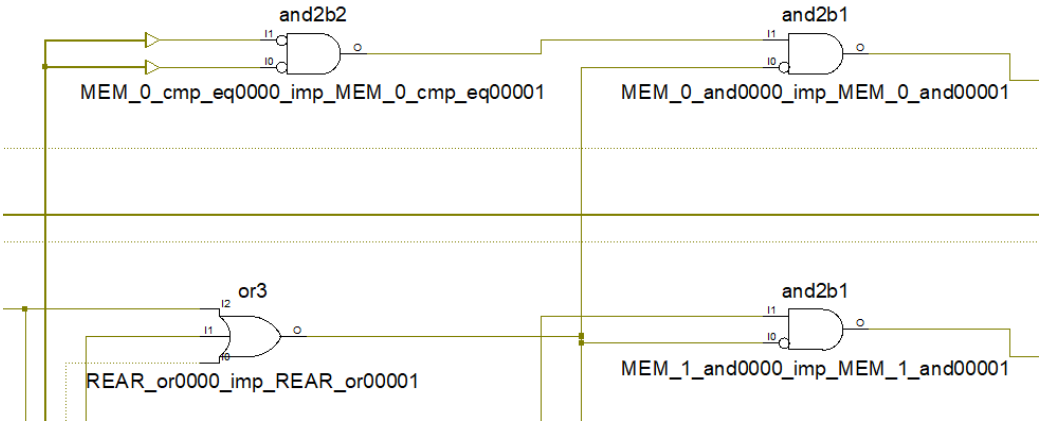


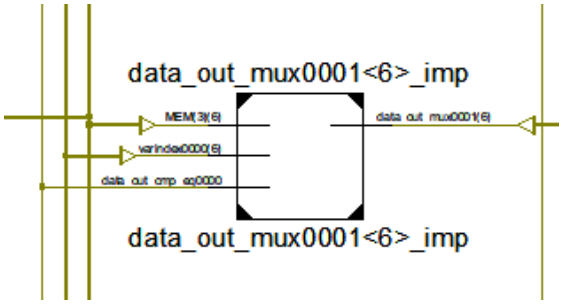


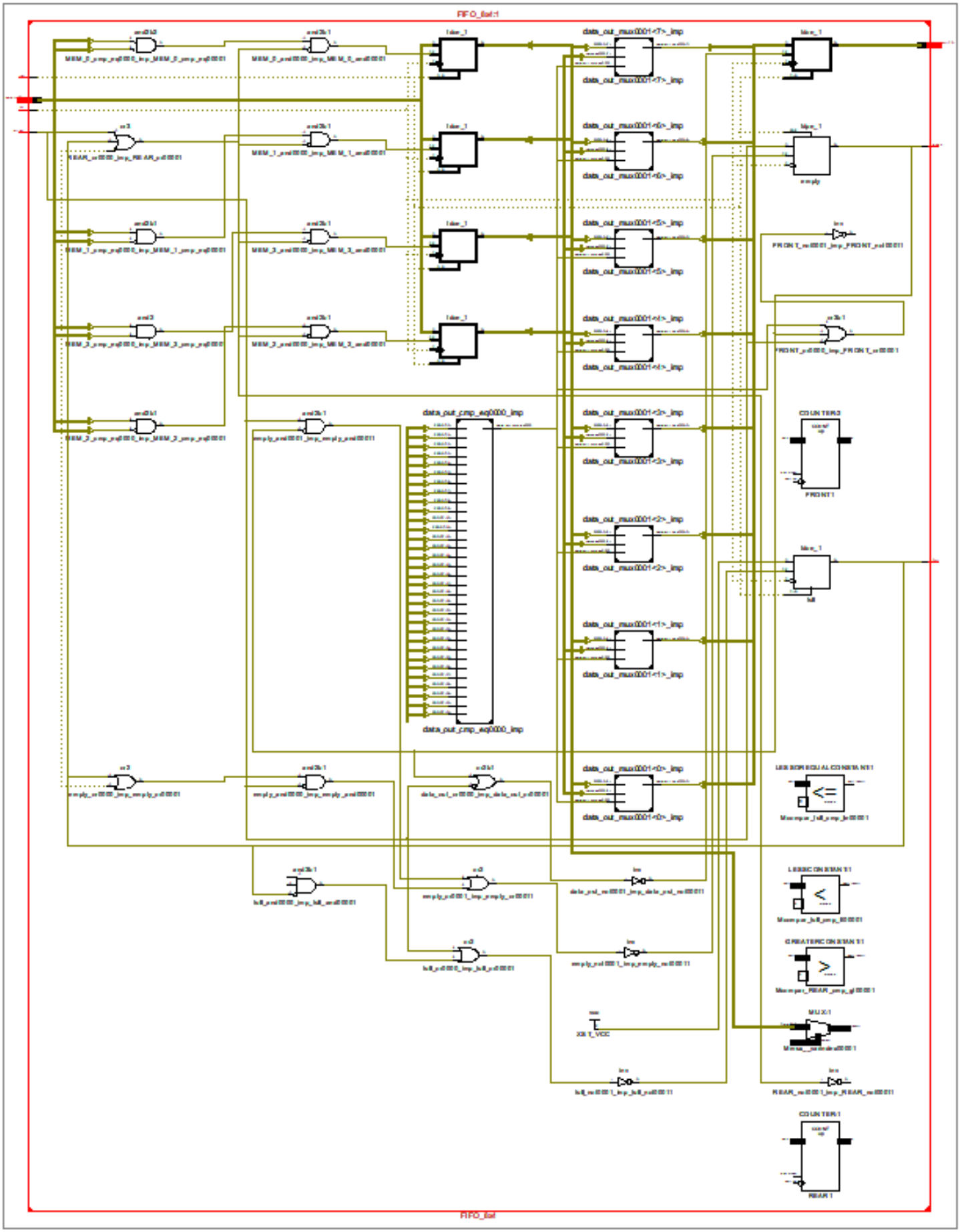




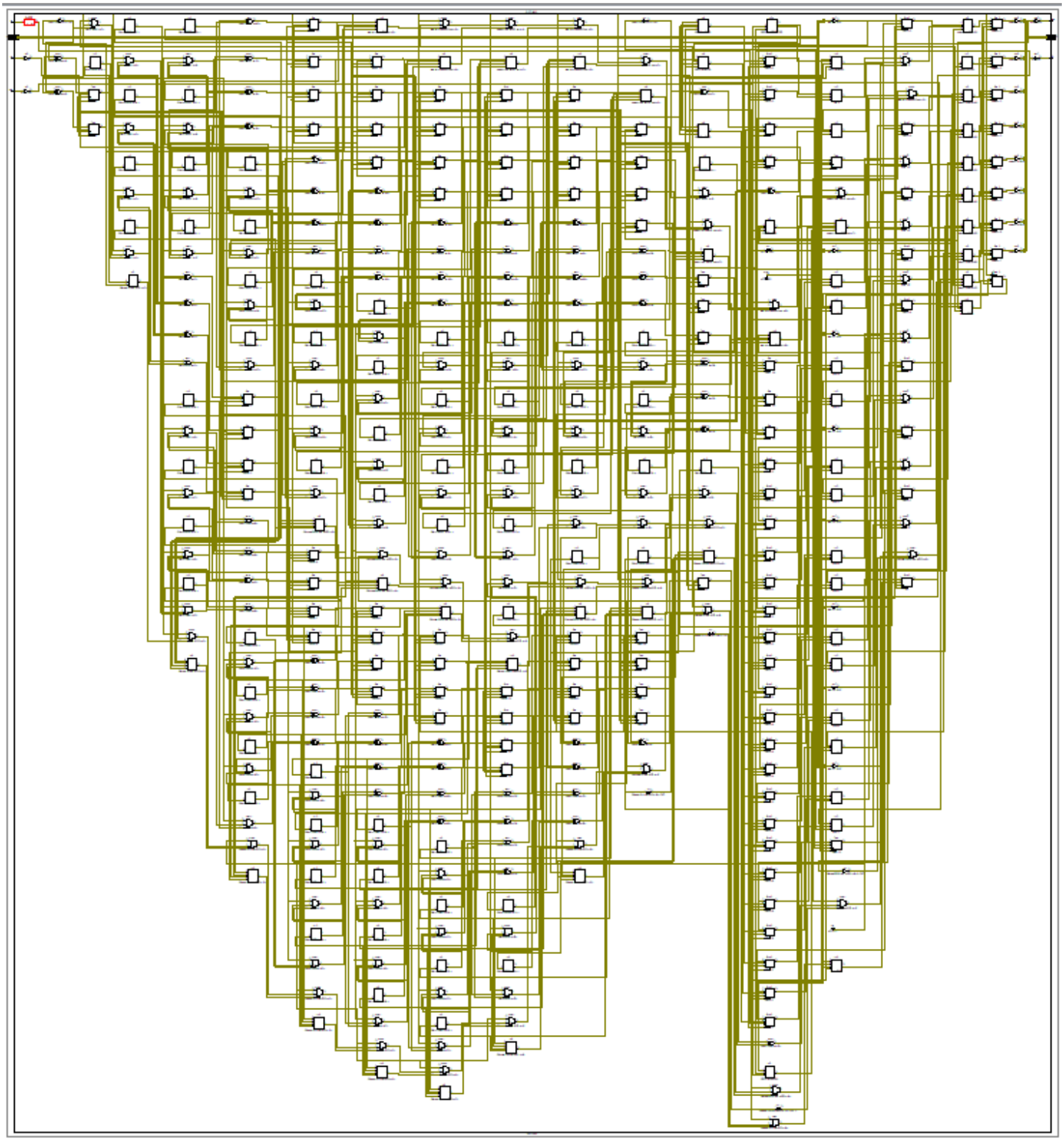


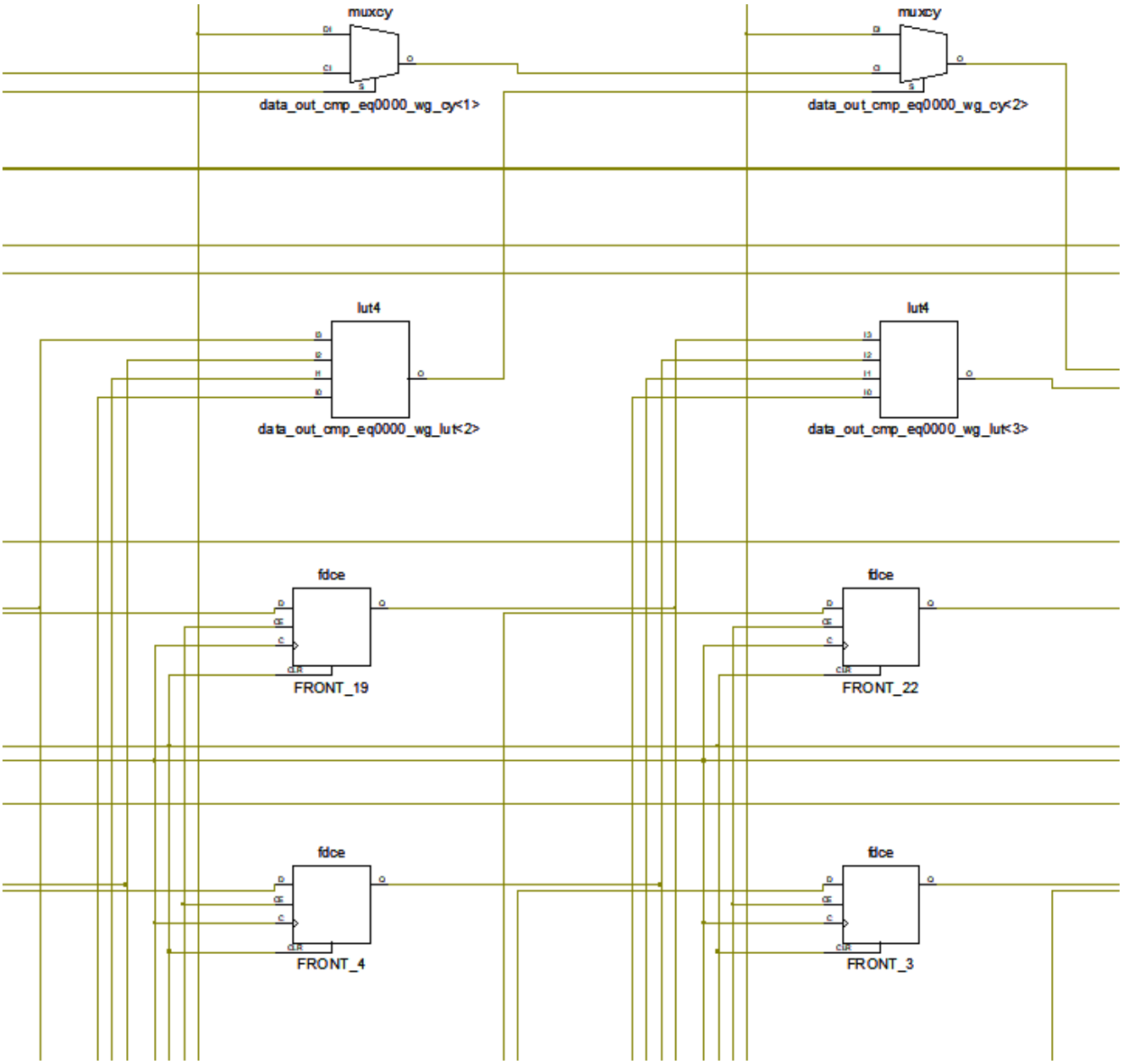





FIFO_Sol:1
data_out_mux0001<7>_Imp
data_out_mux0001<6>_Imp
data_out_mux0001<5>_Imp
data_out_mux0001<4>_Imp
data_out_mux0001<3>_Imp
data_out_mux0001<2>_Imp
data_out_mux0001<1>_Imp
data_out_mux0001<0>_Imp
data_out_cmp_eq0000_Imp
COUNTER3
FRONT1
COUNTER1
REAR1
MUX1
FIFO_Sol

TECHNOLOGY SCHEMATIC




muxcy
DI
CI
S
O
data_out_cmp_eq0000_wg_cy<1>
muxcy
DI
CI
S
O
data_out_cmp_eq0000_wg_cy<2>
lut4
I3
I2
I1
I0
O
data_out_cmp_eq0000_wg_lut<2>
lut4
I3
I2
I1
I0
O
data_out_cmp_eq0000_wg_lut<3>
fdce
D
CE
C
CLR
Q
FRONT_19
fdce
D
CE
C
CLR
Q
FRONT_22
fdce
D
CE
C
CLR
Q
FRONT_4
fdce
D
CE
C
CLR
Q
FRONT_3

SYNTHESIS REPORT

1) Device Utilisation Summary

```
=========================================================================
*                  Final Report                  *
=========================================================================
Final Results
RTL Top Level Output File Name     : FIFO_4x8.ngr
Top Level Output File Name         : FIFO_4x8
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No
Design Statistics
# IOs                              : 21

Cell Usage :
# BELS                             : 289
#      GND                         : 1
#      INV                         : 7
#      LUT1                        : 62
#      LUT2                        : 2
#      LUT2_D                      : 1
#      LUT3                        : 26
#      LUT4                        : 28
#      MUXCY                       : 89
#      MUXF5                       : 8
#      VCC                         : 1
#      XORCY                       : 64
# FlipFlops/Latches                : 106
#      FDCE                        : 64
#      FDCE_1                      : 41
#      FDPE_1                      : 1
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 20
#      IBUF                        : 10
#      OBUF                        : 10
=========================================================================
Device utilization summary:
---------------------------
Selected Device : 3s250epq208-5
 Number of Slices:                  81  out of   2448     3%
 Number of Slice Flip Flops:        106  out of   4896     2%
 Number of 4 input LUTs:            126  out of   4896     2%
 Number of IOs:                     21
 Number of bonded IOBs:             21  out of    158    13%
 Number of GCLKs:                   1  out of     24     4%
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
```

2) TIMING REPORT

Timing Summary:

Speed Grade: -5

Minimum period: 5.693ns (Maximum Frequency: 175.653MHz)

Minimum input arrival time before clock: 4.609ns

Maximum output required time after clock: 4.221ns

Maximum combinational path delay: No path found

Timing Detail:

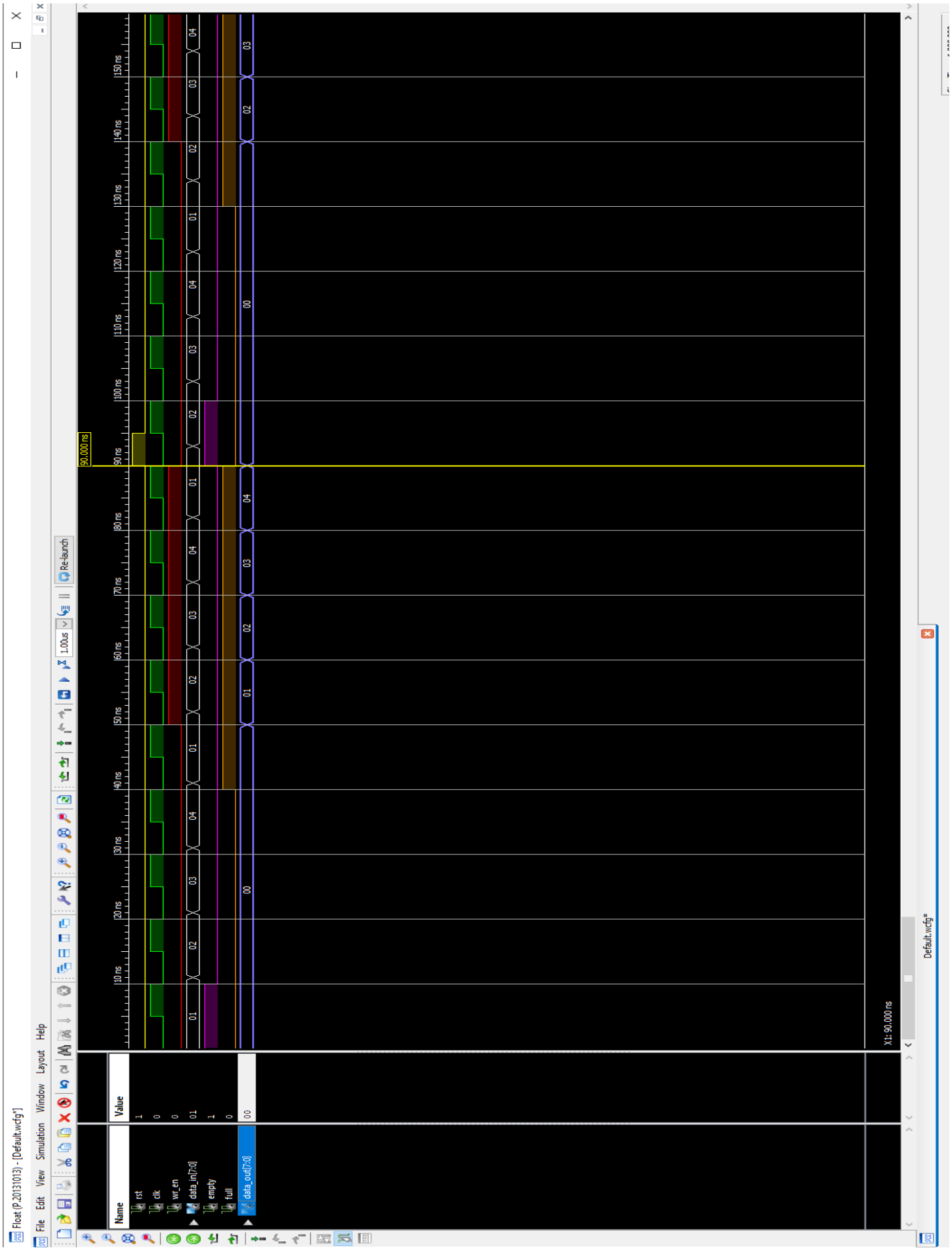
All values displayed in nanoseconds (ns)

TESTBENCH PROGRAM

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY FIFO_4x8_tb IS
END FIFO_4x8_tb;

ARCHITECTURE behavior OF FIFO_4x8_tb IS
   COMPONENT FIFO_4x8
   PORT(
        data_in : IN  std_logic_vector(7 downto 0);
        rst : IN  std_logic;
        clk : IN  std_logic;
        wr_en : IN  std_logic;
        data_out : OUT  std_logic_vector(7 downto 0);
        empty : INOUT  std_logic;
        full : INOUT  std_logic
       );
   END COMPONENT;

  signal data_in : std_logic_vector(7 downto 0) := (others => '0');
  signal rst : std_logic := '1';
  signal clk : std_logic := '0';
  signal wr_en : std_logic := '0';

  signal empty : std_logic;
  signal full : std_logic;

  signal data_out : std_logic_vector(7 downto 0);

  constant clk_period : time := 10 ns;

BEGIN
  uut: FIFO_4x8 PORT MAP (
        data_in => data_in,
        rst => rst,
        clk => clk,
        wr_en => wr_en,
        data_out => data_out,
        empty => empty,
        full => full
       );
```

```
  clk_process :process
  begin
        clk <= '0';
        wait for clk_period/2;
        clk <= '1';
        wait for clk_period/2;
  end process;

  stim_proc_data_in: process
  begin
        data_in<=X"01";
        wait for 11 ns;
        data_in<=X"02";
        wait for 10 ns;
        data_in<=X"03";
        wait for 10 ns;
        data_in<=X"04";
        wait for 10 ns;
  end process;

  stim_proc_rst: process
  begin
        rst<='0';
        wait for 90 ns;
        rst<='1';
        wait for 5 ns;
  end process;

  stim_proc_wr_en: process
  begin
        wr_en<='0';
        wait for 50 ns;
        wr_en<='1';
        wait for 40 ns;
  end process;
END;
```

ISIM WAVEFORMS



PIN-LOCKING REPORT

```
# PlanAhead Generated physical constraints

NET "data_in[7]" LOC = P165;     #sw4-0
NET "data_in[6]" LOC = P167;     #sw4-1
NET "data_in[5]" LOC = P163;     #sw4-2
NET "data_in[4]" LOC = P164;
NET "data_in[3]" LOC = P161;
NET "data_in[2]" LOC = P162;
NET "data_in[1]" LOC = P160;
NET "data_in[0]" LOC = P153;     #sw4-7
NET "data_out[7]" LOC = P179;  #sw3-0
NET "data_out[6]" LOC = P180;  #sw3-1
NET "data_out[5]" LOC = P177;
NET "data_out[4]" LOC = P178;
NET "data_out[3]" LOC = P152;
NET "data_out[2]" LOC = P168;
NET "data_out[1]" LOC = P171;
NET "data_out[0]" LOC = P172;  #sw3-7
NET "clk" LOC = P132;
NET "rst" LOC = P204;              #k0
NET "enr" LOC = P184;              #sw2-6
NET "enw" LOC = P194;              #sw2-7
NET "empty" LOC = P199;#sw1-6
NET "full" LOC = P196;   #sw1-7
```

Conclusion:

Thus we have :

1) Modeled a 4x8 FIFO using Behavioral Modeling Style.
2) Observed following Schematics: **RTL** & **Technology Schematics** generated **Post-Synthesis**.
3) Interpreted **Device Utilization Summary** in terms of LUTs, SLICES, IOBs, Multiplexers & D FFs used out of the available device resources.
4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency.
5) Written a TESTBENCH to verify the functionality of 4x8 FIFO & verified the functionality as per the TRUTH-TABLE by observing ISIM Waveforms.
6) Used PlanAhead Editor for pin-locking.
7) Prototyped the FPGA **XC3S250EPQ208-5** to realize 4x8 FIFO & verified its operation by giving suitable input combinations.