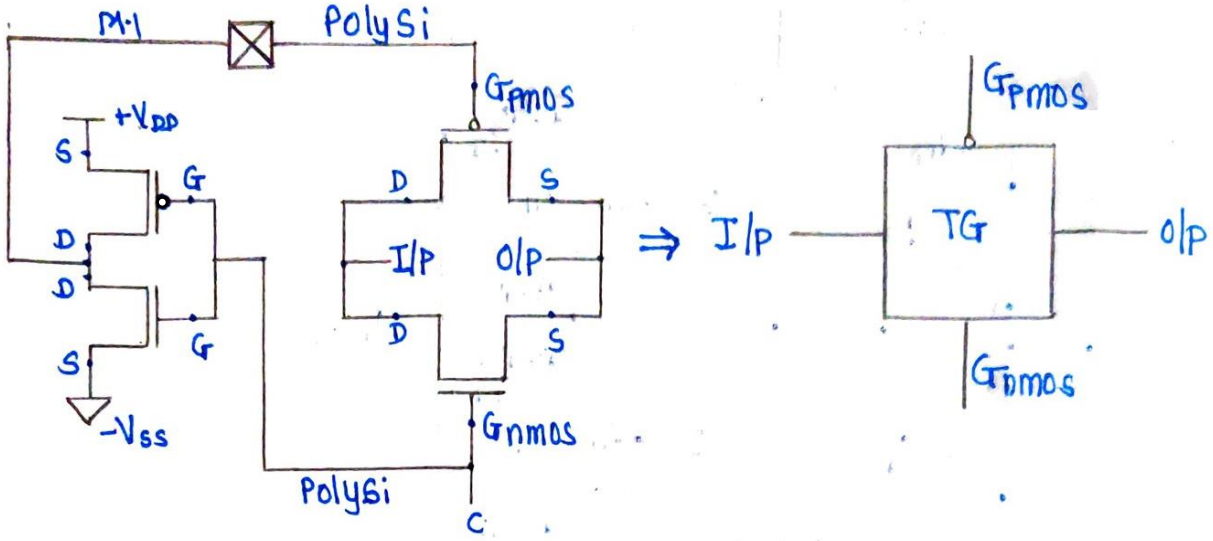
TITLE PAGE

Class	:	BE - 8
Roll. No	:	42428
Assignment No.	:	B. 2
Assignment Name	:	2:1 MUX using TG
Date Of Performance	:	21-11-2020

Theory:

Schematic of TG-

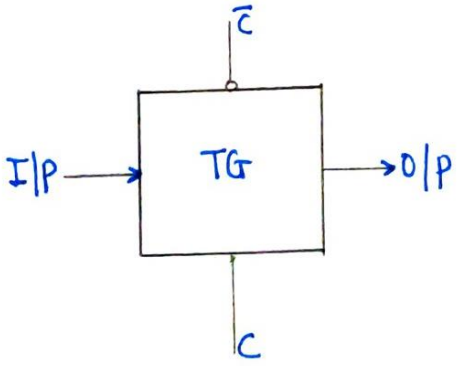


For $C = 1$, $O/P = I/P$

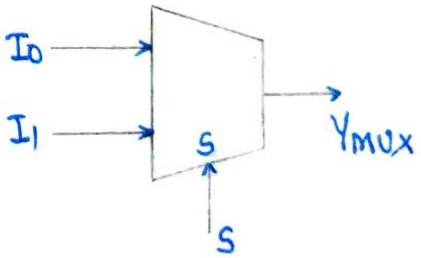
$C = 0$, $O/P = 0$

Schematic of 2:1 MUX using TG

Symbol of TG



Symbol of 2:1 MUX

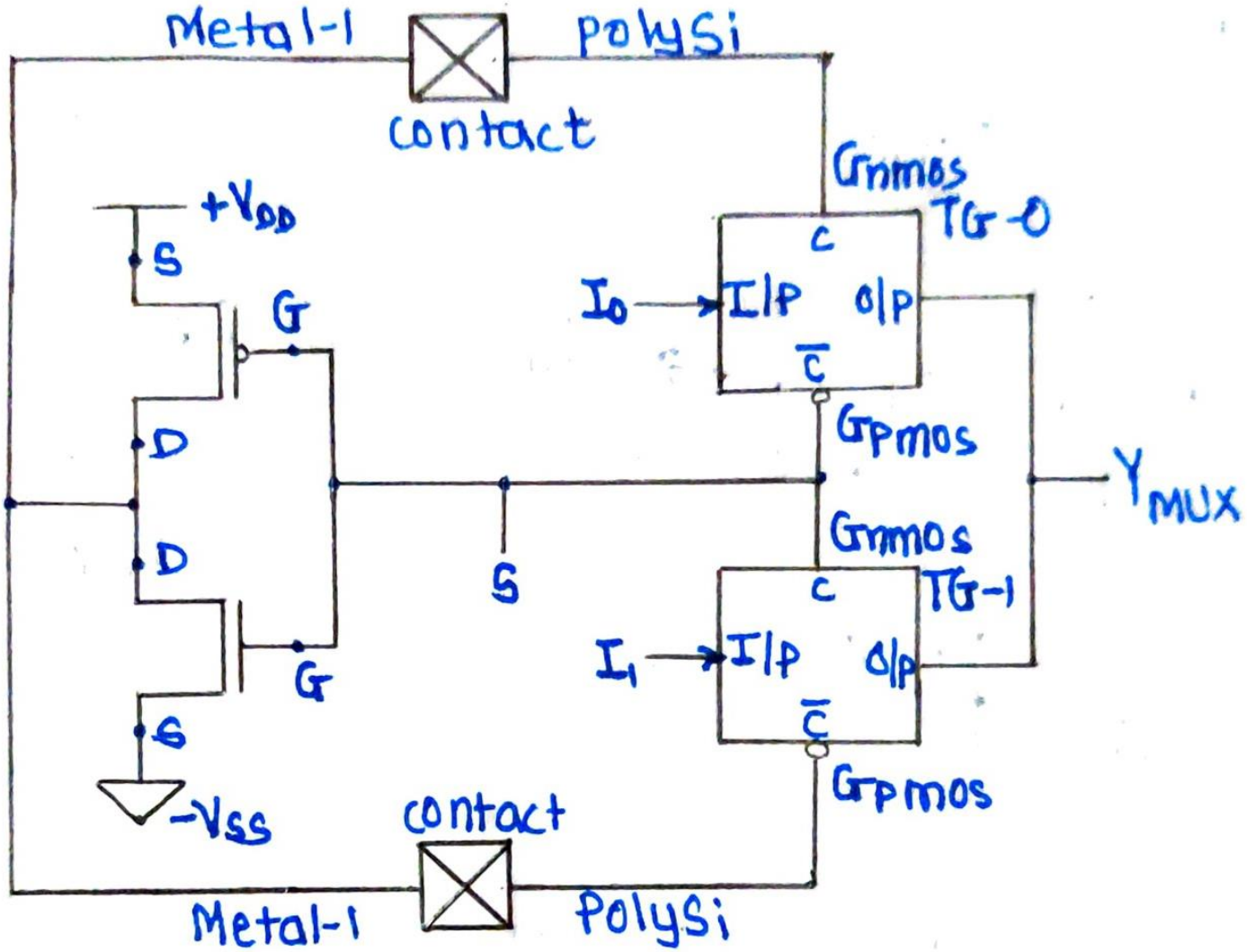


Truth Table

C	O/P
1	I/P
0	0

Truth Table

S	Y_{MUX}
0	I_0
1	I_1



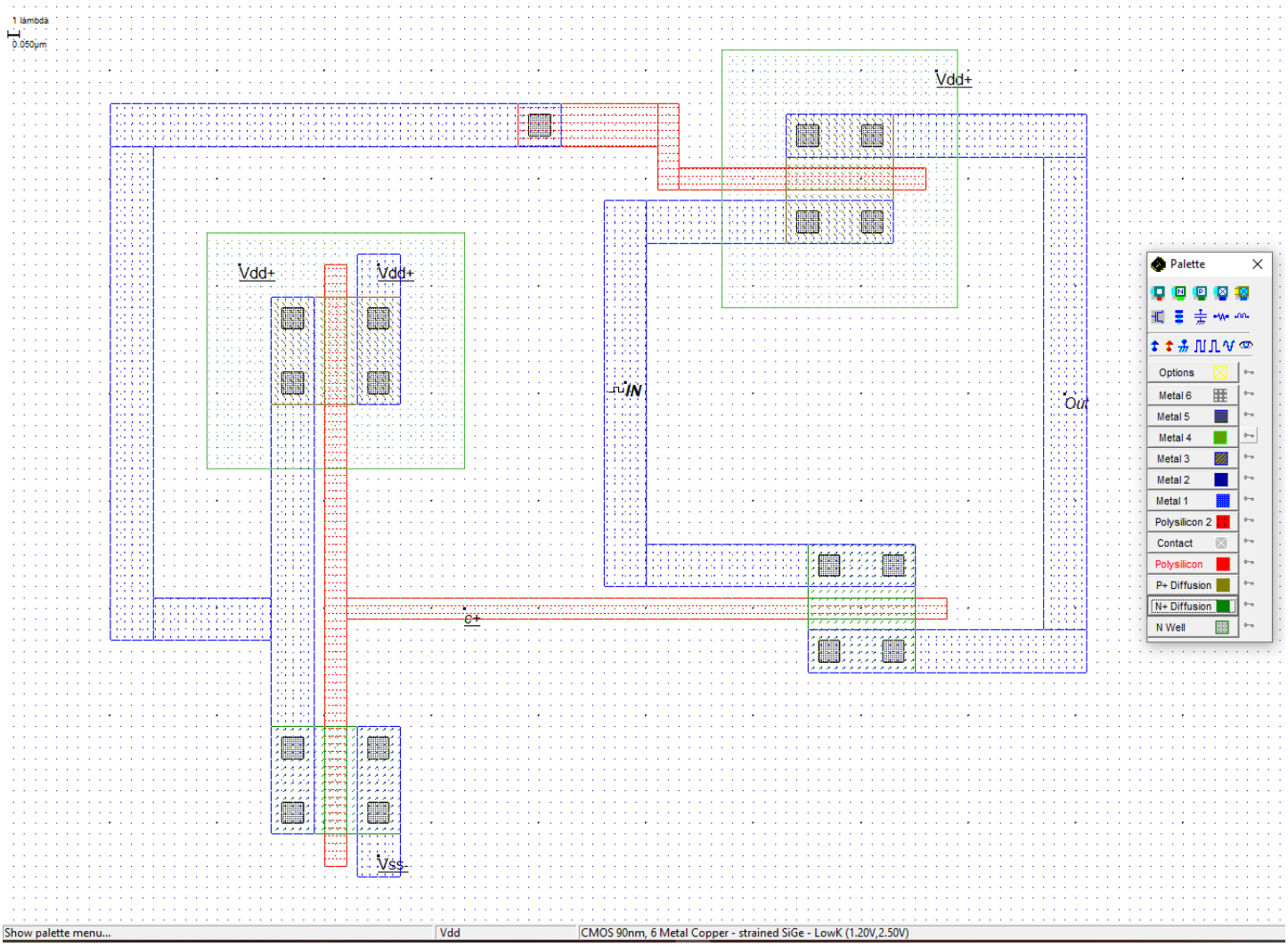
All PMOS & NMOS Devices have sizes-

$$P = n = \left(\frac{500}{100}\right) nm = 5$$

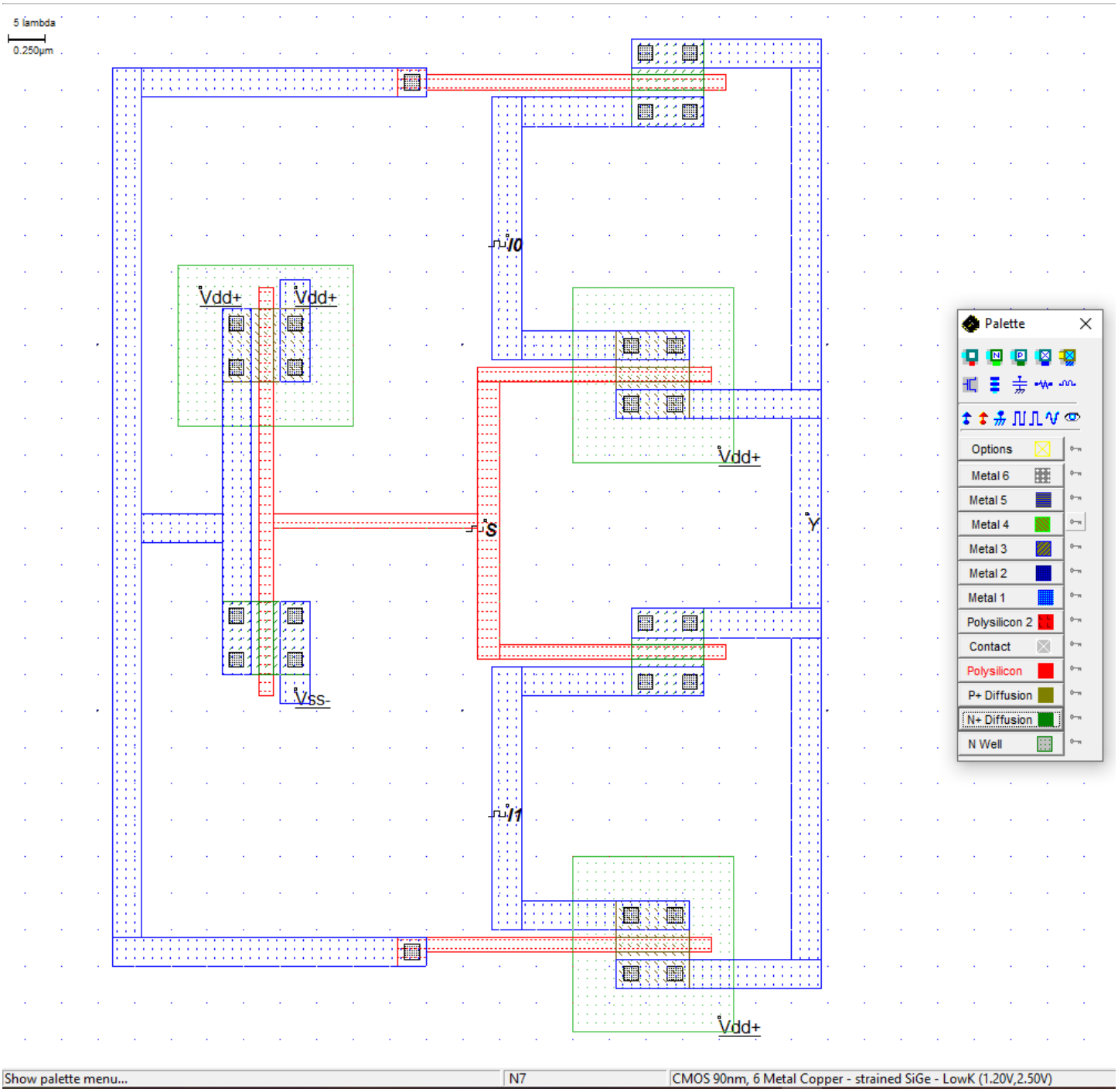
$$P/n = 1$$

LAYOUT

a) Transmission Gate

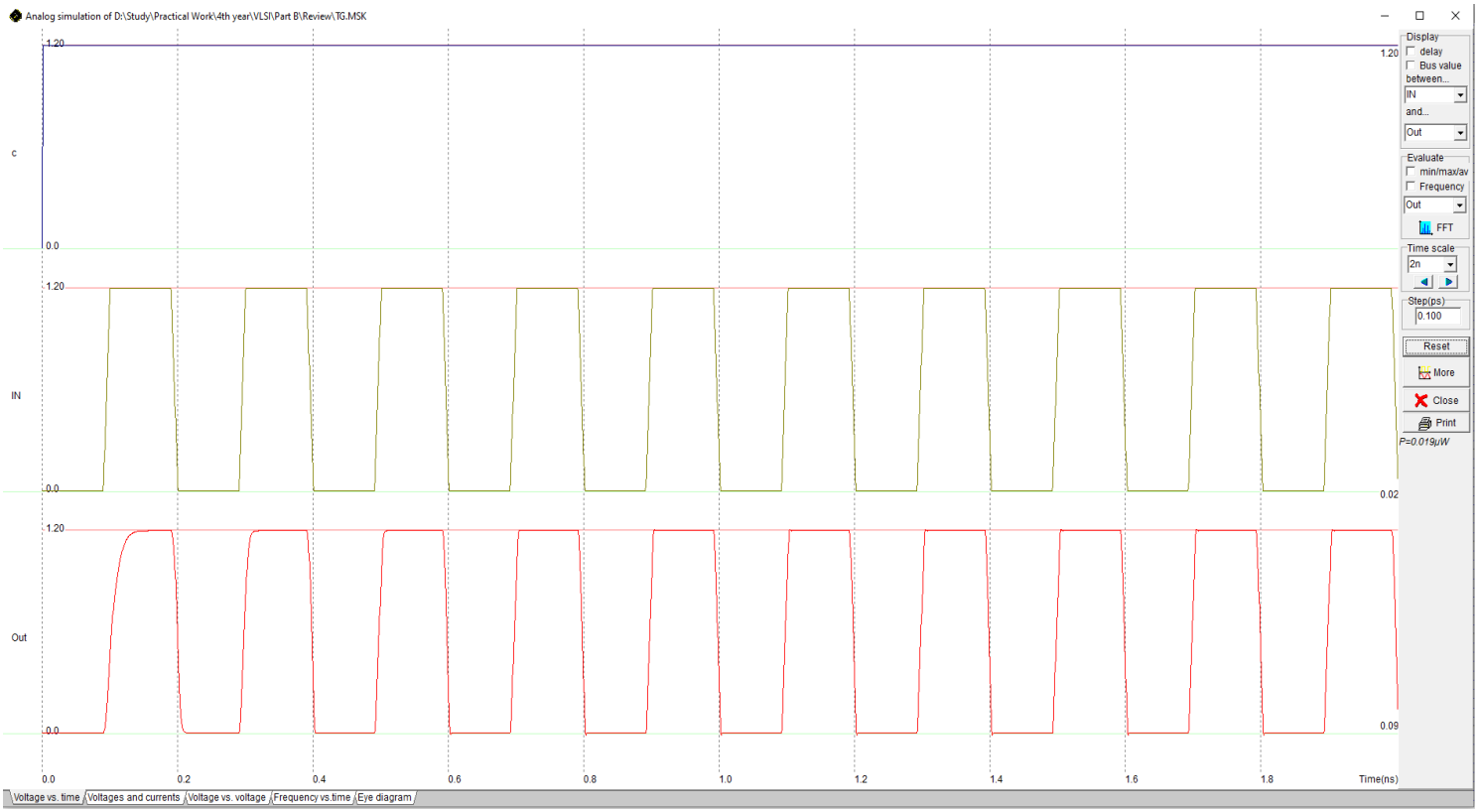


b) 2:1 MUX using 2 Transmission Gates

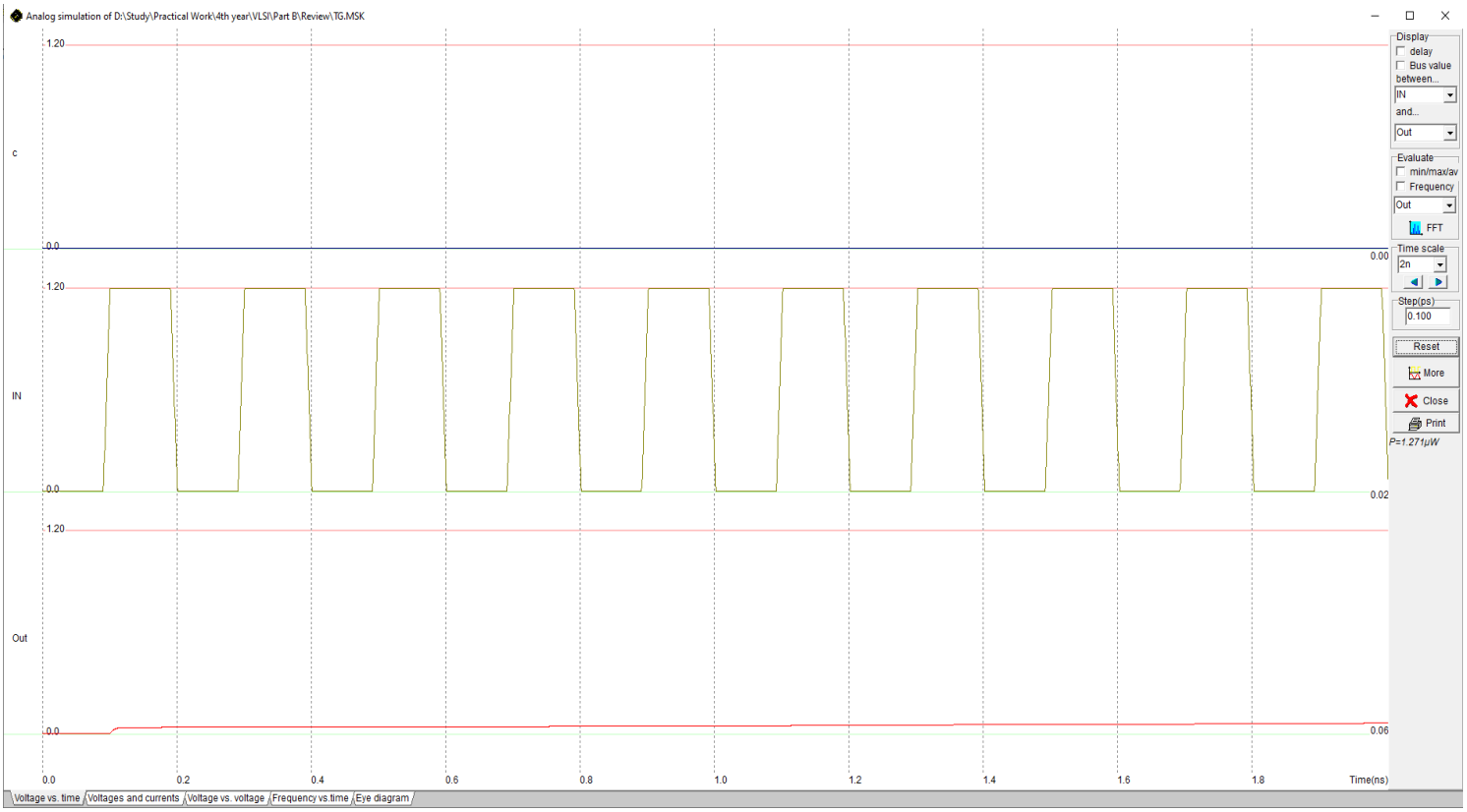


Waveforms

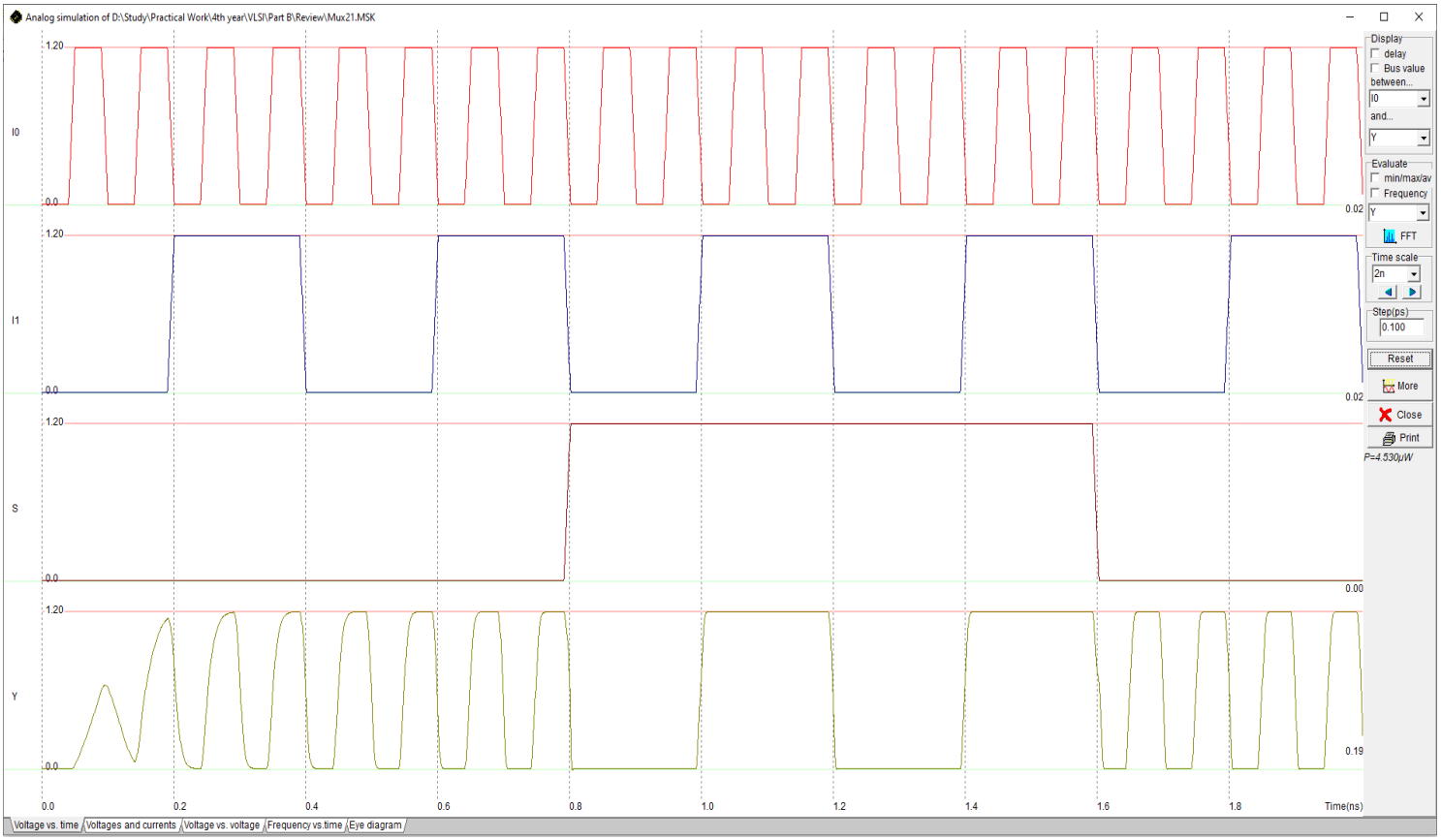
a) Output of Transmission Gate when c = 1



b) Output of Transmission Gate when c = 0



c) Output of 2:1 MUX



Conclusion:

Thus we have :

1) Drawn the LAYOUT for Transmission Gate using 90 nm Foundry.
2) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.
3) Using the above verified LAYOUT of Transmission gate, drawn the LAYOUT for 2:1 MUX.
4) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.
5) TG is a CMOS Switch; hence it gives both STRONG-1 and STRONG-0 at the output.
6) Multiplexer is built using 2 TG Switches and 1 CMOS Inverter hence, it is a CMOS Multiplexer, gives both STRONG-1 and STRONG-0 at the output.
7) TG Logic reduces the transistor count for MUX implementation over CMOS Logic from 20 to 6.