

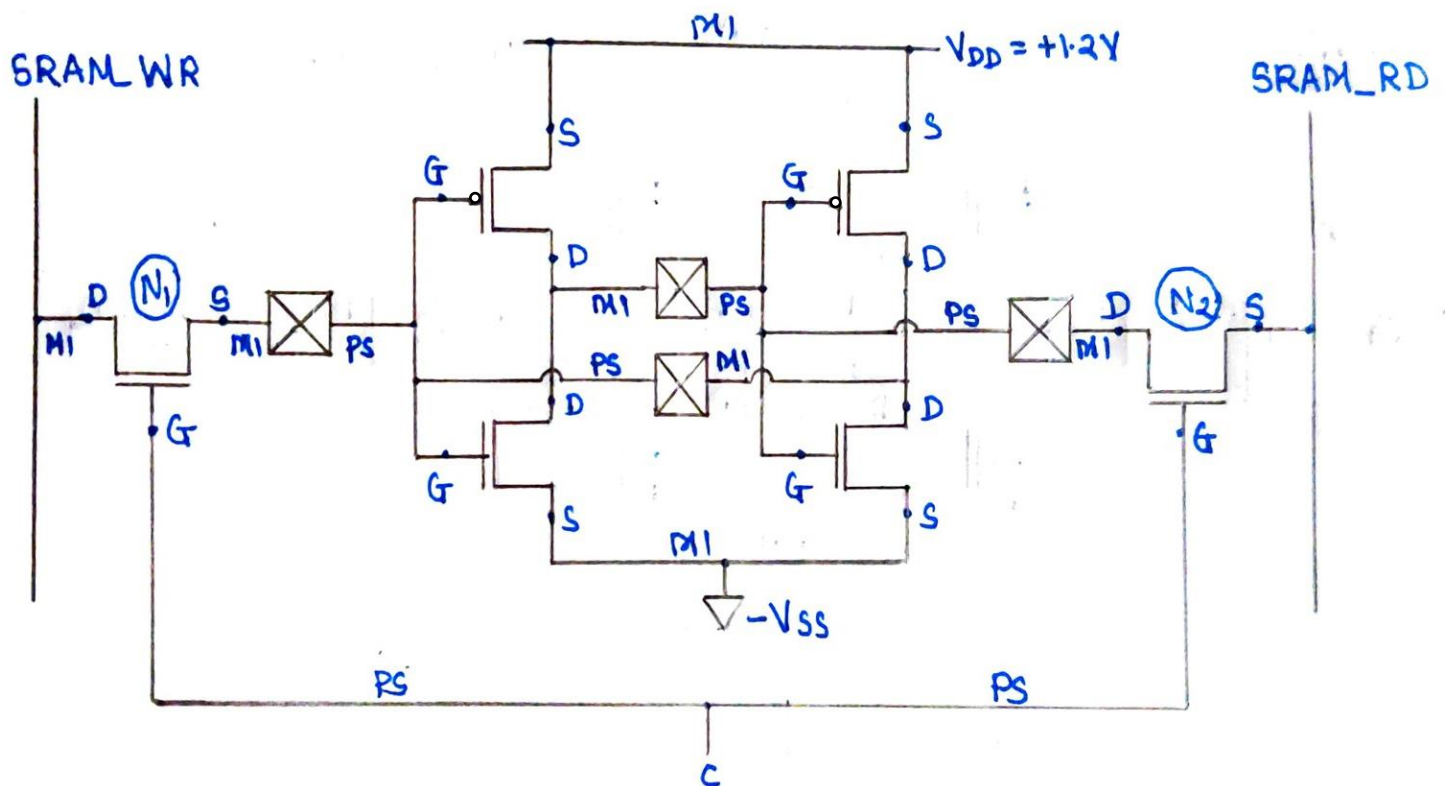
## TITLE PAGE

Class	:	BE - 8
Roll. No	:	42428
Assignment No.	:	B. 3
Assignment Name	:	1-bit SRAM Cell
Date Of Performance	:	28-11-2020

**Theory:**

$$F = 90 \text{ nm.}$$

3.a) : 1-bit SRAM Cell using NMOS Switches-

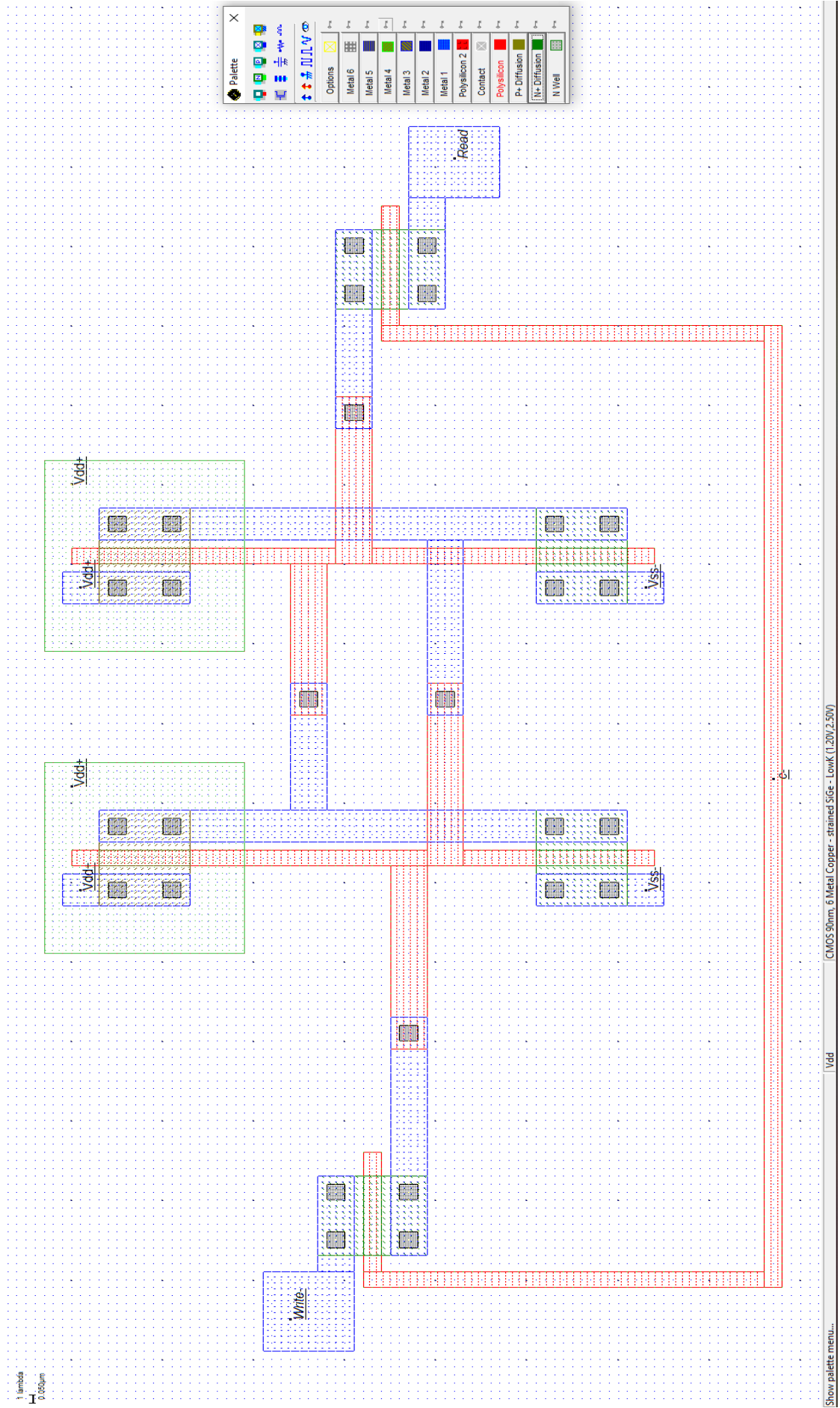


$N_1, N_2$  : NMOS S/W's

### Function Table-

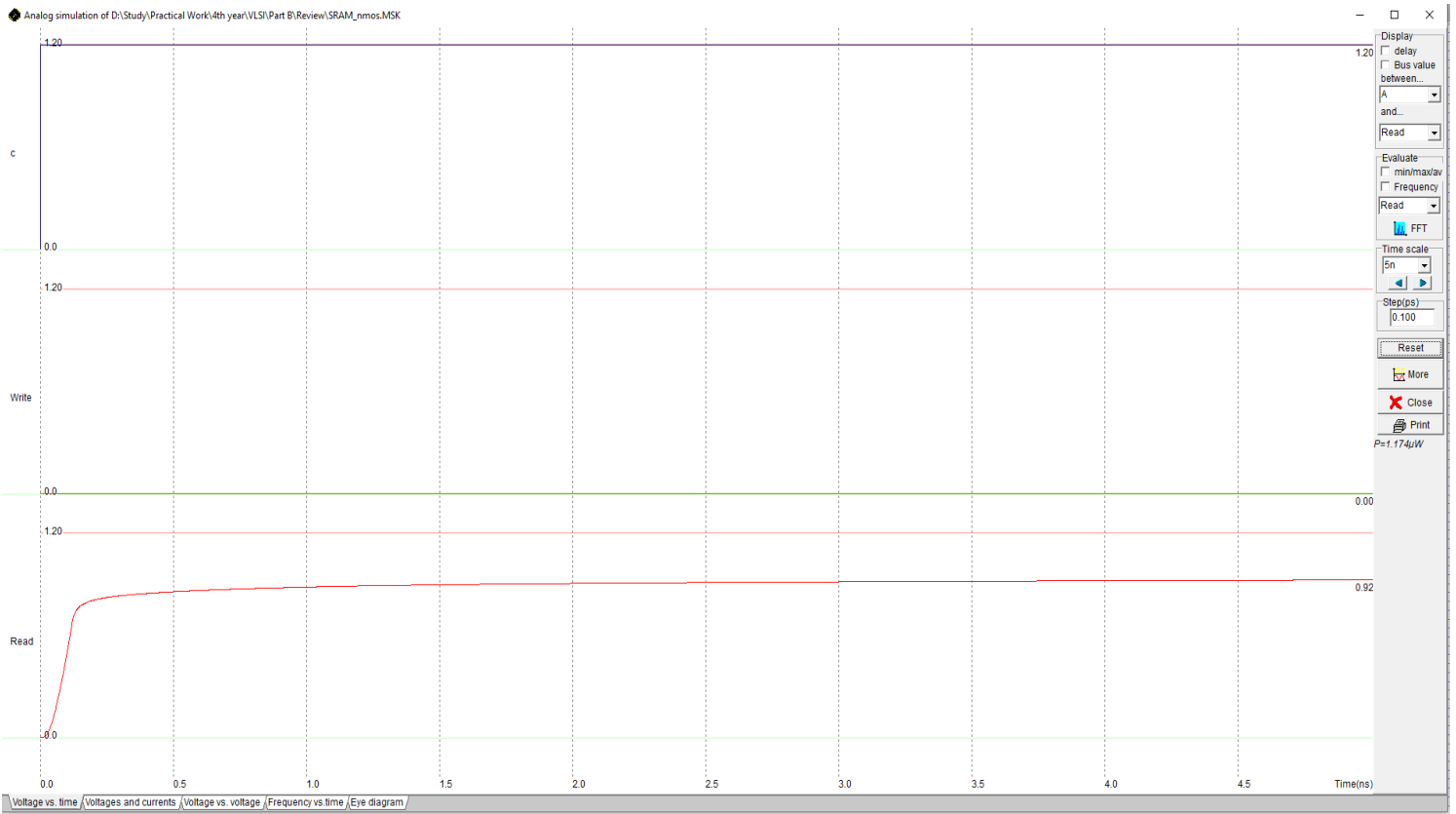
C	SRAM_WR	SRAM_RD
1	0	WEAK-1
1	1	STRONG-0
0	X	0/HOLD

# LAYOUT

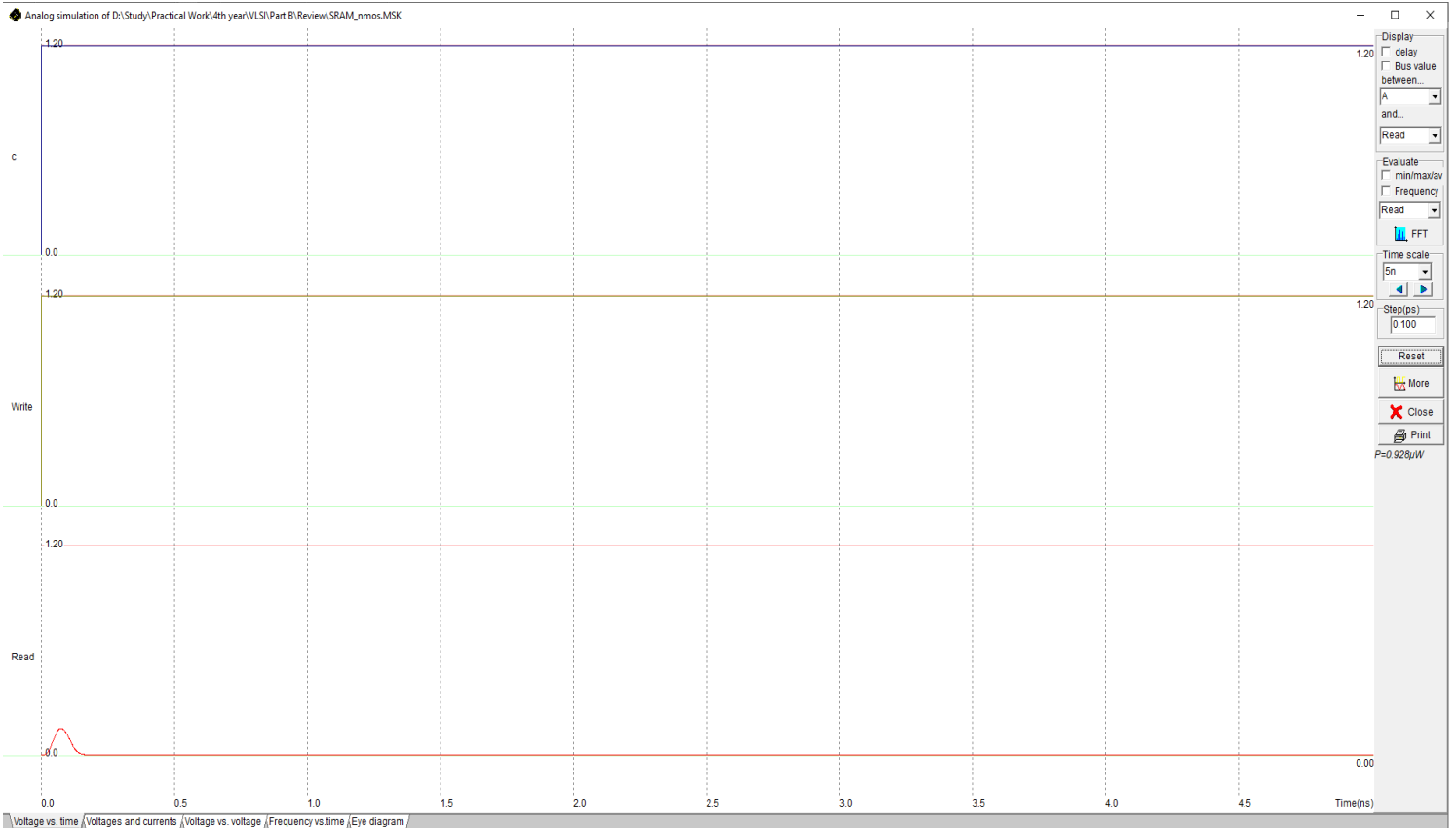


## Waveforms

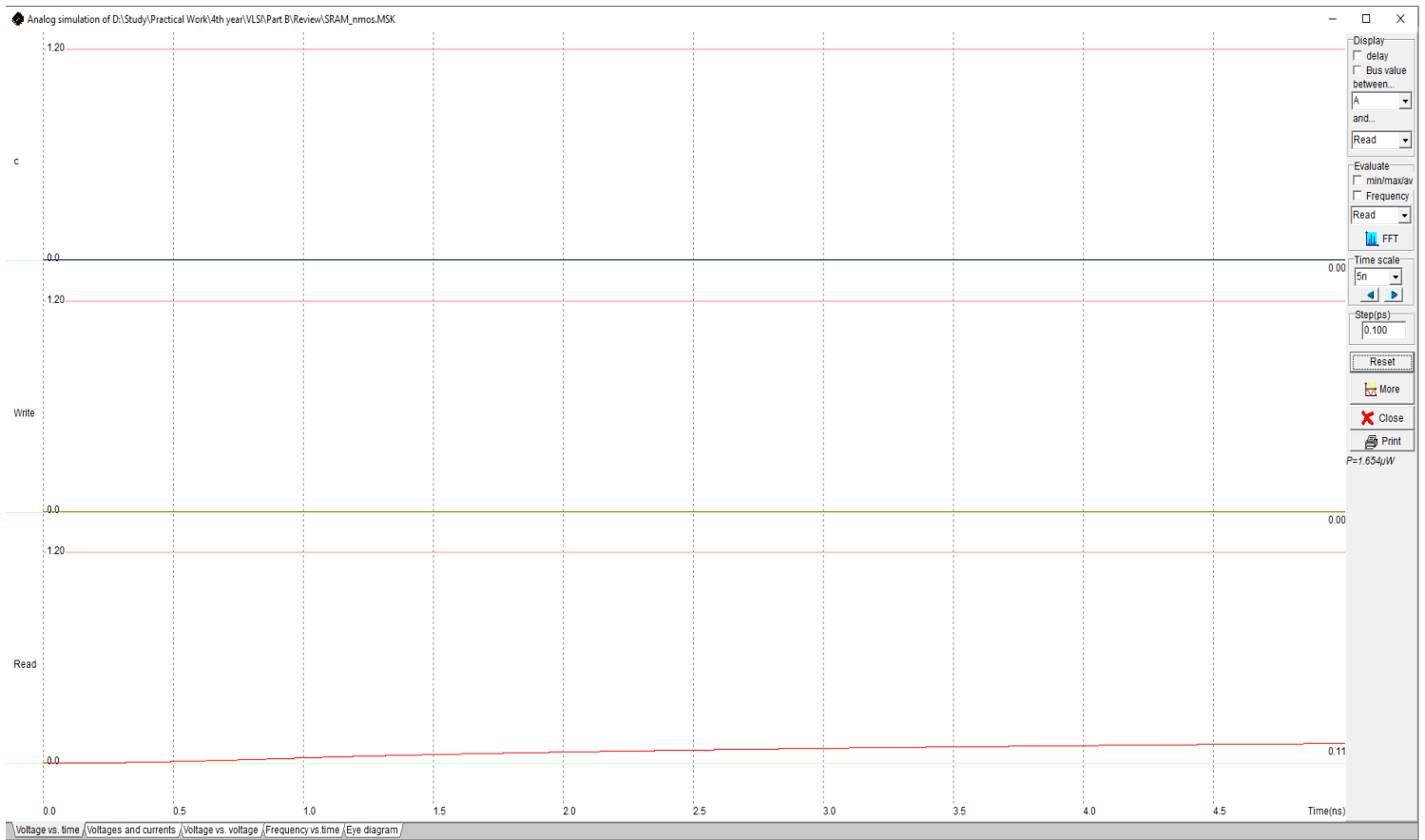
### a) Read output when $c = 1$ and Write = 0; Read = WEAK-1



### b) Read output when $c = 1$ and Write = 1; Read = STRONG-0

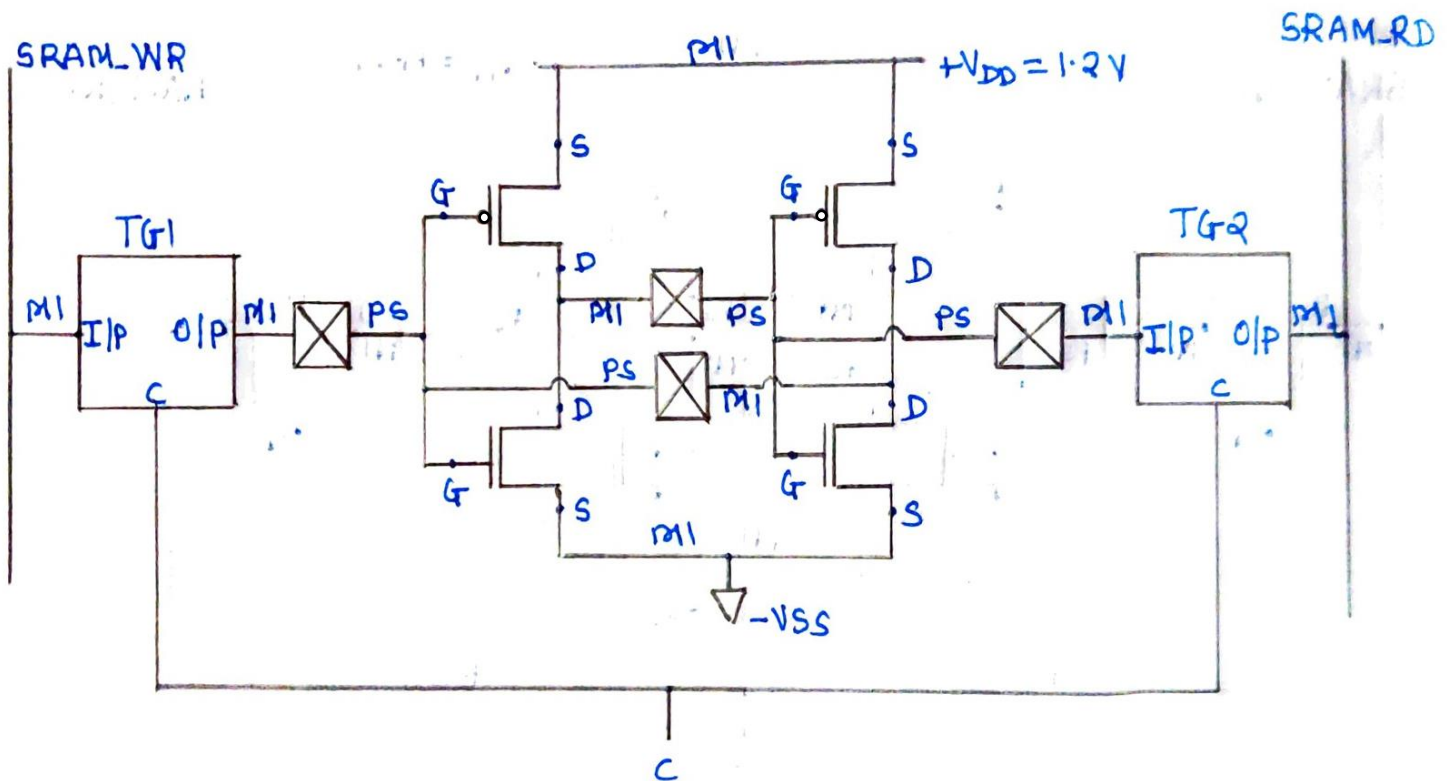


c) Read output when c = 0 and Write = 0; Read = HOLD



Theory:

3.b)- 1-bit SRAM cell using TG switches.

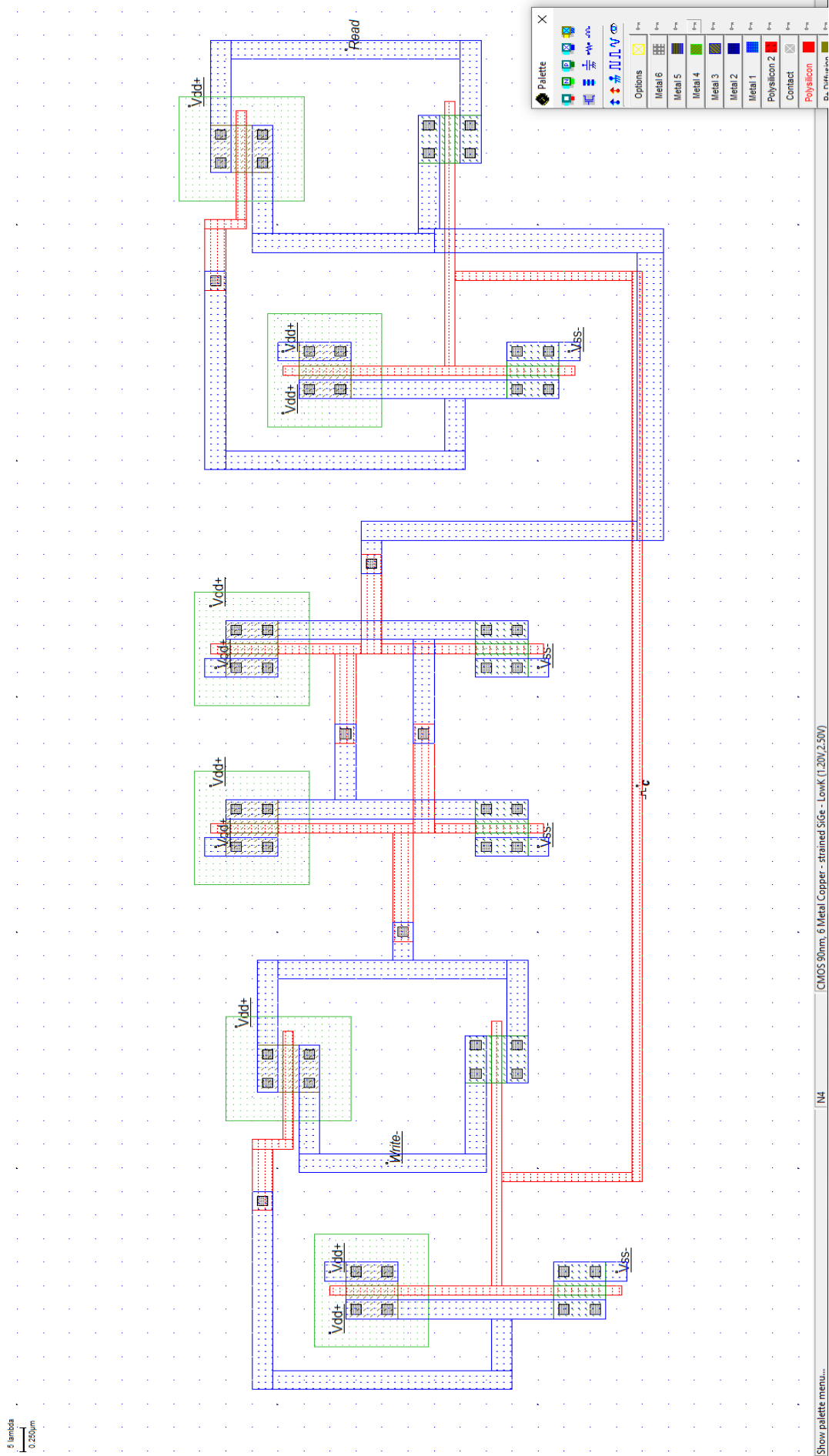


TG1, TG2 : Transmission Gate switches

Function Table-

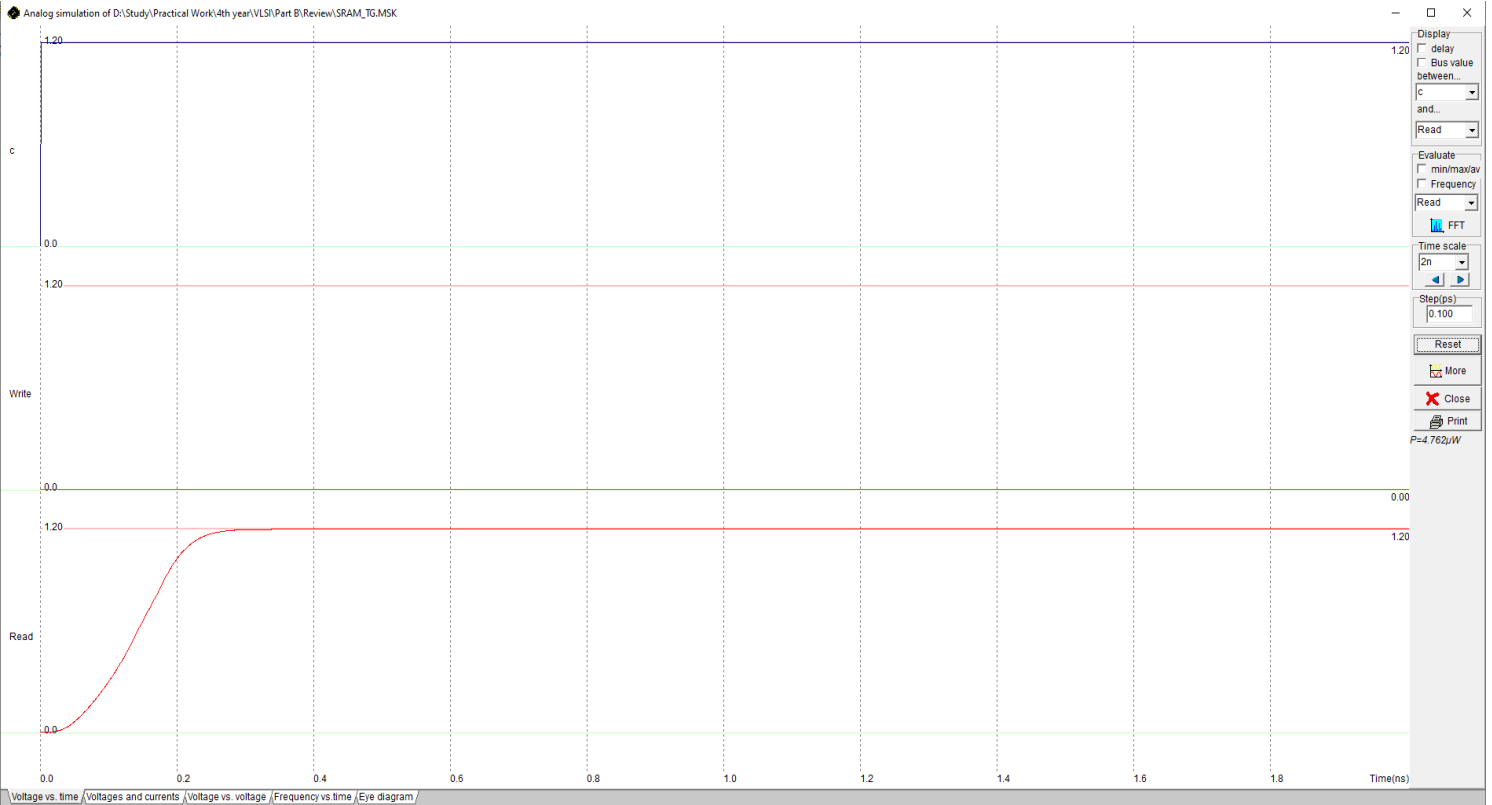
C	SRAM_WR	SRAM_RD
1	0	STRONG-1
1	1	STRONG-0
0	X	0/HOLD

# LAYOUT

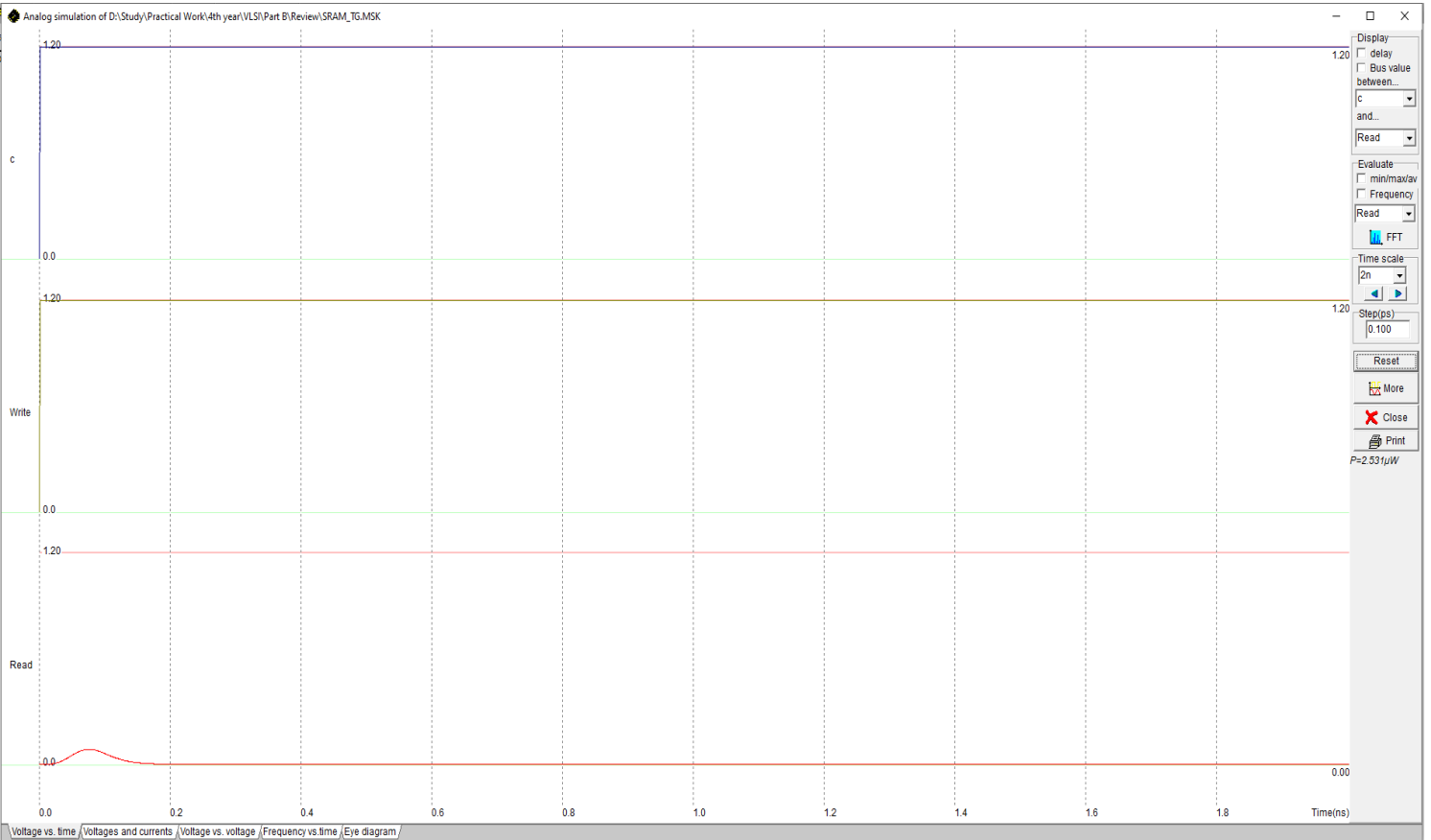


## Waveforms

a) Read output when  $c = 1$  and Write = 0; Read = STRONG-1

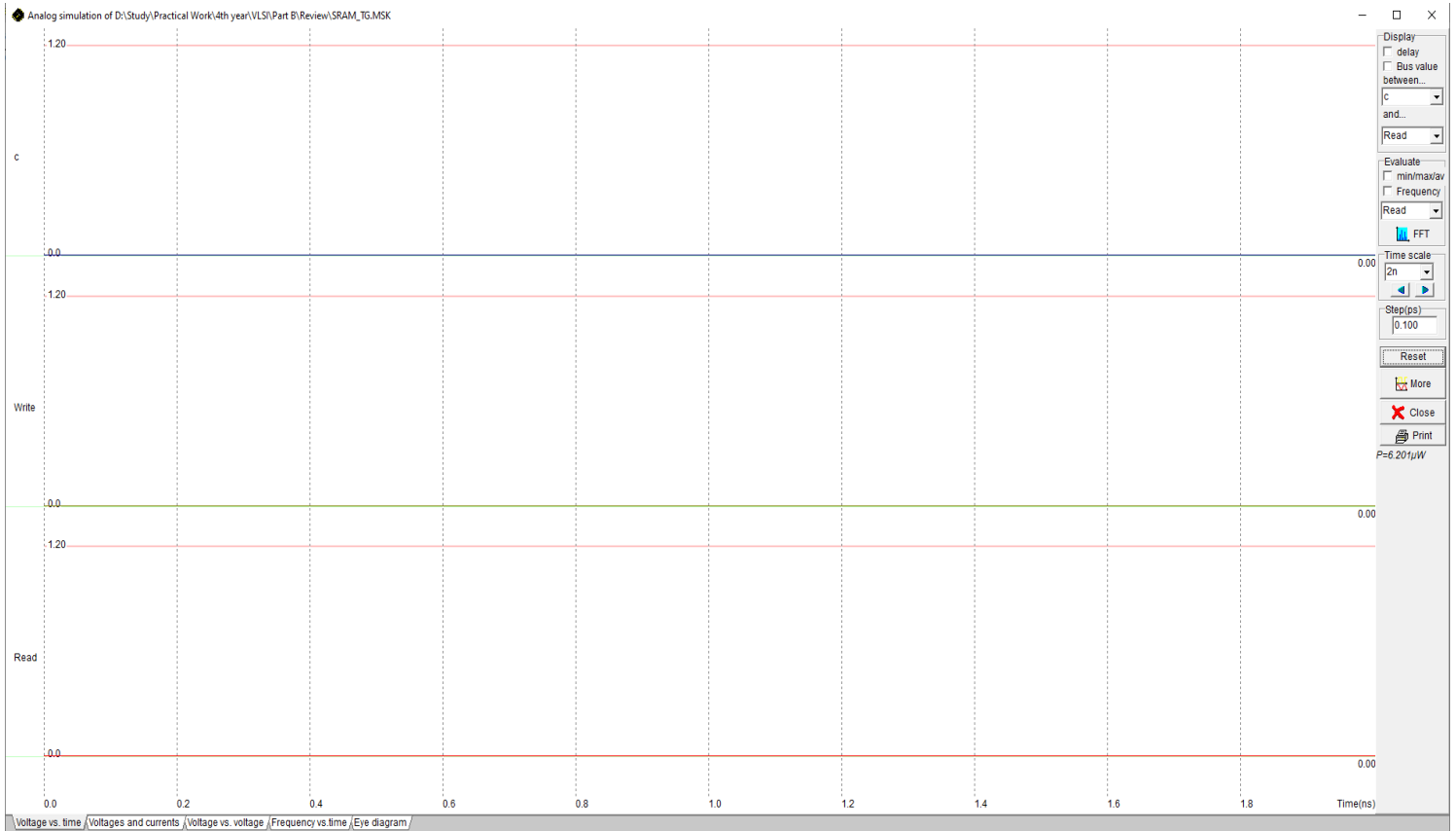


b) Read output when  $c = 1$  and Write = 1; Read = STRONG-0





**c) Read output when c = 0 and Write = 0; Read = HOLD**



**Conclusion:**

**Thus we have :**

- 1) Drawn the LAYOUT for 1-bit SRAM Cell using 2 CMOS Inverters and 2 NMOS Transistors for switching purpose, using 90 nm Foundry.
- 2) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.
- 3) Observed the inability of NMOS to provide STRONG 1 at the output.
- 4) To avoid the WEAK-1/WEAK-0 outputs while using NMOS and PMOS Switches respectively, replacing them with TG Switches gives STRONG-1 and STRONG-0 at the Read Line.
- 5) The only drawback of this circuit is that a complemented value of the data written is read.