**TITLE PAGE**

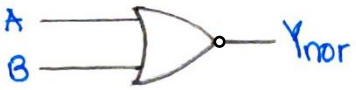
| | | |
|---|---|---|
| Class | : | BE - 8 |
| Roll. No | : | 42428 |
| Assignment No. | : | B. 1d , 1e |
| Assignment Name | : | 2 input CMOS NOR & OR Gates |
| Date Of Performance | : | 12-11-2020 |

**Theory**:

F = 90 nm

Symbols-

2 i/p NOR Gate




$Y_{nor} = \overline{A+B}$

2 i/p OR Gate.

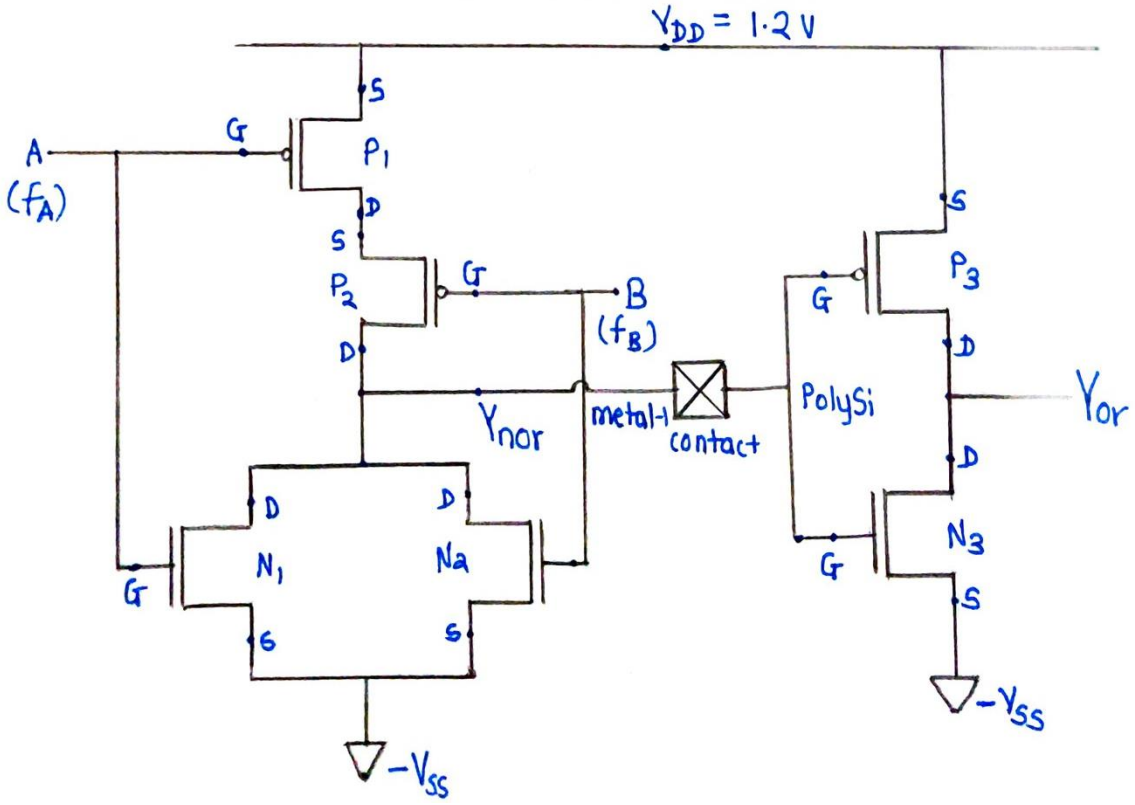

$Y_{or} = A+B$

## Truth Tables

| A | B | $Y_{nor}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

| A | B | $Y_{or}$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

## Combined Schematic



$f_B = 2f_A$

Size of each PMOS Transistor (P1, P2, P3)

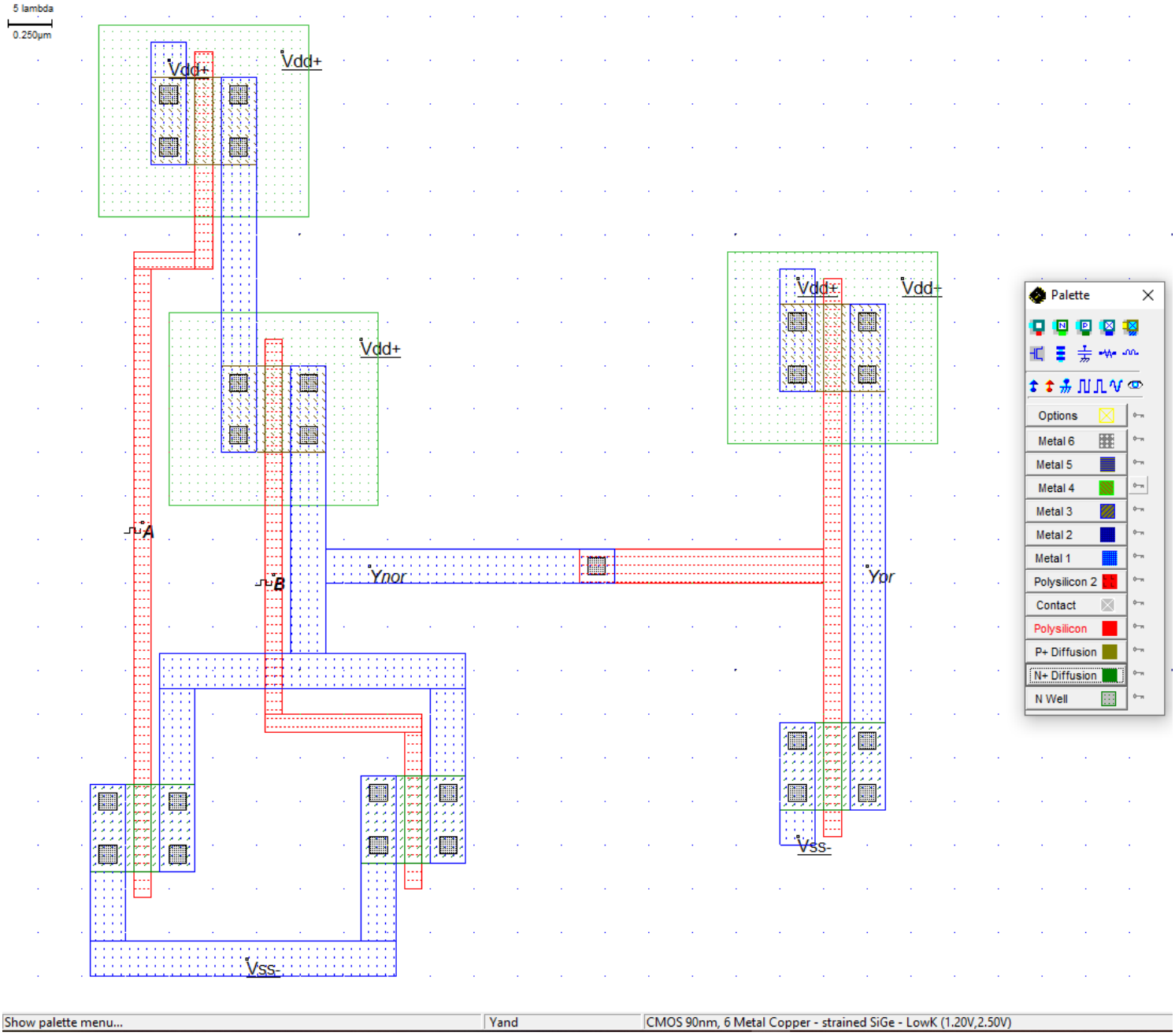
$$P = \left(\frac{500}{100}\right) nm = 5$$

Size of each NMOS Transistor (N1, N2, N3)

$$n = \left(\frac{500}{100}\right) nm = 5$$

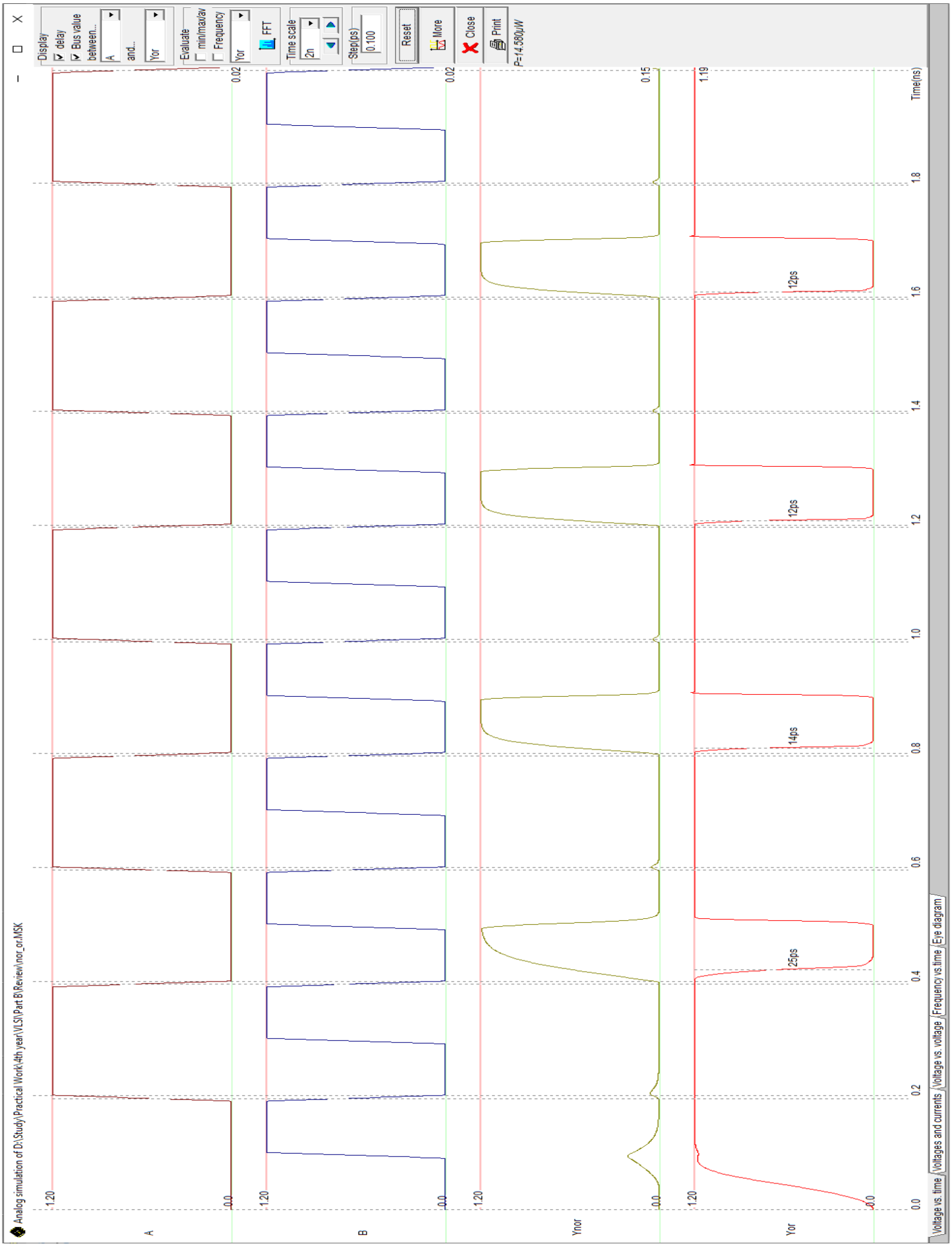
Relative Size $= \frac{P}{n} = 1$

# LAYOUT




Show palette menu... | Yand | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

# Waveforms


Analog simulation of D:\Study\Practical Work\4th year\VLSI\Part B\Review\nor_or.MSK
Display
delay
Bus value
between...
A
and...
Yor
Evaluate
min/max/av
Frequency
Yor
FFT
Time scale
2n
Step(ps)
100
Reset
More
Close
Print
P=14.580µW
A
B
Ynor
Yor
1.20
0.0
0.02
0.15
1.19
12ps
14ps
25ps
Time(ns)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

**Conclusion**:

**Thus we have :**

1) Drawn the LAYOUT for CMOS NOR & OR Gates using 90 nm Foundry.
2) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.