TITLE PAGE

Class	:	BE - 8
Roll. No	:	42428
Assignment No.	:	B. 1b , 1c
Assignment Name	:	2 input CMOS NAND & AND Gates
Date Of Performance	:	12-11-2020

Theory:

F = 90 nm

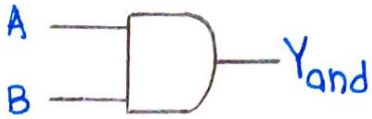
Symbols

2 i/p nand gate

$Y_{nand} = \overline{A \cdot B}$

A	B	Y_{nand}
0	0	1
0	1	1
1	0	1
1	1	0

2 i/p AND gate.

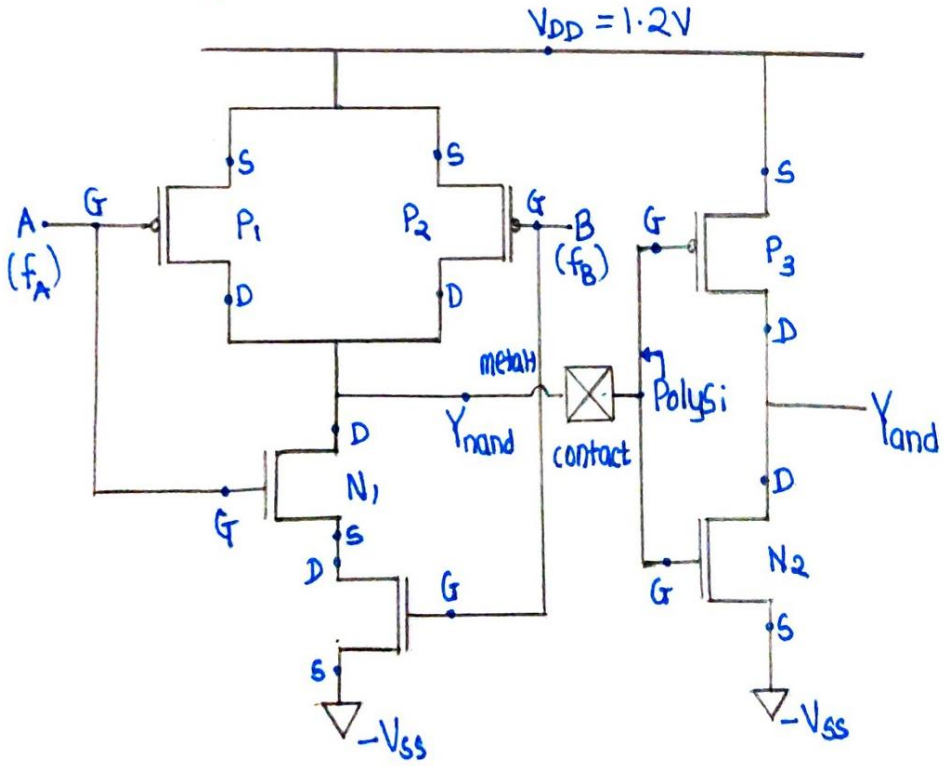


$Y_{and} = A \cdot B.$

A	B	Y_{and}
0	0	0
0	1	0
1	0	0
1	1	1

Truth Tables

Combined Schematic.



$f_B = 2f_A$

Size of each PMOS Transistor (P1, P2, P3)

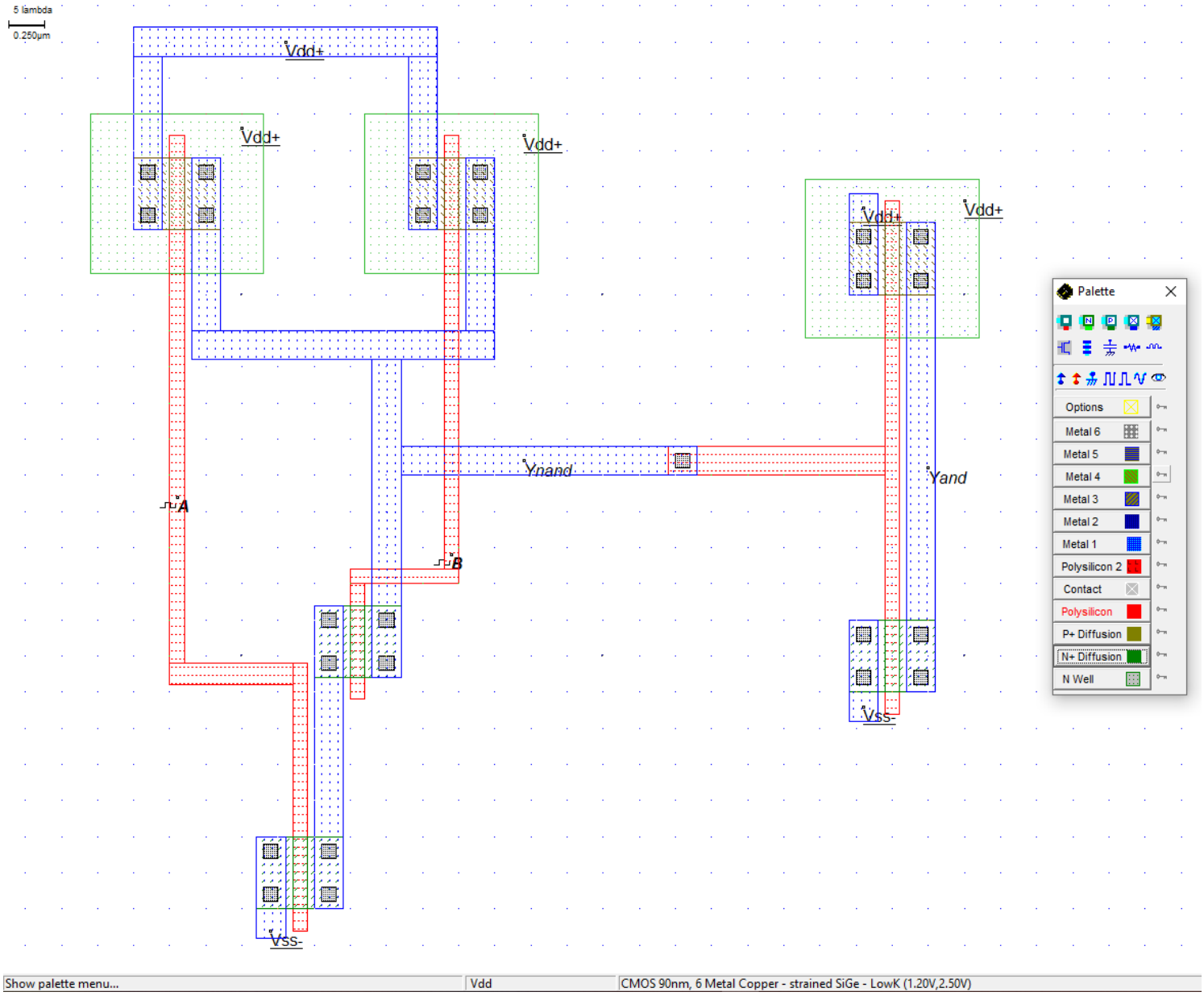
$$P = \left(\frac{500}{100}\right) nm = 5$$

Size of each NMOS Transistor (N1, N2, N3)

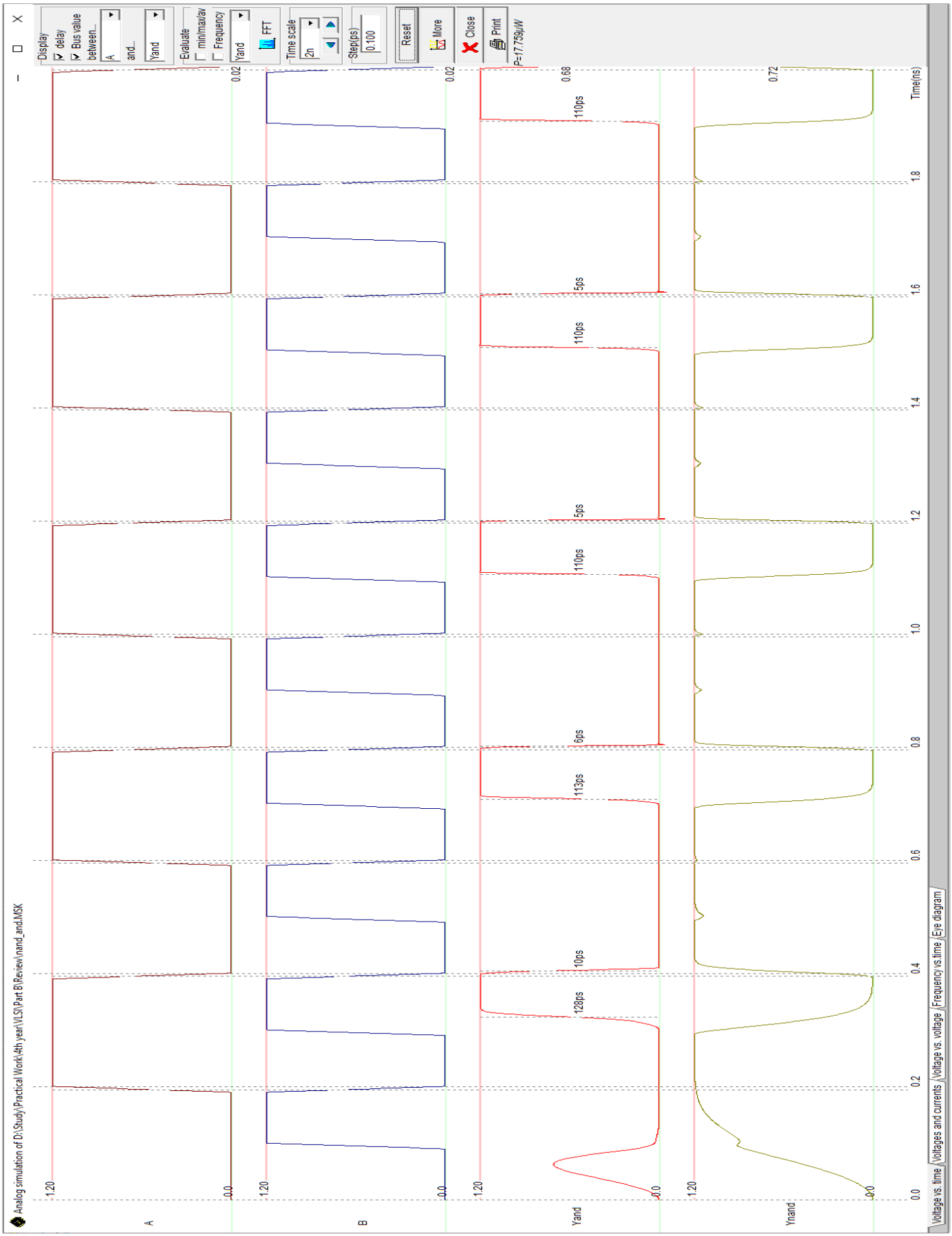
$$n = \left(\frac{500}{100}\right) nm = 5$$

Relative Size $= \frac{P}{n} = 1$

LAYOUT


5 lambda
0.250µm
Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
Ynand
Yand
A
B
Vss-
Vss-
Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
Show palette menu...
Vdd
CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

Waveforms


Analog simulation of D:\Study\Practical Work\4th year\VLSI\Part B\Review\nand_and.MSK
Display
delay
Bus value between...
A
and...
Ynand
Evaluate
min/max/av
Frequency
Yand
FFT
Time scale
2n
Step(ps)
0.100
Reset
More
Close
Print
P=17.759µW
A
B
Yand
Ynand
1.20
0.0
0.02
0.68
0.72
110ps
5ps
6ps
113ps
10ps
128ps
Time(ns)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

Conclusion:

Thus we have :

1) Drawn the LAYOUT for CMOS NAND & AND Gates using 90 nm Foundry.
2) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.