TITLE PAGE

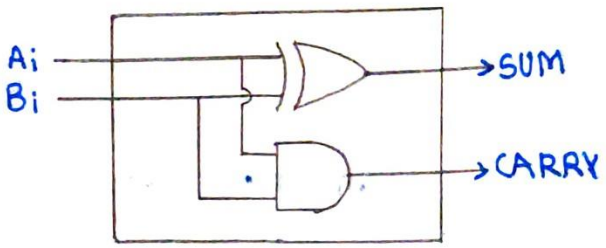
Class	:	BE - 8
Roll. No	:	42428
Assignment No.	:	B. 1f
Assignment Name	:	Half Adder Using TG
Date Of Performance	:	21-11-2020

Theory:

F = 90 nm.

Symbol.

Gate Level Schematic



$SUM = A_i \oplus B_i$

$CARRY = A_i \cdot B_i$

Truth Table-

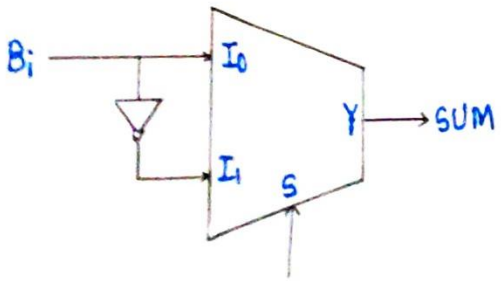
A_i	B_i	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Approach-

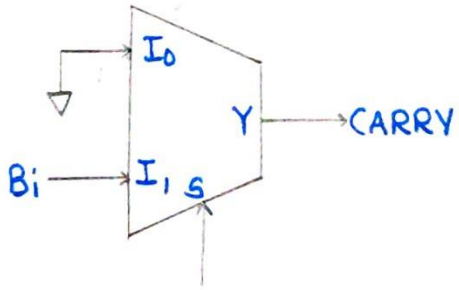
- Half adder is made up of Ex-OR & AND gates for sum & carry resp.
- Ex-OR & AND gates will be implemented using a 2:1 MUX each.
- A 2:1 MUX is implemented using 2 TG's.

- For Schematic of 2:1 MUX using TG, review assign?

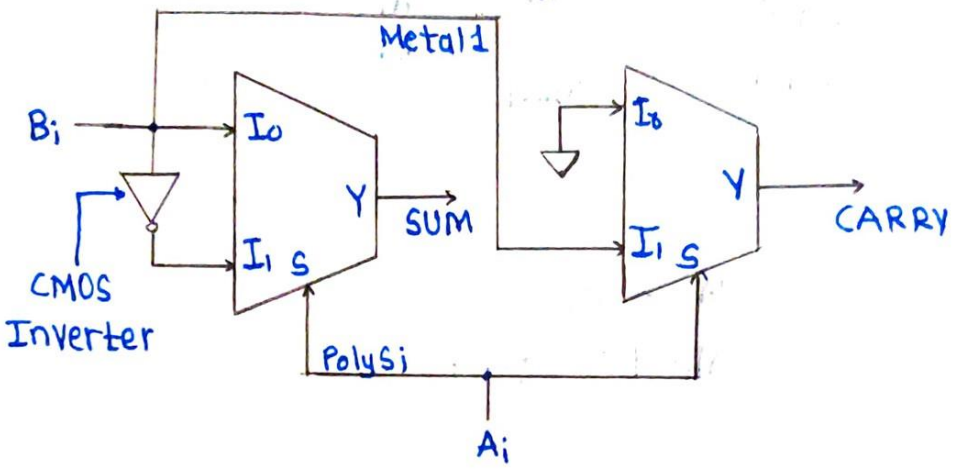
MUX-1 (Ex-OR Gate)

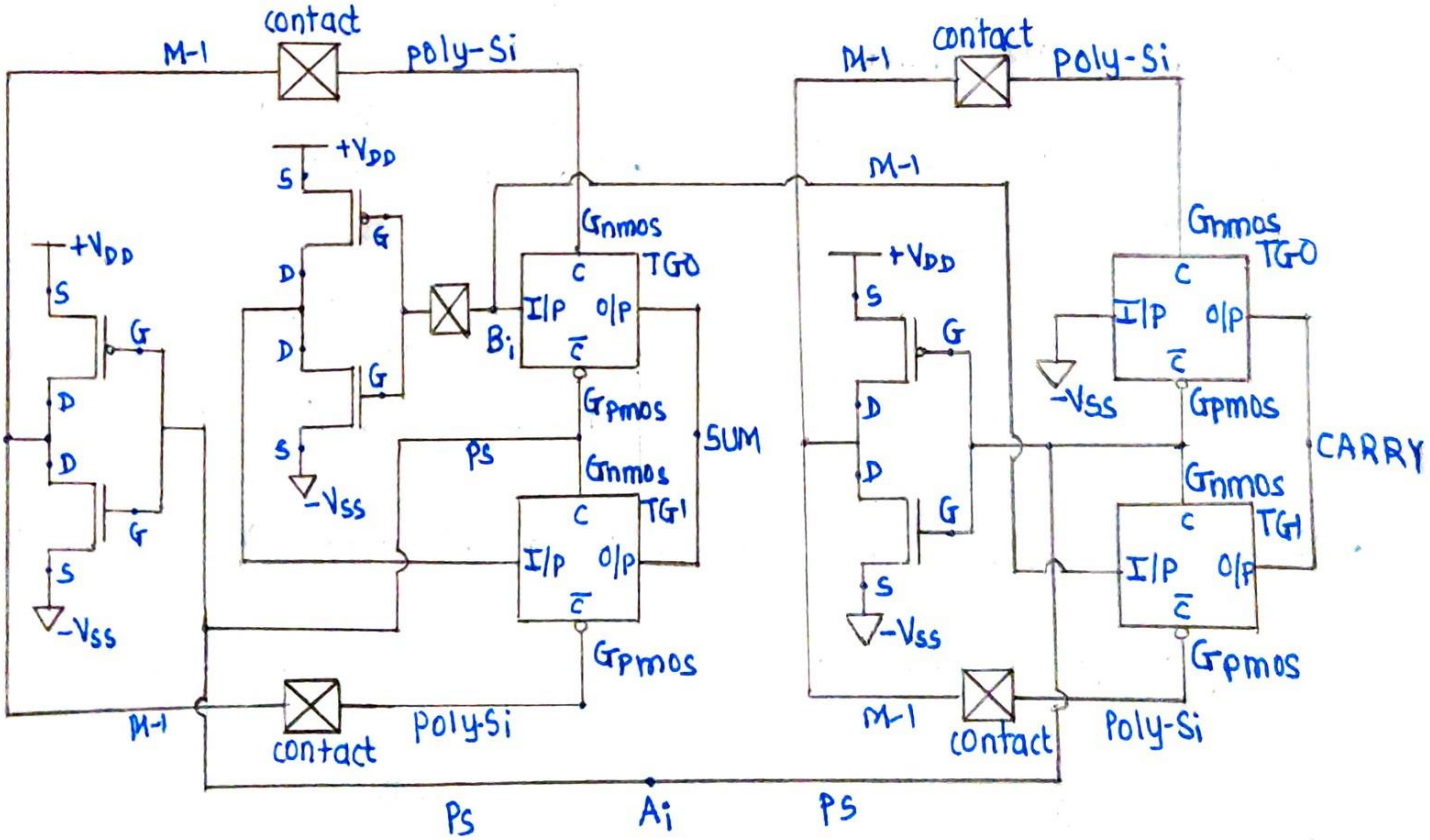


MUX-2 (AND Gate)

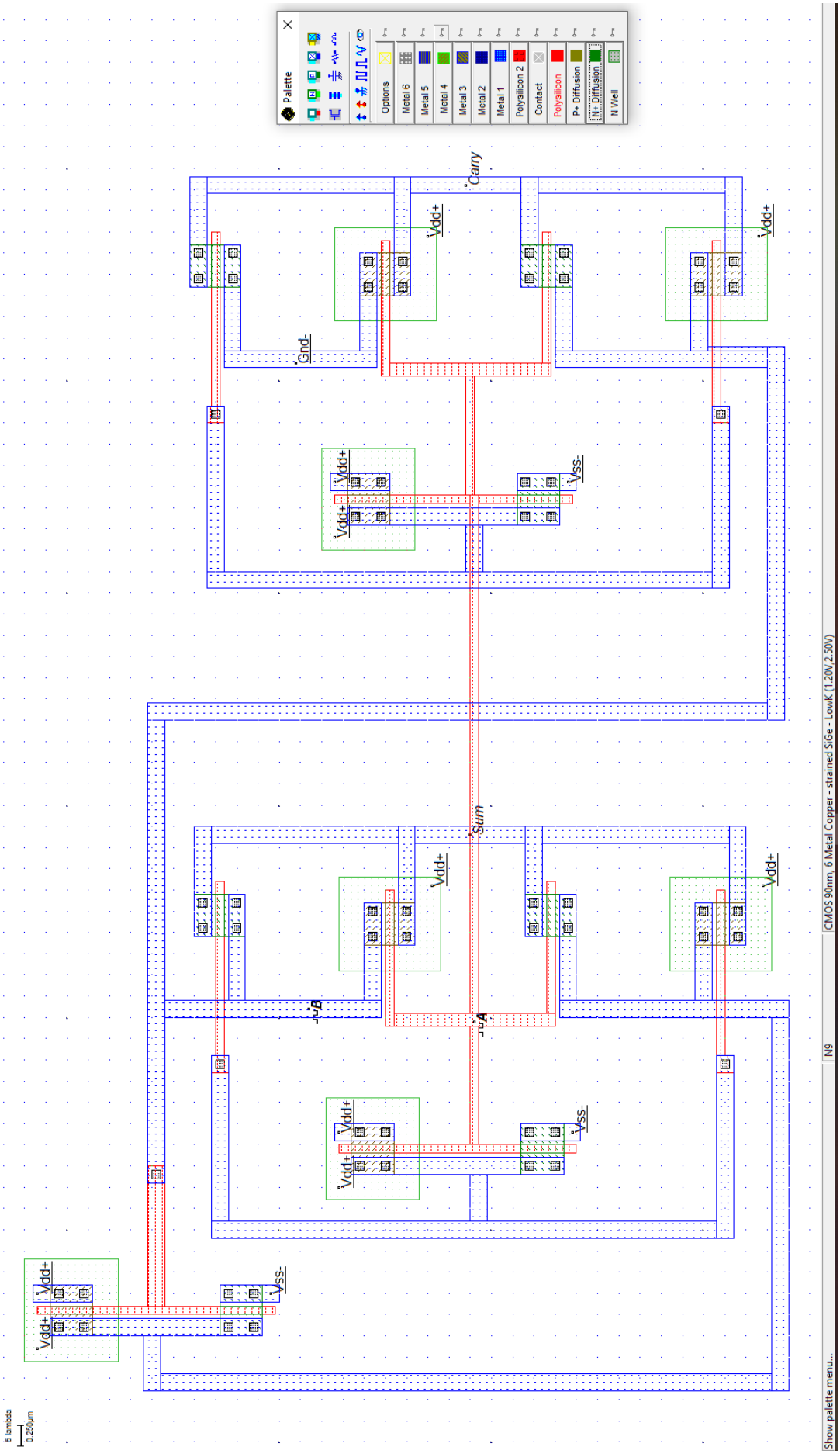


Combined Schematic

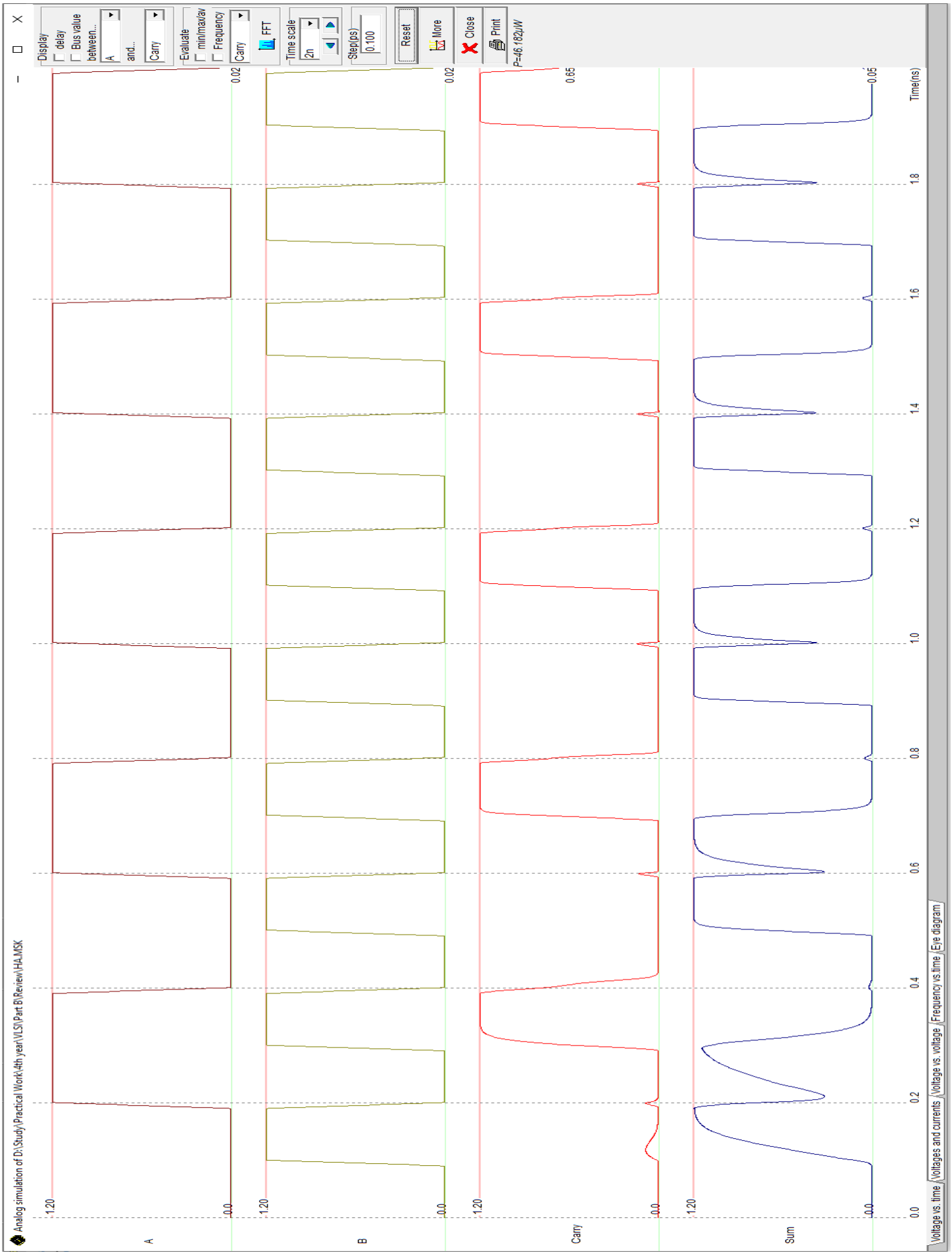




LAYOUT


Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
Carry
Sum
Vdd+
Vss-
Gnd-
B
A
5 lambda
0.250µm
Show palette menu...
N9
CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

Waveforms


Analog simulation of D:\Study\Practical Work\4th year\VLSI\Part B\Review\HA.MSK
Display
delay
Bus value
between...
A
and...
Carry
Evaluate
min/max/av
Frequency
Carry
FFT
Time scale
2n
Step(ps)
0.100
Reset
More
Close
Print
P=46.182µW
A
B
Carry
Sum
1.20
0.0
0.02
0.65
0.05
Time(ns)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs. time
Eye diagram

Conclusion:

Thus we have :

1) Drawn the LAYOUT for Half Adder using Transmission Gates and 90 nm Foundry.
2) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.