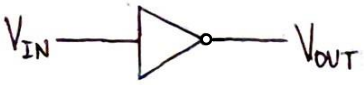
TITLE PAGE

Class	:	BE – 8
Roll. No	:	42428
Assignment No.	:	B. 1a
Assignment Name	:	CMOS Inverter and Analysis
Date Of Performance	:	03-11-2020 & 21-11-2020

Theory:

Symbol.



Truth Table

V_{IN}	$V_{OUT} = \overline{V_{IN}}$
0	STRONG-1
1	STRONG-0

	O/P	Value of V_{OUT} (V)
1)	STRONG-1	$+V_{DD}$
2)	WEAK-1	$< +V_{DD}$
3)	STRONG-0	$-V_{SS}$ (0)
4)	WEAK-0	>0

$$P_{dyn} = C_L (V_{DD})^2 f$$

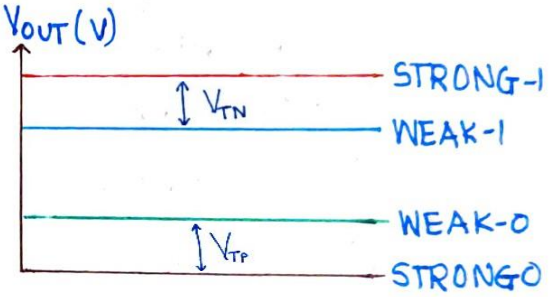
$\rightarrow P_{dyn} \propto C_L$

$\rightarrow P_{dyn} \propto (V_{DD})^2$

$\rightarrow P_{dyn} \propto f$

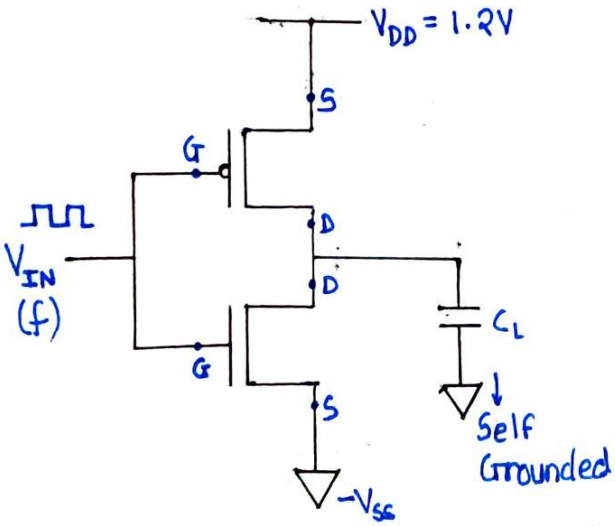
For 90nm Foundry

$V_{DD} = +1.2\,V$

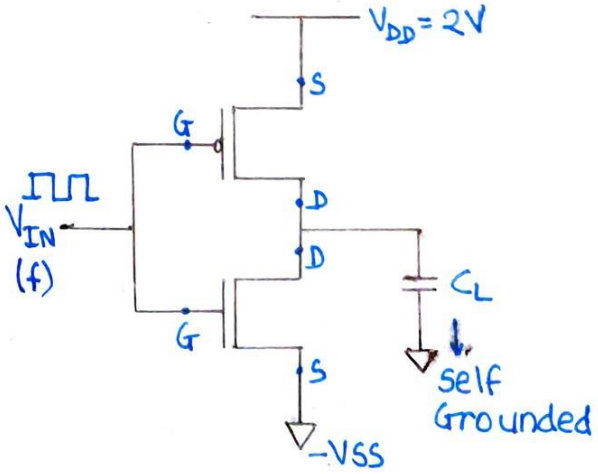


Schematics

F = 90 nm



F = 180nm



$$p = \frac{W_p}{L_p} = \left(\frac{500}{100}\right)nm = 5$$

$$n = \frac{W_n}{L_n} = \left(\frac{500}{100}\right)nm = 5$$

$$\frac{p}{n} = 1$$

Nominal values-

$C_L = 0.01\,pF$

$f = 2.5\,GHz$

$C_L' = 0.005\,pF$

$C_L'' = 0.02\,pF$

$f' = 1.25\,GHz$

$f'' = 5\,GHz$

$$p = \frac{W_p}{L_p} = \left(\frac{1000}{200}\right)nm = 5$$

$$n = \frac{W_n}{L_n} = \left(\frac{1000}{200}\right)nm = 5$$

$$\frac{p}{n} = 1$$

Nominal Values

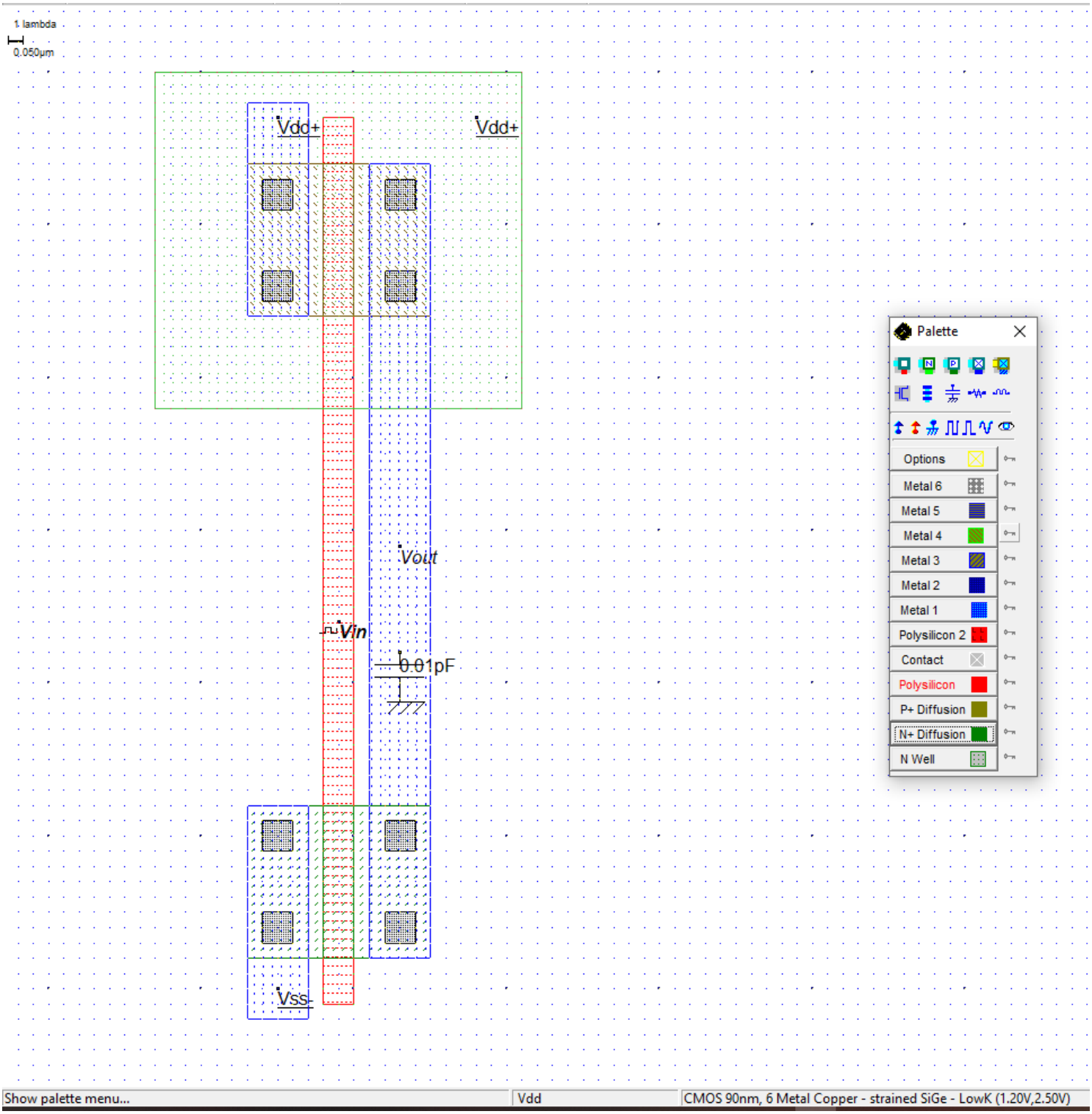
$C_L = 0.01\,pF$

$f = 2.5\,GHz$

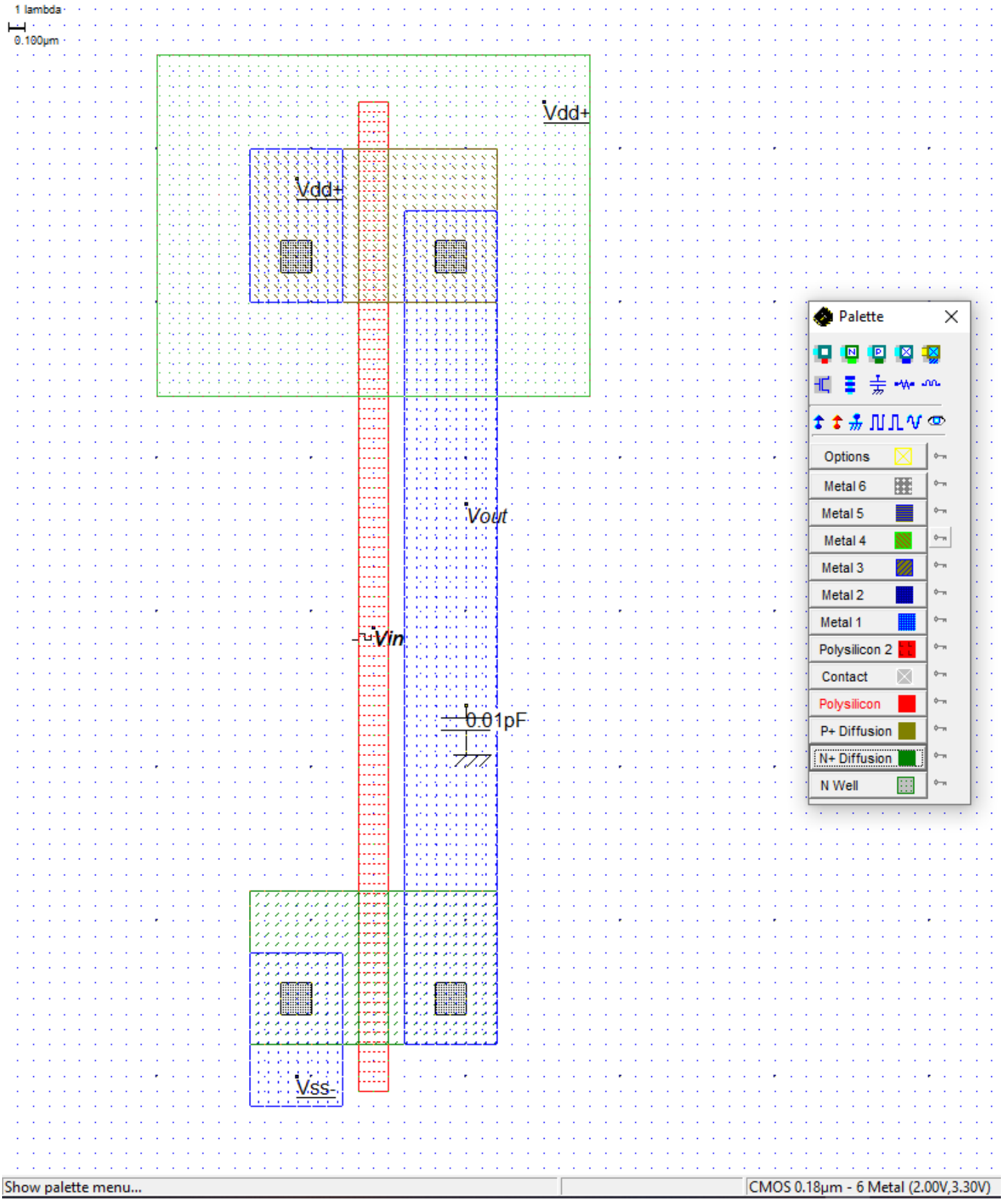
C_L & f are not varied.

LAYOUT

a) CMOS Inverter with 90 nm Foundry



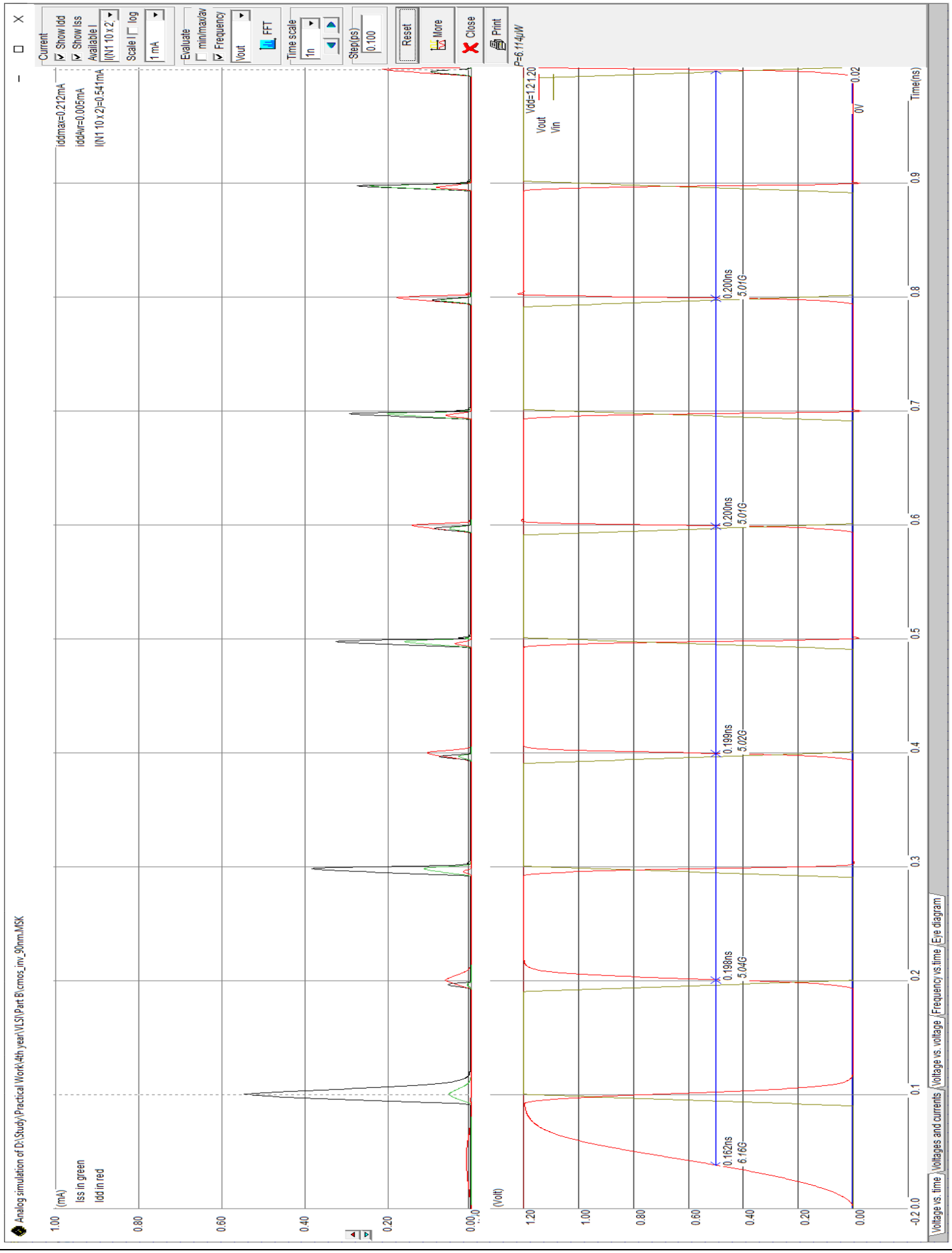
b) CMOS Inverter with 180 nm Foundry



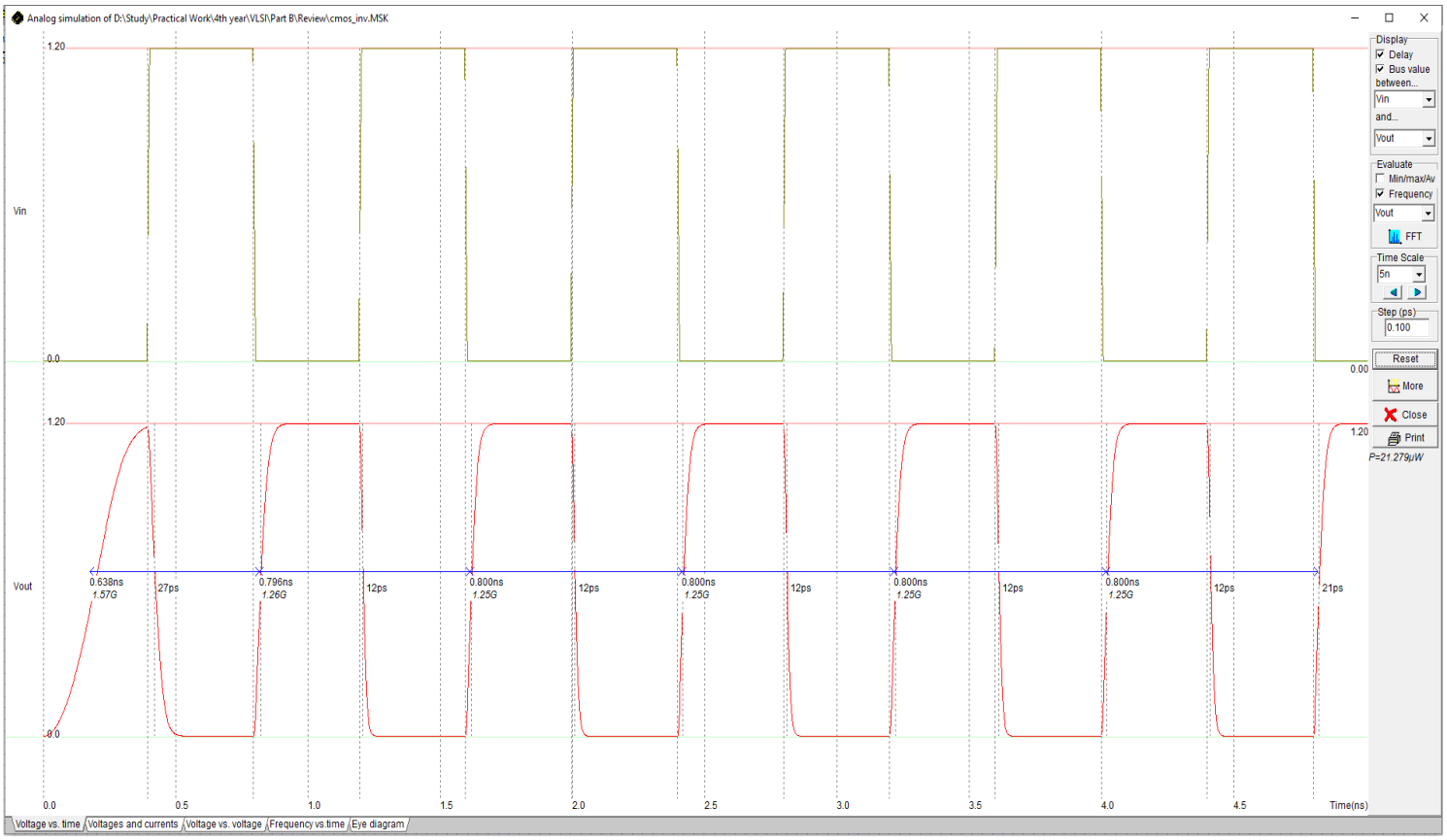
Waveforms

a) Vin , Vout

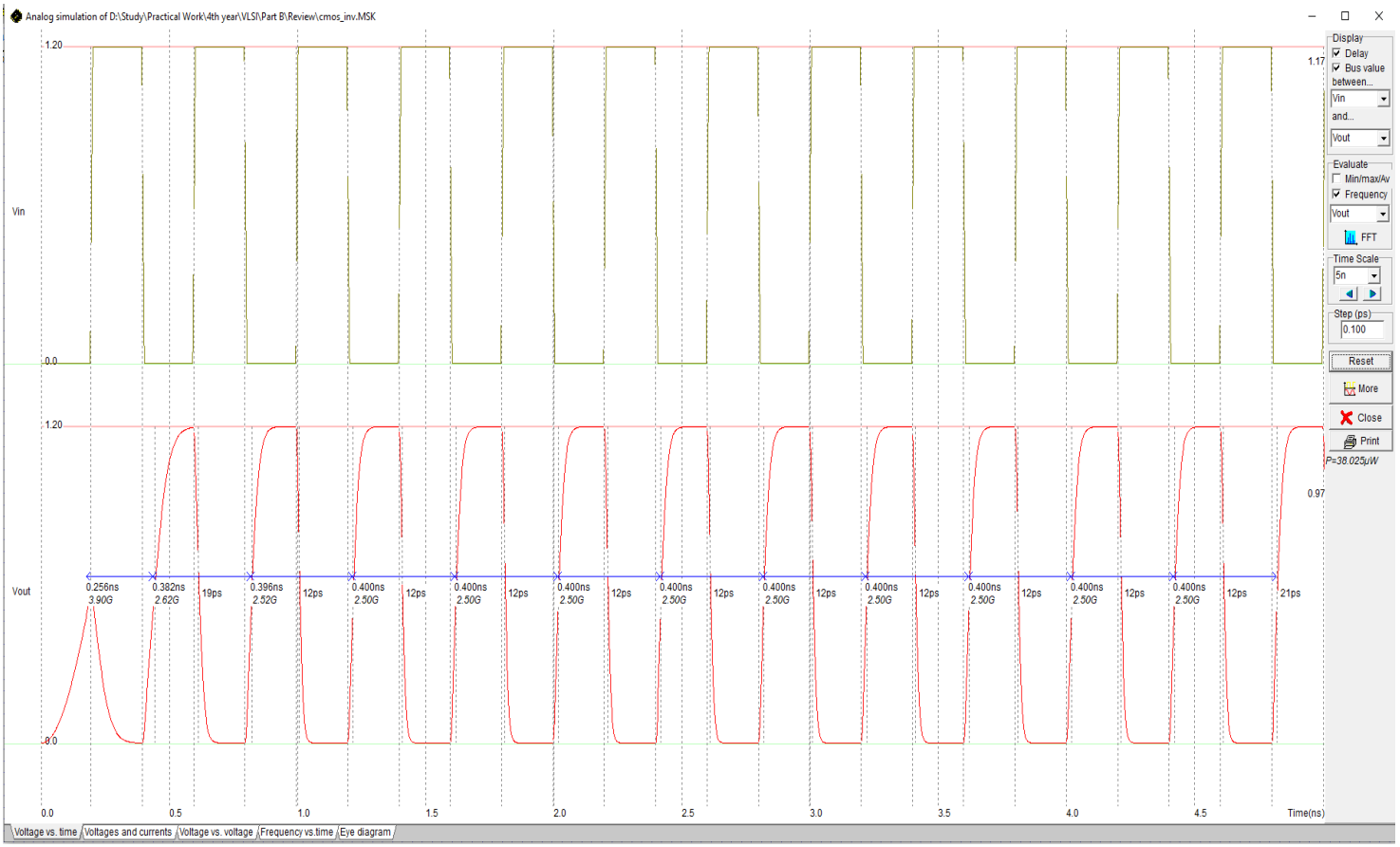
b) Vout , Iout


Analog simulation of D:\Study\Practical Work\4th year\VLSI\Part B\cmos_inv_90nm.MSK
Current
Show Idd
Show Iss
Available I
I(N1 10 x 2
Scale I
log
1 mA
Evaluate
min/max/av
Frequency
Vout
FFT
Time scale
1n
Step(ps)
0.100
Reset
More
Close
Print
iddmax=0.212mA
iddAvr=0.005mA
I(N1 10 x 2)=0.541mA
(mA)
Iss in green
Idd in red
P=6.114µW
Vdd=1.2
1.20
Vout
Vin
0.162ns
6.16G
0.198ns
5.04G
0.199ns
5.02G
0.200ns
5.01G
0.200ns
5.01G
0V
0.02
(Volt)
Time(ns)
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

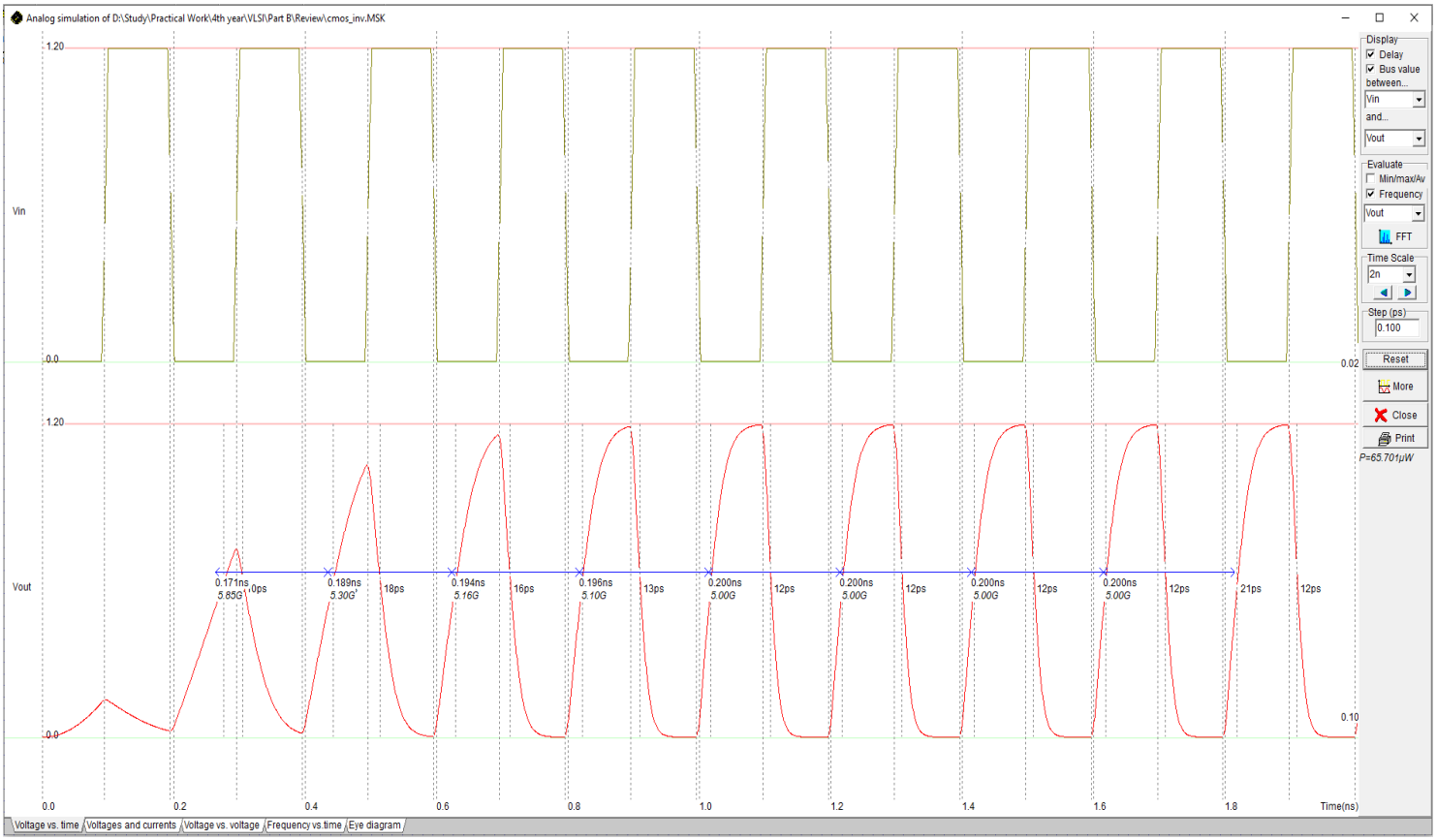
c) f_{clk} = 1.25 GHz , C_L = 0.01 pF , V_{DD} = 1.2 V



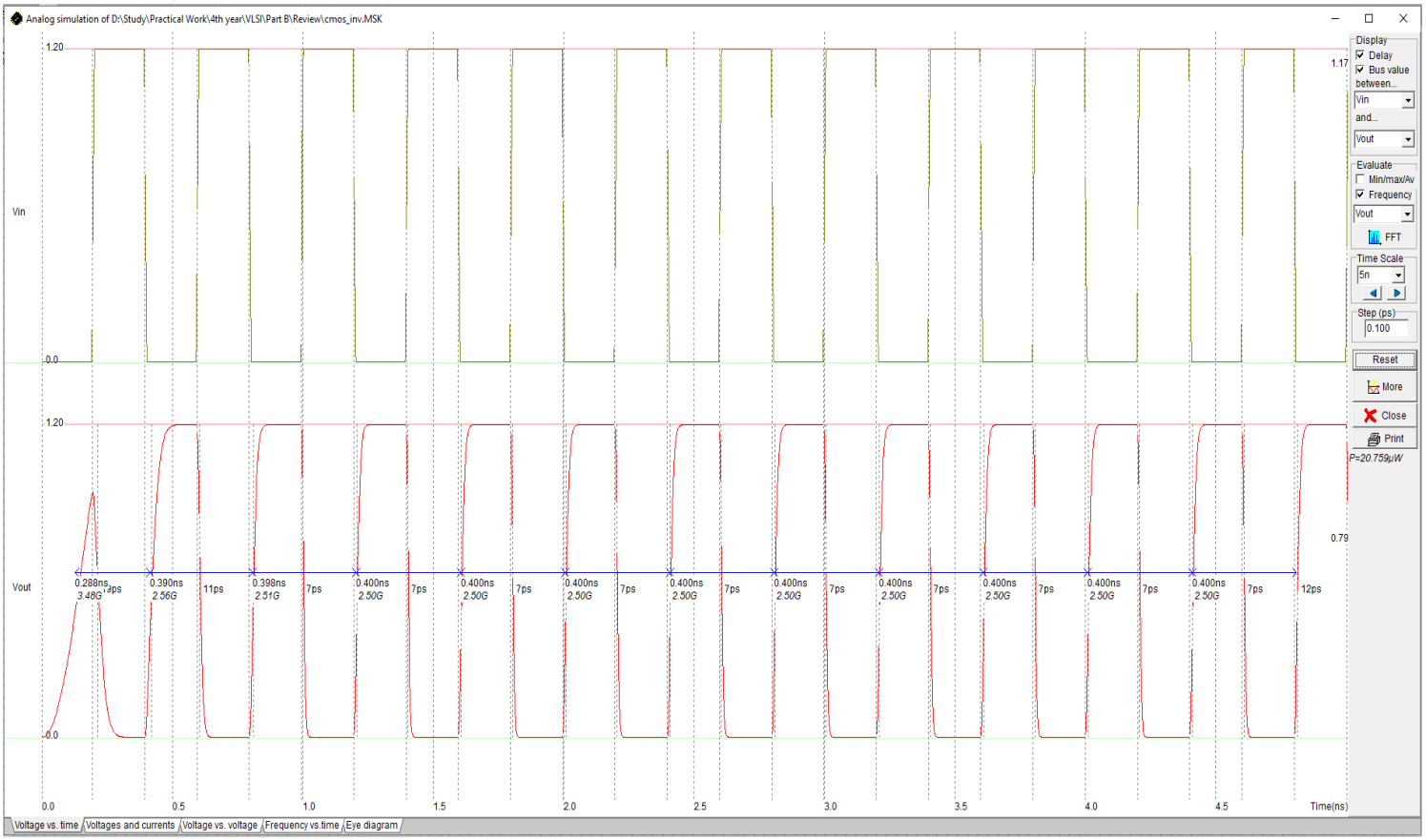
d) f_{clk} = 2.5 GHz , C_L = 0.01 pF , V_{DD} = 1.2 V



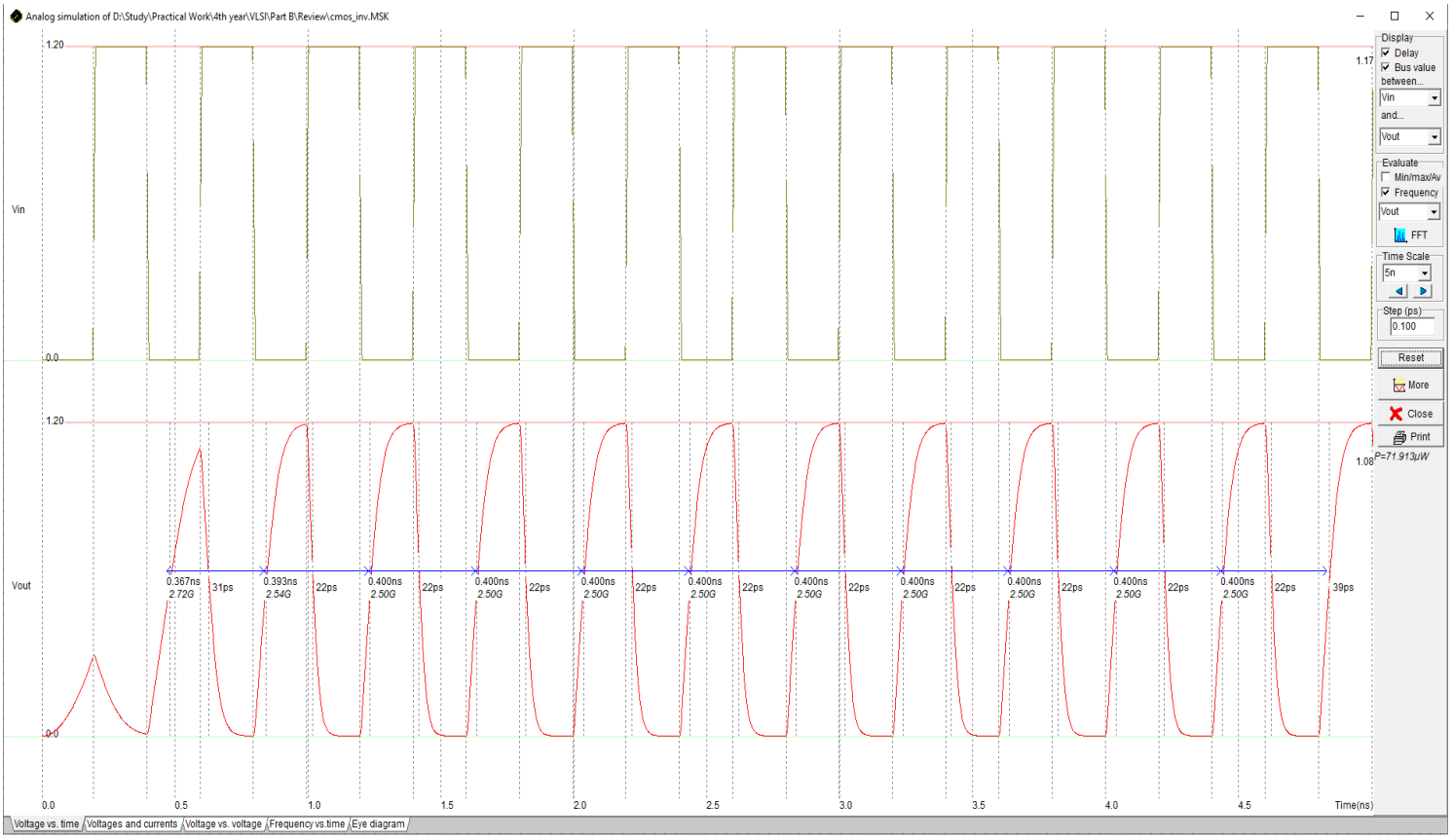
e) f_{clk} = 5 GHz , C_L = 0.01 pF , V_{DD} = 1.2 V



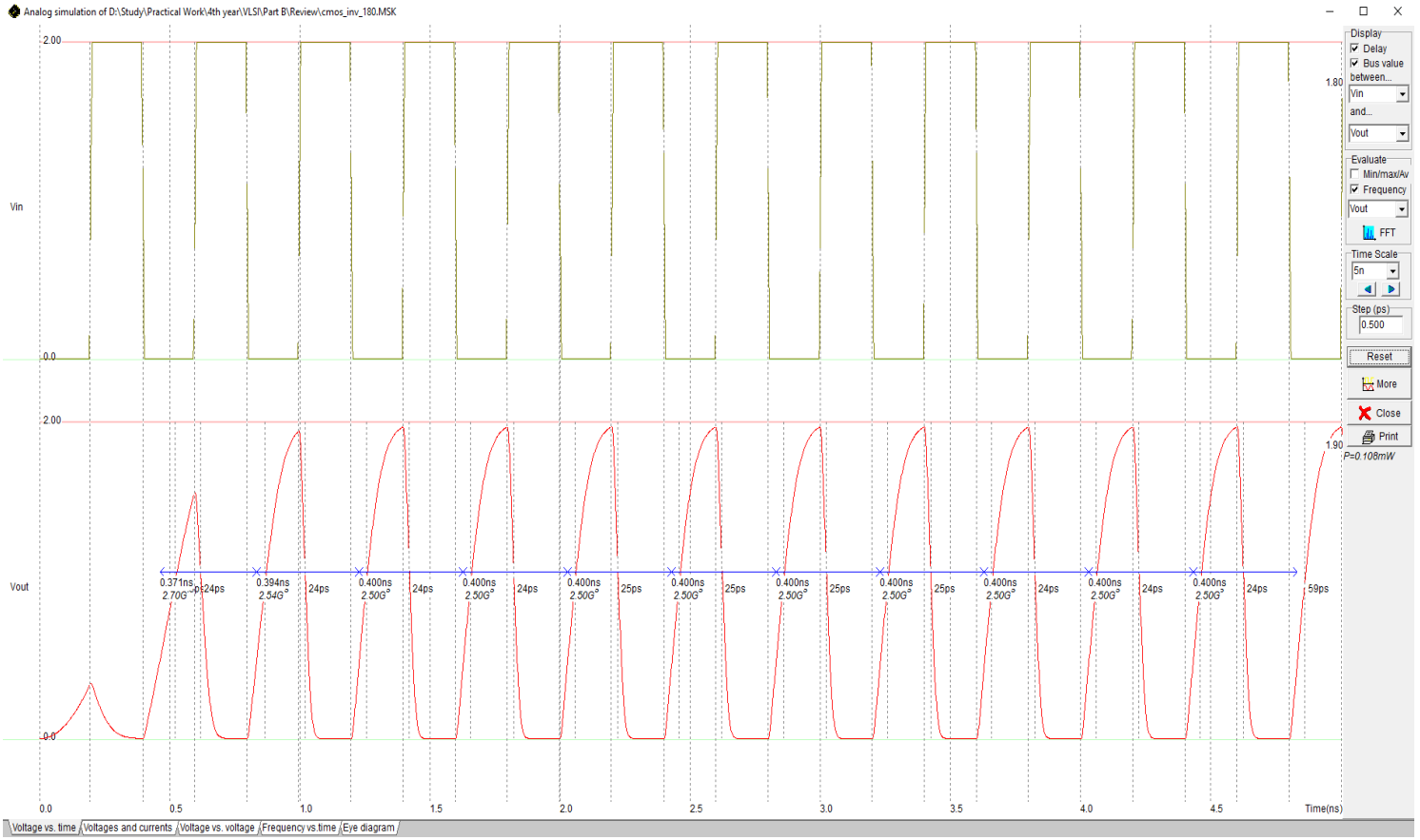
f) f_{clk} = 2.5 GHz , C_L = 0.005 pF , V_{DD} = 1.2 V



g) f_{clk} = 2.5 GHz , C_L = 0.02 pF , V_{DD} = 1.2 V



h) f_{clk} = 2.5 GHz , C_L = 0.01 pF , V_{DD} = 2 V



PERFORMANCE ANALYSIS

OT-1 :- $f_{CLK} = 2.5$ GHz , $V_{dd} = 1.2$ V (90 nm)

C_L (pF)	P_{dyn} (μW)
0.005	20.759
0.01	38.025
0.02	71.913

OT-2 :- $C_L = 0.01$ pF , $V_{dd} = 1.2$ V (90nm)

f_{CLK} (GHz)	P_{dyn} (μW)
1.25	21.279
2.5	38.025
5	65.701

OT-3 :- $f_{CLK} = 2.5$ GHz , $C_L = 0.01$ pF

V_{dd} (V)	P_{dyn} (μW)
1.2	38.025
2	108

$$\frac{P_{dyn2}}{P_{dyn1}} = \left[\frac{V_{dd2}}{V_{dd1}}\right]^2 = \left[\frac{2}{1.2}\right]^2 = 2.78$$

Conclusion:

Thus we have :

1) Drawn the LAYOUT for CMOS Inverter using 90 nm & 180 nm Foundry.
2) Simulated the LAYOUT to observe waveforms & verified its functionality as per TRUTH-TABLE.
3) Noted the values of $P_{dynamic}$ for floating Load.
4) Appreciated the validity of the mathematical model : $P_{dyynamic} = C_L * (Vdd)^2 * f_{clk}$; by Doubling & Halving the values of C_L & f_{clk}
5) Found a reduction in $P_{dynamic}$ by using a better Foundry i.e. 90 nm instead of 180 nm.
6) Learnt that the presence of spikes in O/P waveform at Switching instants indicate the inability of the MOSFETs to switch at GHz frequencies.
7) Learnt that the using a better Foundry enables the MOSFETs the inability of the MOSFETS to switch at Higher GHz frequencies, as proved by the removal of Spikes at the O/P.