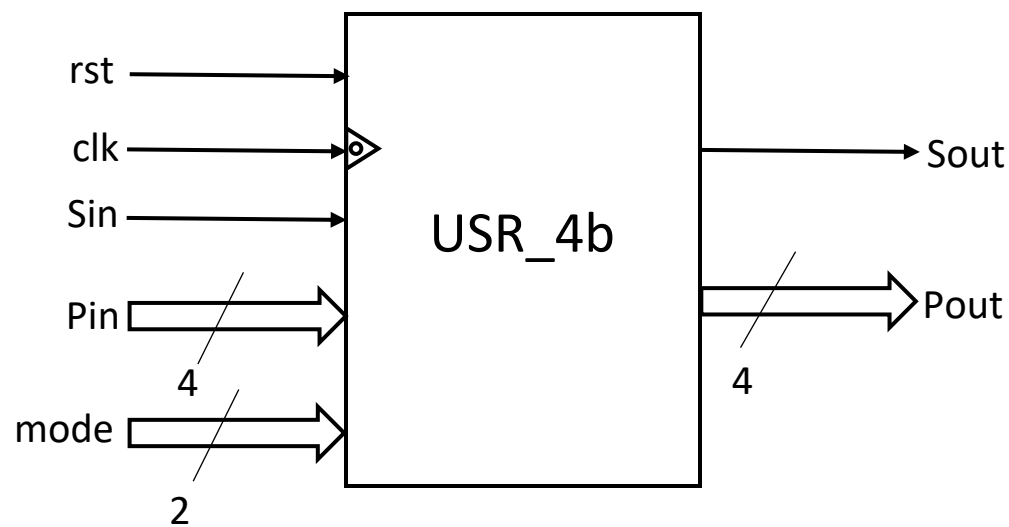






TITLE PAGE

Class	:	BE - 8
Roll. No	:	42428
Assignment No.	:	A. 2
Assignment Name	:	4 bit USB
Date Of Performance	:	19-9-2020 to 3-10-2020

Block Diagram:



Truth-Table :

rst	clk	mode	outputs
1	x	x	Sout = 0 Pout = 0000
0		00	SISO
0		01	SIPO
0		10	PISO
0		11	PIPO

MAIN VHDL PROGRAM

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;

entity USR_4b is
    Port ( rst : in  STD_LOGIC;
          clk : in  STD_LOGIC;
          Sin : in  STD_LOGIC;
          Pin : in  STD_LOGIC_VECTOR (3 Downto 0);
          mode : in  STD_LOGIC_VECTOR (1 downto 0);
          Sout : out STD_LOGIC;
          Pout : out STD_LOGIC_VECTOR (3 downto 0));
end USR_4b;

architecture USR_4b_arch of USR_4b is

    SIGNAL temp : STD_LOGIC_VECTOR(3 DOWNT0 0):="0000" ;
    SIGNAL flag : STD_LOGIC:='0';

begin
    PROCESS(rst, clk, mode, Sin, Pin)
    BEGIN
        IF rst='1' THEN
            temp <= "0000";
            Sout <= '0';
            Pout <= "0000";
            flag <= '0';

        ELSIF falling_edge(clk) THEN
            CASE MODE IS
                WHEN "00" =>
                    temp(3 DOWNT0 1) <= temp(2 DOWNT0 0);
                    temp(0) <= Sin;
            end case;
        end if;
    end process;
end USR_4b_arch;
```

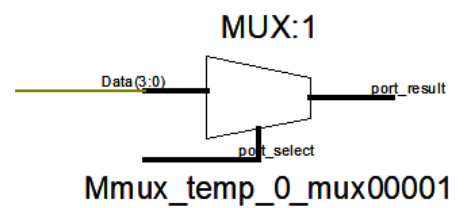
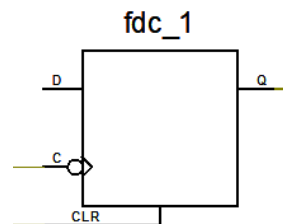
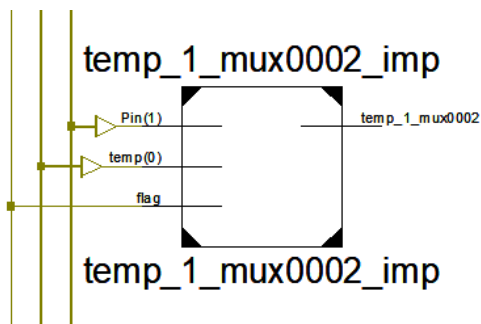
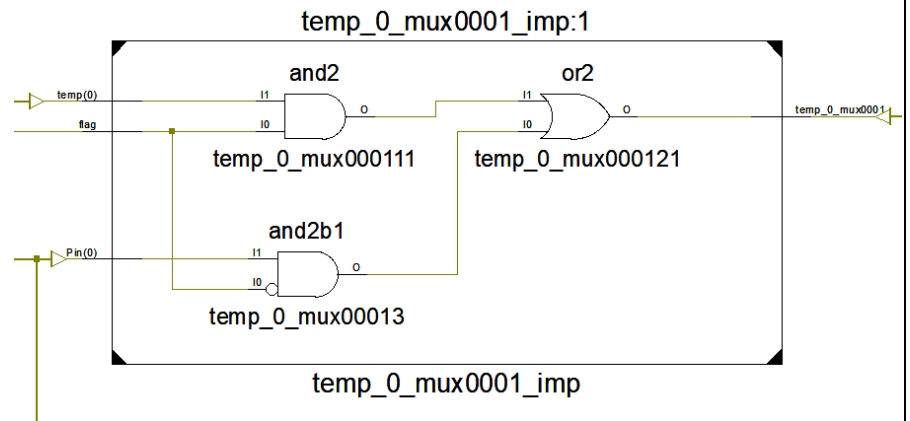
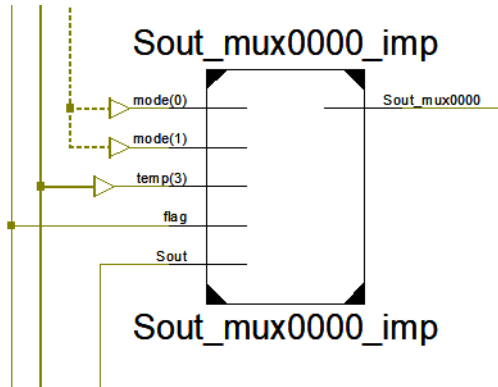
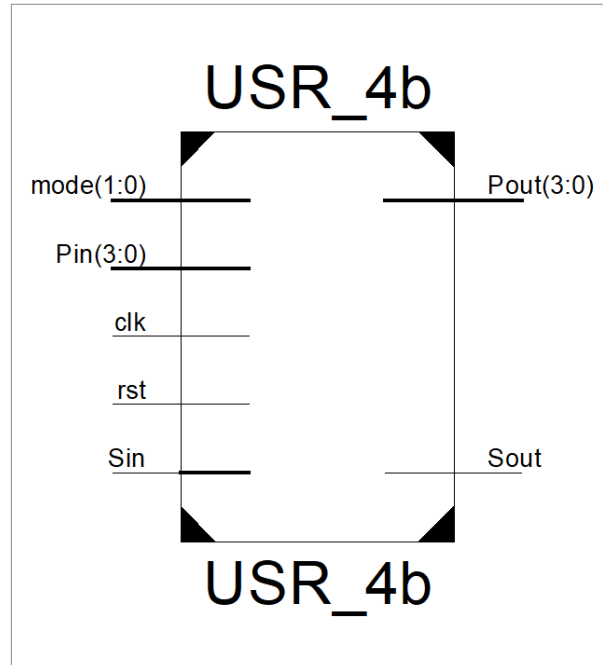
```

        Sout <= temp(3);
        Pout <="0000";
        flag <= '0';
    WHEN "01" =>
        temp(3 DOWNT0 1) <= temp(2 DOWNT0 0);
        temp(0) <= Sin;
        Pout<=temp;
        Sout <= '0';
        flag <= '0';
    WHEN "10" =>
        IF flag='0' THEN
            temp <= Pin;
            Pout <= "0000";
        ELSE
            Sout <= temp(3);
            Pout <= "0000";
            temp(3 DOWNT0 1) <= temp(2 DOWNT0 0);
        END IF;
        flag <= '1';

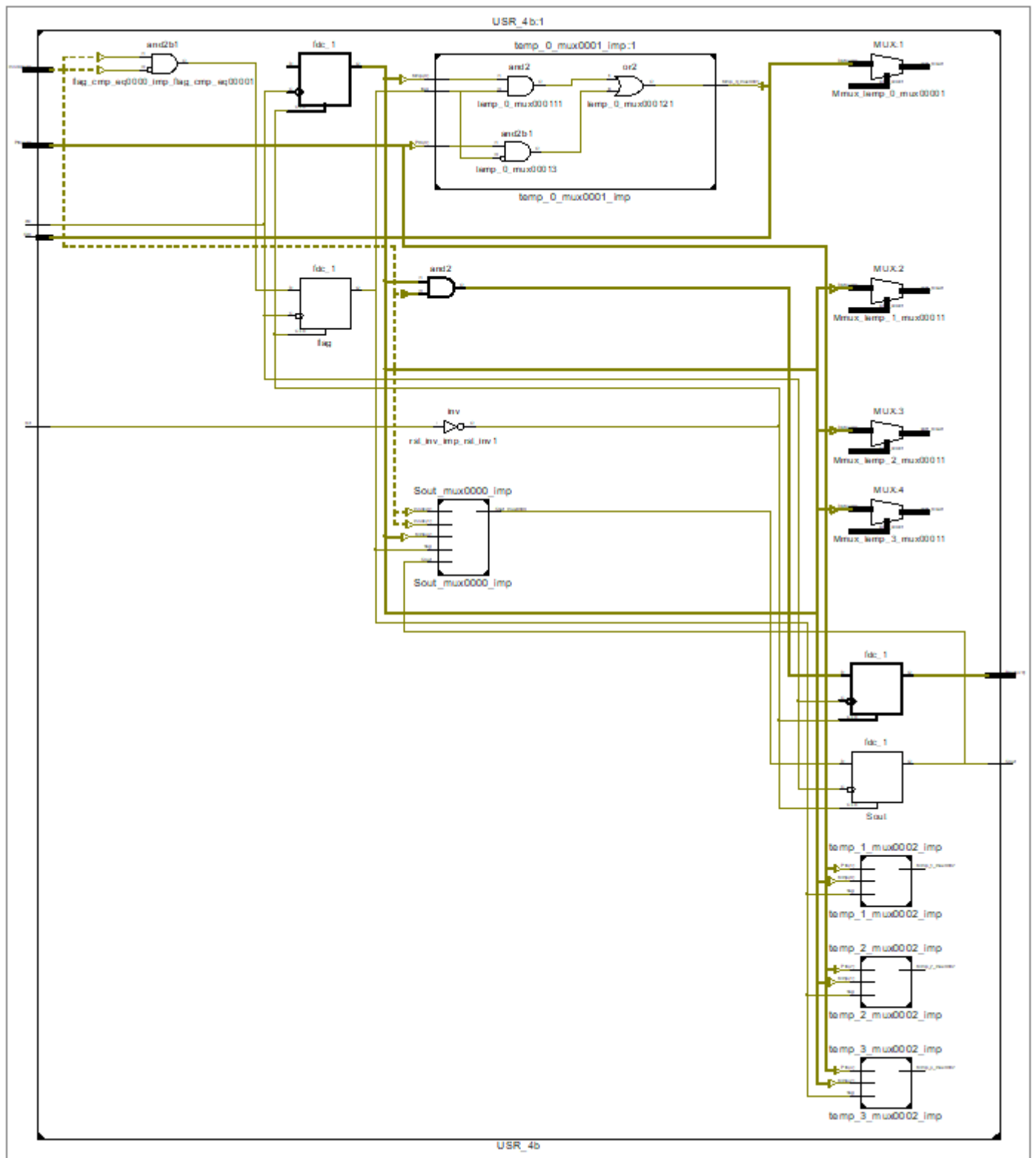
    WHEN OTHERS =>
        temp <= Pin;
        Pout <= temp;
        Sout <= '0';
        flag <= '0';
    END CASE;
END IF;
END PROCESS;
end USR_4b_arch;

```

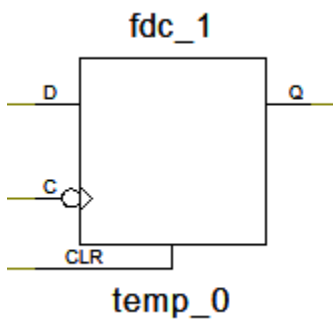
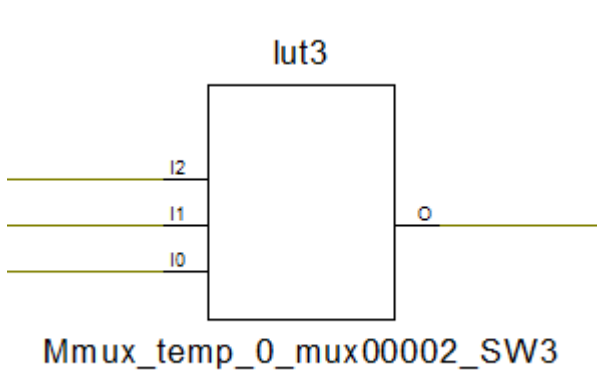
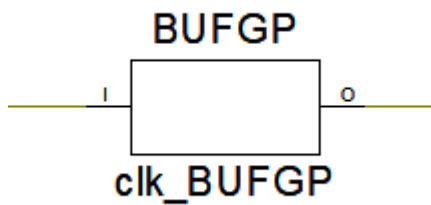
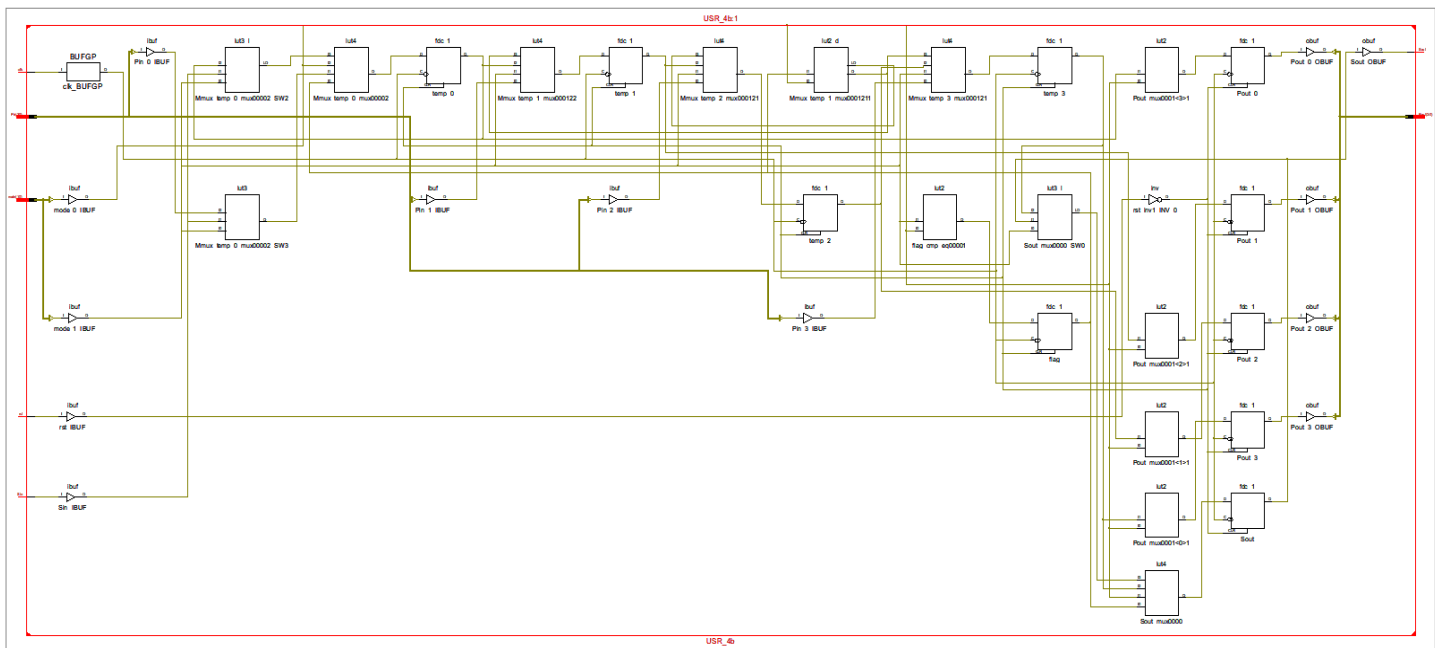
RTL SCHEMATIC



Mmux_temp_0_mux00001



TECHNOLOGY SCHEMATIC



SYNTHESIS REPORT

1) Device Utilisation Summary

=====

* Final Report *

=====

Final Results

RTL Top Level Output File Name : USR_4b.ngr
Top Level Output File Name : USR_4b
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : No

Design Statistics

IOs : 14

Cell Usage :

BELS : 15
INV : 1
LUT2 : 5
LUT2_D : 1
LUT3 : 1
LUT3_L : 2
LUT4 : 5
FlipFlops/Latches : 10
FDC_1 : 10
Clock Buffers : 1
BUFGP : 1
IO Buffers : 13
IBUF : 8
OBUF : 5

=====

Device utilization summary:

Selected Device : 3s250epq208-5

Number of Slices: 8 out of 2448 0%
Number of Slice Flip Flops: 10 out of 4896 0%
Number of 4 input LUTs: 15 out of 4896 0%
Number of IOs: 14
Number of bonded IOBs: 14 out of 158 8%
Number of GCLKs: 1 out of 24 4%

Partition Resource Summary:

No Partitions were found in this design.

2) TIMING REPORT

Timing Summary:

Speed Grade: -5

Minimum period: 2.909ns (Maximum Frequency: 343.725MHz)

Minimum input arrival time before clock: 3.778ns

Maximum output required time after clock: 4.063ns

Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

TESTBENCH PROGRAM

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
USE ieee.numeric_std.ALL;

ENTITY USR_4b_tb IS
END USR_4b_tb;

ARCHITECTURE behavior OF USR_4b_tb IS
    COMPONENT USR_4b
    PORT(
        rst : IN std_logic;
        clk : IN std_logic;
        Sin : IN std_logic;
        Pin : IN std_logic_vector(3 downto 0);
        mode : IN std_logic_vector(1 downto 0);
        Sout : OUT std_logic;
        Pout : OUT std_logic_vector(3 downto 0)
    );
    END COMPONENT;

    signal rst : std_logic := '1';
    signal clk : std_logic := '0';
    signal Sin : std_logic := '0';
    signal Pin : std_logic_vector(3 downto 0) := "1111";
    signal mode : std_logic_vector(1 downto 0) := (others => '0');

    signal Sout : std_logic;
    signal Pout : std_logic_vector(3 downto 0);

    constant clk_period : time := 10 ns;

BEGIN
    uut: USR_4b PORT MAP (
        rst => rst,
        clk => clk,
        Sin => Sin,
        Pin => Pin,
        mode => mode,
        Sout => Sout,
        Pout => Pout
    );

    clk_process : process
    begin
        clk <= '0';
        wait for clk_period/2;
        clk <= '1';
        wait for clk_period/2;
```

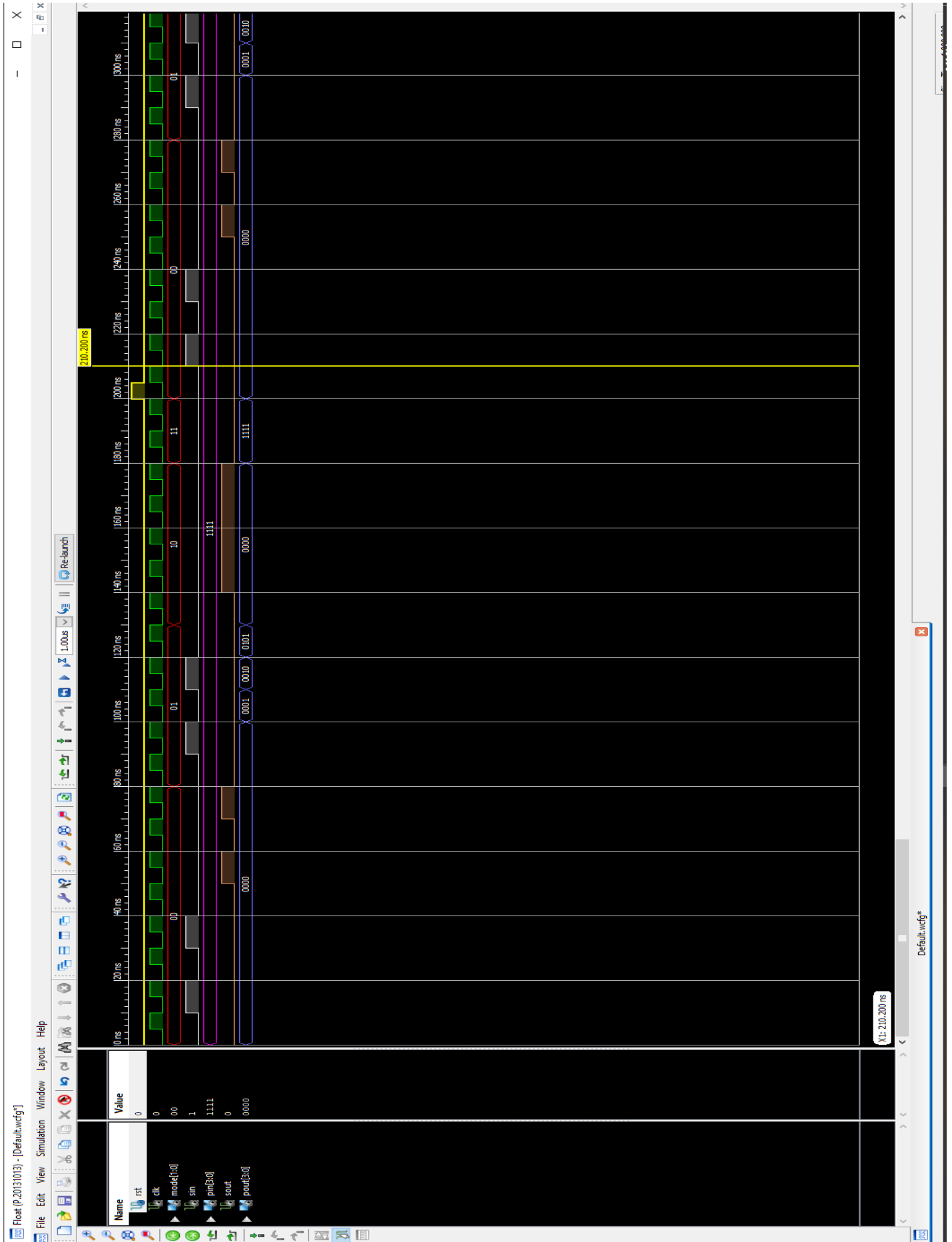
```
end process;

stim_proc_rst: process
begin
    rst<='0';
    wait for 200 ns;
    rst<='1';
    wait for 5 ns;
end process;

stim_proc_mode: process
begin
    mode <= "00";
    wait for 80 ns;
    mode <= "01";
    wait for 50 ns;
    mode <= "10";
    wait for 50 ns;
    mode <= "11";
    wait for 20 ns;
end process;

stim_proc_Sin: process
begin
    wait for 10 ns;
    Sin <= '1';
    wait for 10 ns;
    Sin <= '0';
    wait for 10 ns;
    Sin <= '1';
    wait for 10 ns;
    Sin <= '0';
    wait for 50 ns;
    Sin <= '1';
    wait for 10 ns;
    Sin <= '0';
    wait for 10 ns;
    Sin <= '1';
    wait for 10 ns;
    Sin <= '0';
    wait for 80 ns;
end process;
END;
```

ISIM WAVEFORMS



PIN-LOCKING REPORT

PlanAhead Generated physical constraints

NET "CLK" LOC = P132;

NET "RST" LOC = P204;

NET "mode[1]" LOC = P205;

NET "mode[0]" LOC = P206;

NET "Sin" LOC = P203;

NET "Pin[3]" LOC = P202;

NET "Pin[2]" LOC = P197;

NET "Pin[1]" LOC = P199;

NET "Pin[0]" LOC = P196;

NET "Sout" LOC = P193;

NET "Pout[3]" LOC = P186;

NET "Pout[2]" LOC = P187;

NET "Pout[1]" LOC = P185;

NET "Pout[0]" LOC = P181;

Conclusion:

Thus we have :

- 1) Modeled a 4-bit USR using Behavioral Modeling Style.
- 2) Observed following Schematics: **RTL & Technology Schematics** generated **Post-Synthesis**.
- 3) Interpreted **Device Utilization Summary** in terms of LUTs, SLICES, IOBs, Multiplexers & D FFs used out of the available device resources.
- 4) Interpreted the TIMING Report in terms of Maximum combinational delay as indicative of the Maximum Operating Frequency.
- 5) Written a TESTBENCH to verify the functionality of 4-bit USR & verified the functionality as per the TRUTH-TABLE by observing ISIM Waveforms.
- 6) Used PlanAhead Editor for pin-locking.
- 7) Prototyped the FPGA **XC3S250EPQ208-5** to realize 4-bit USR & verified its operation by giving suitable input combinations.