Kathmandu University

Department of Computer Science and Engineering

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A Report on '**Lab Work 3** [COMP 306]

ALU Circuit

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Qlab1

1. ***Design and simulate an ALU circuit using multiple full adders and other logic gates in Proteus. The circuit should be able to perform various arithmetic and logic operations on two binary numbers of any length.***

Objective:

To Design Arithmetic logic unit (ALU)

Components Required:

- Probe
- Logic-state
- Wire
- Gates (AND, XOR, OR)
- Components (Full adder, Decoder)
- Digital Constant

Truth Table:

The truth table obtained for the ALU circuit are shown in the table below:

S0	S1	S2	Cin	Output
0	0	0	X	And
0	0	1	X	Or
0	1	0	X	Xor
0	1	1	X	Not
1	0	0	0	Add
1	0	1	1	Subract
1	1	0	0	Decrement A
1	1	1	1	Increment A

Fig 4: Truth Table Full-Adder

Circuit Diagram and Screenshots

The following circuit diagrams are exported from proteus simulation:

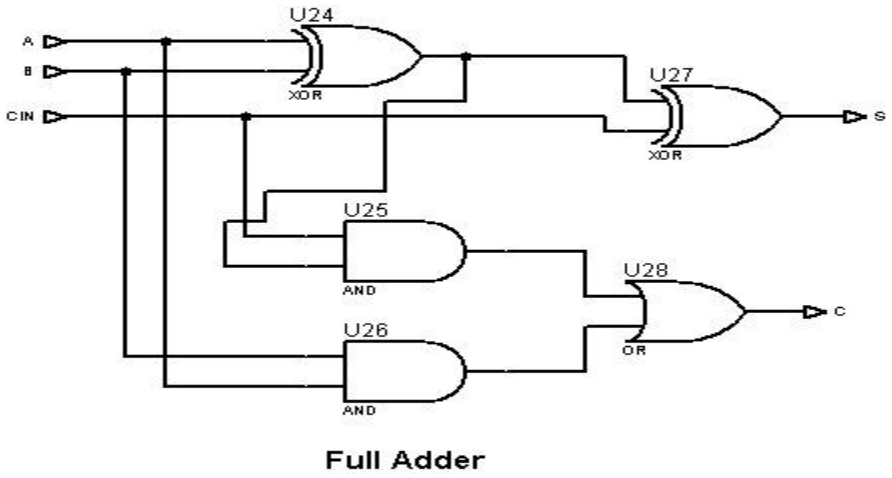

Fig 1: Full Adder circuit

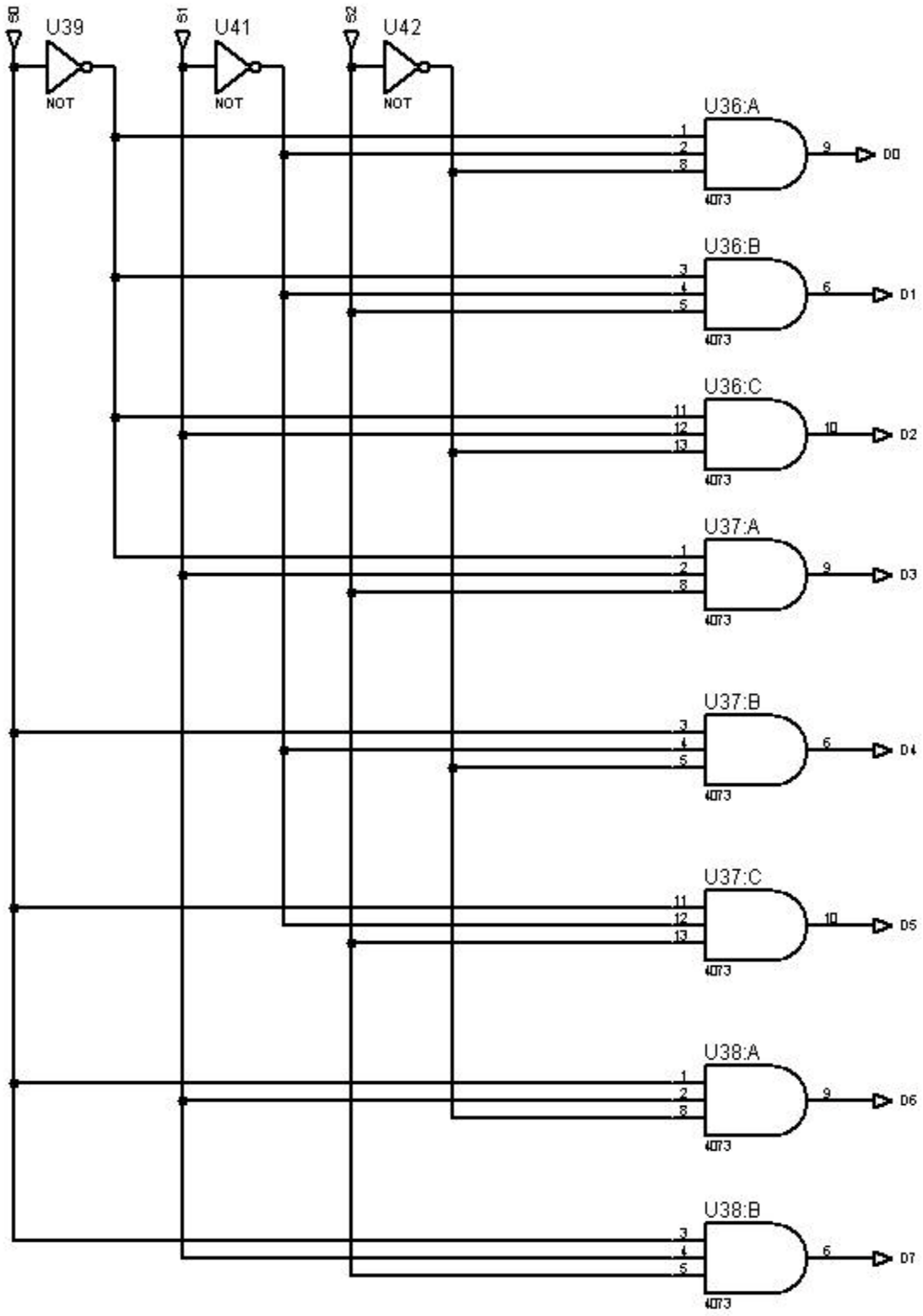

Fig 2: 3 * 8 Decoder

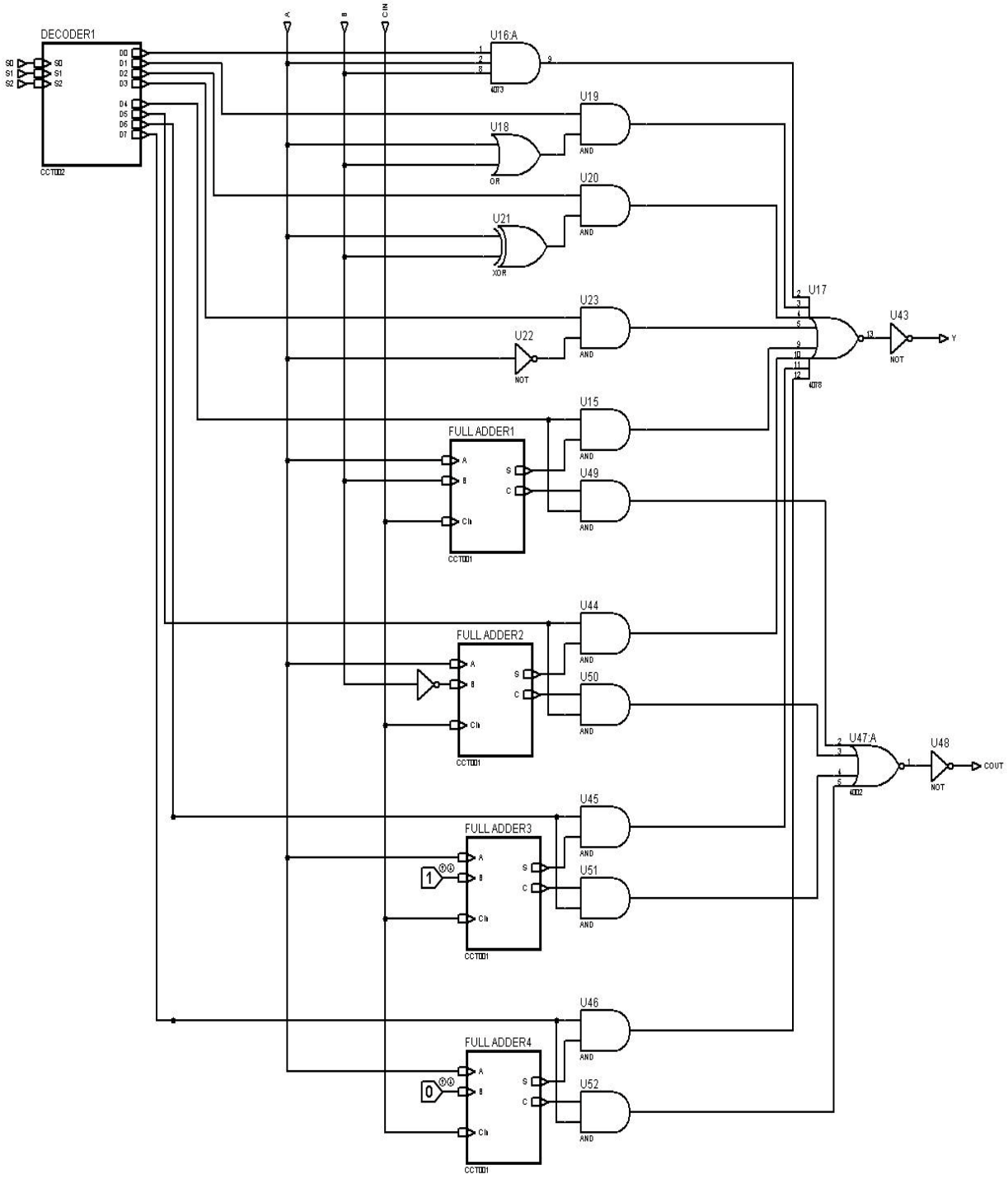

Fig 3: ALU Circuit (single bit)

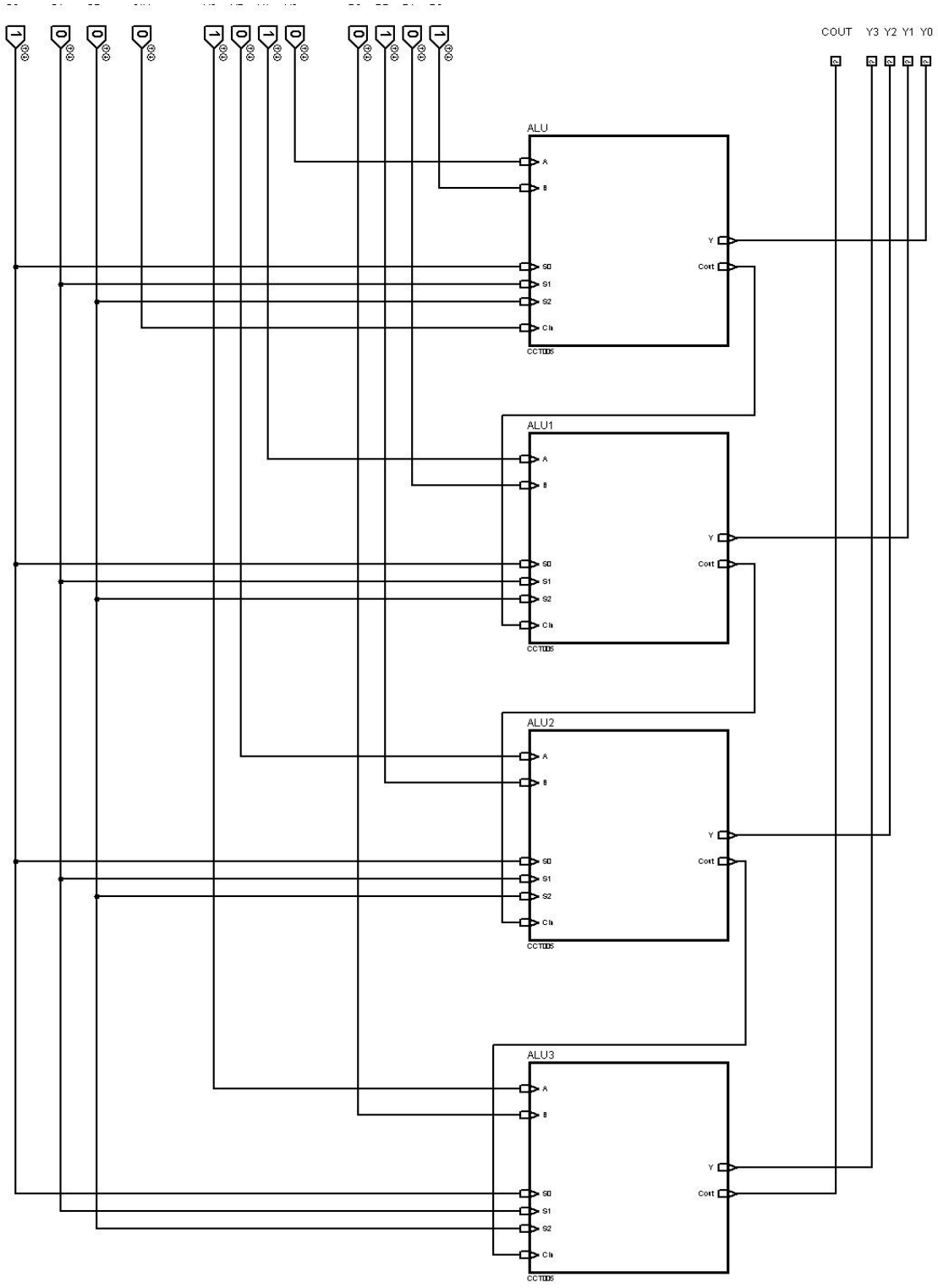

Fig 4: 4-Bit ALU

Conclusion:

After designing and simulating the ALU circuit using multiple full adders and other logic gates in Proteus, it was found that the circuit was able to perform various arithmetic and logic operations on two binary numbers of 4-bit length. The ALU circuit was able to accurately perform operations such as addition, subtraction, AND, OR, Xor, Not, Decrement A and Increment A. The circuit was also able to handle binary numbers of 4-bit length. The truth tables were determined by checking multiple combinations of inputs and their effects on the probe. Overall, the ALU circuit design was successful in meeting the requirements and demonstrating its functionality through simulation.