LAB 2

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CE III/II	
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1. Design and simulate an ALU circuit using multiple full adders and other logic gates in Proteus. The circuit should be able to perform various arithmetic and logic operations on two binary numbers of any length.

2. Display the result on a seven-segment display or other output component

Truth Table for ALU

S0	S1	S2	Cin	Output
0	0	0	X	And
0	0	1	X	Or
0	1	0	X	Xor
0	1	1	X	Complement A
1	0	0	0	Add
1	0	1	1	Subract
1	1	0	0	Decrement A
1	1	0	1	Transfer A
1	1	1	1	Increment A

Fig 1: ALU truth table

Circuit Diagram

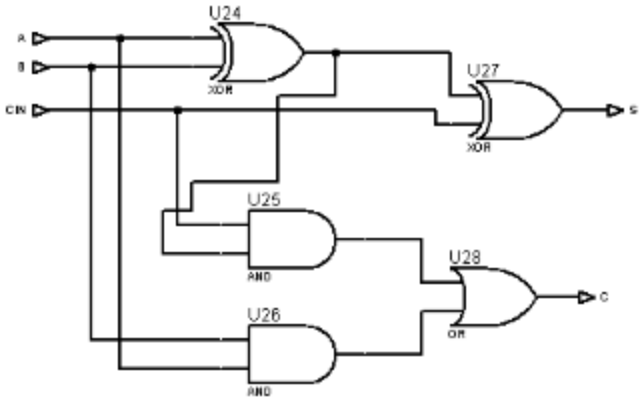

Fig 2: Full Adder

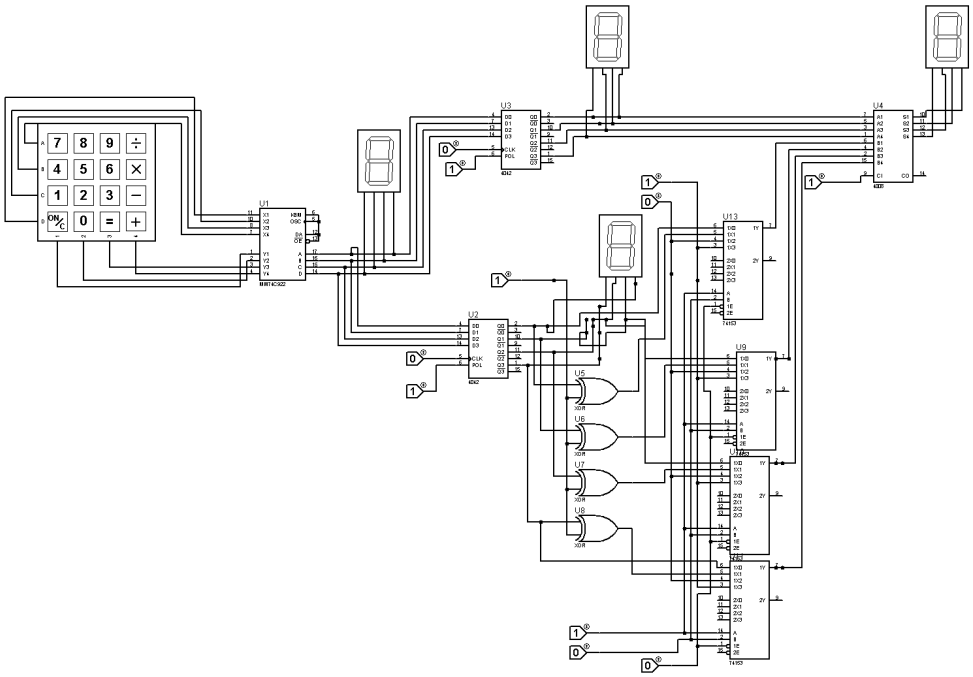

fig: ALU circuit Design

Output

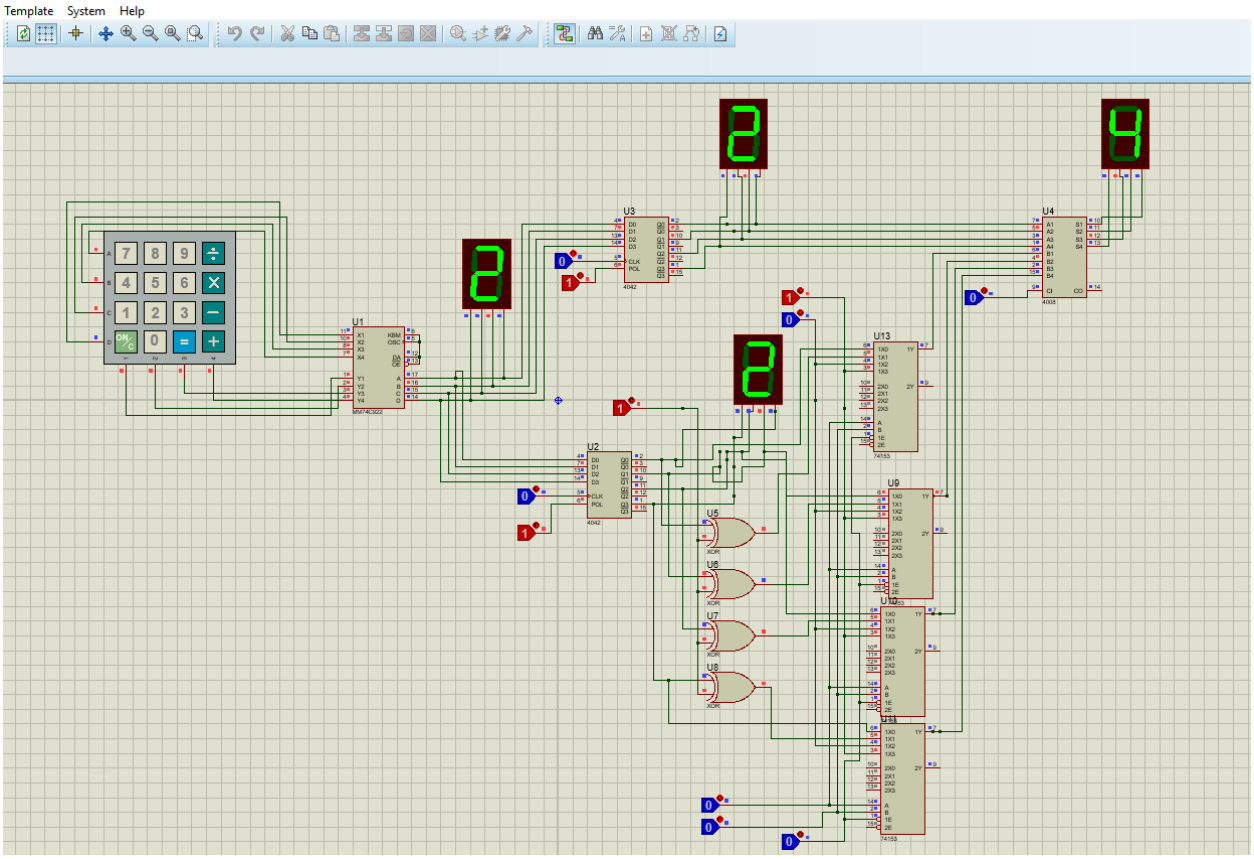

Fig 4: Add operation

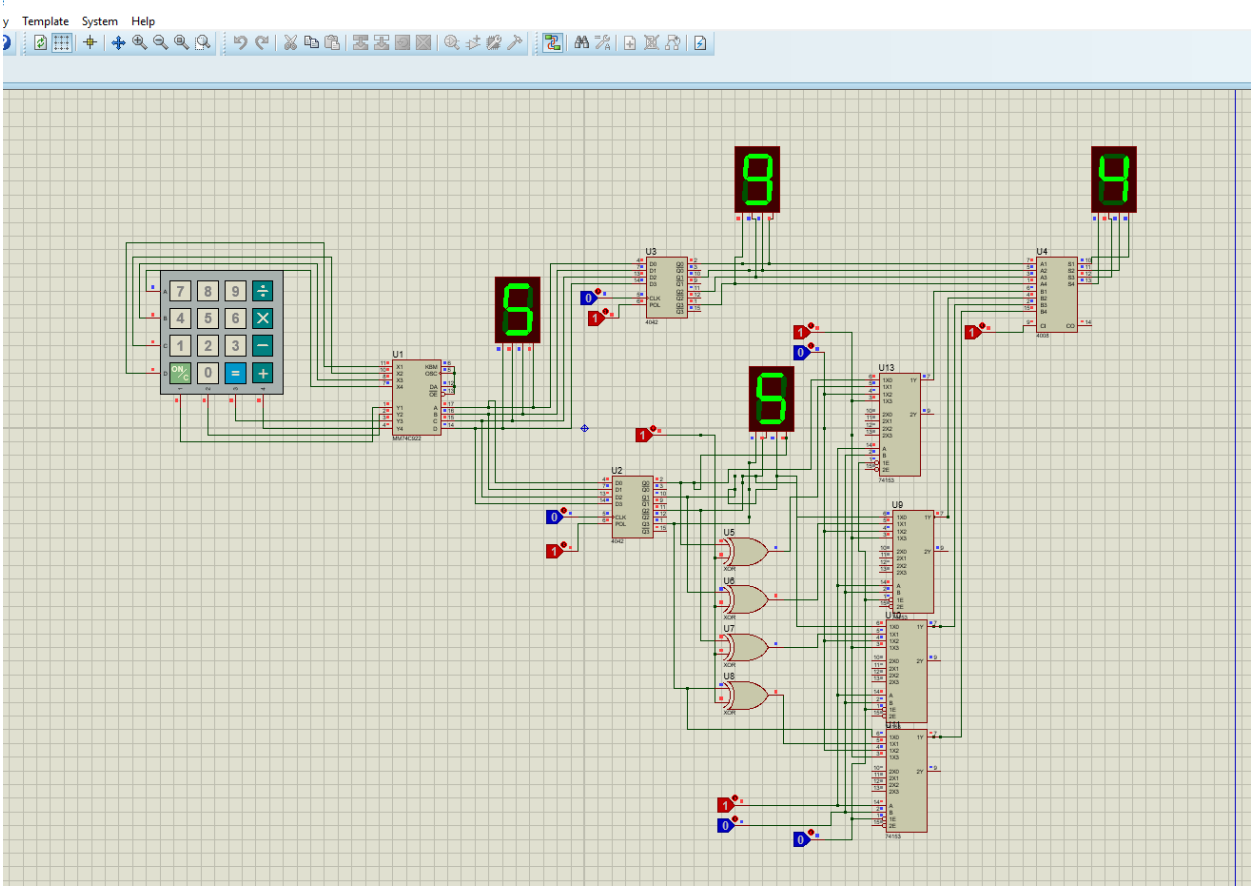

Fig 5: Subtract Operation

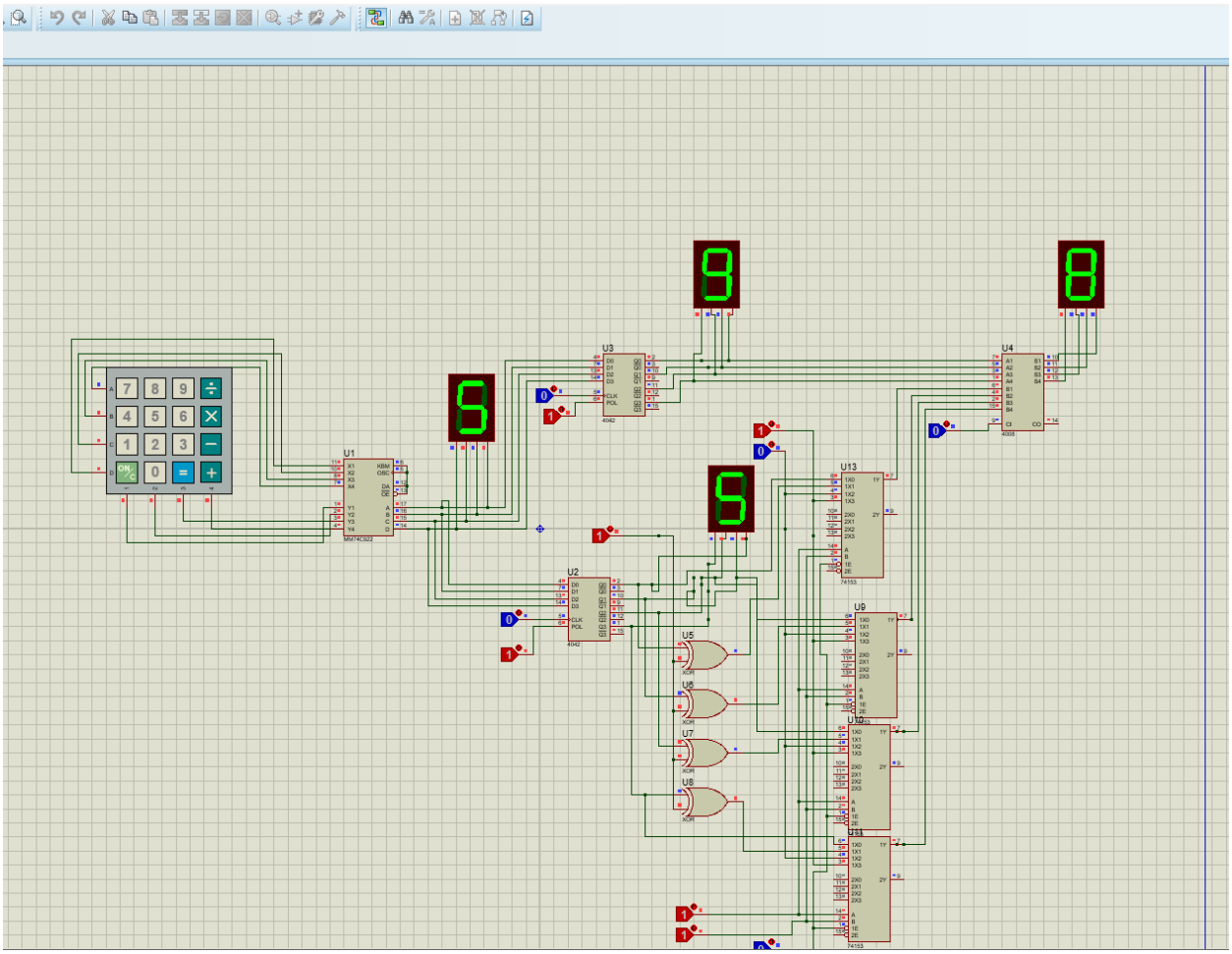

Fig 6: Decrement Operation

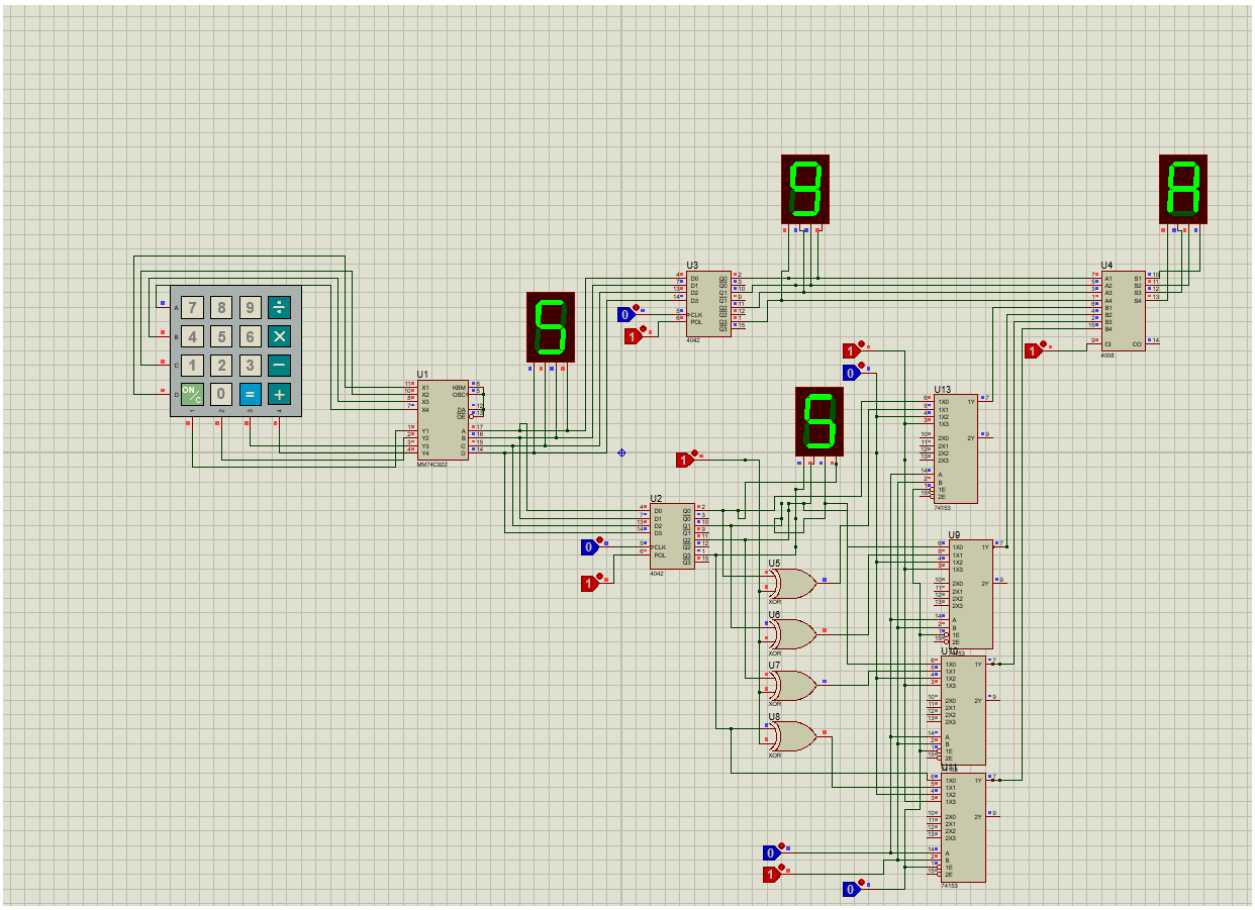

Fig 7: Increment Option