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A Report on '**Lab Work 1** [COMP 306]

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Submitted to:

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Qlab1

1. Design AND, OR, NOT, XOR, NAND & NOR using proteus simulation.

Objective:

To Design AND, OR, NOT, XOR, NAND, NOR Gates

Components Required:

- Probe
- Wire
- Gates (AND, OR, NOT, XOR, NAND and NOR)
- Digital Constant

Circuit Diagram

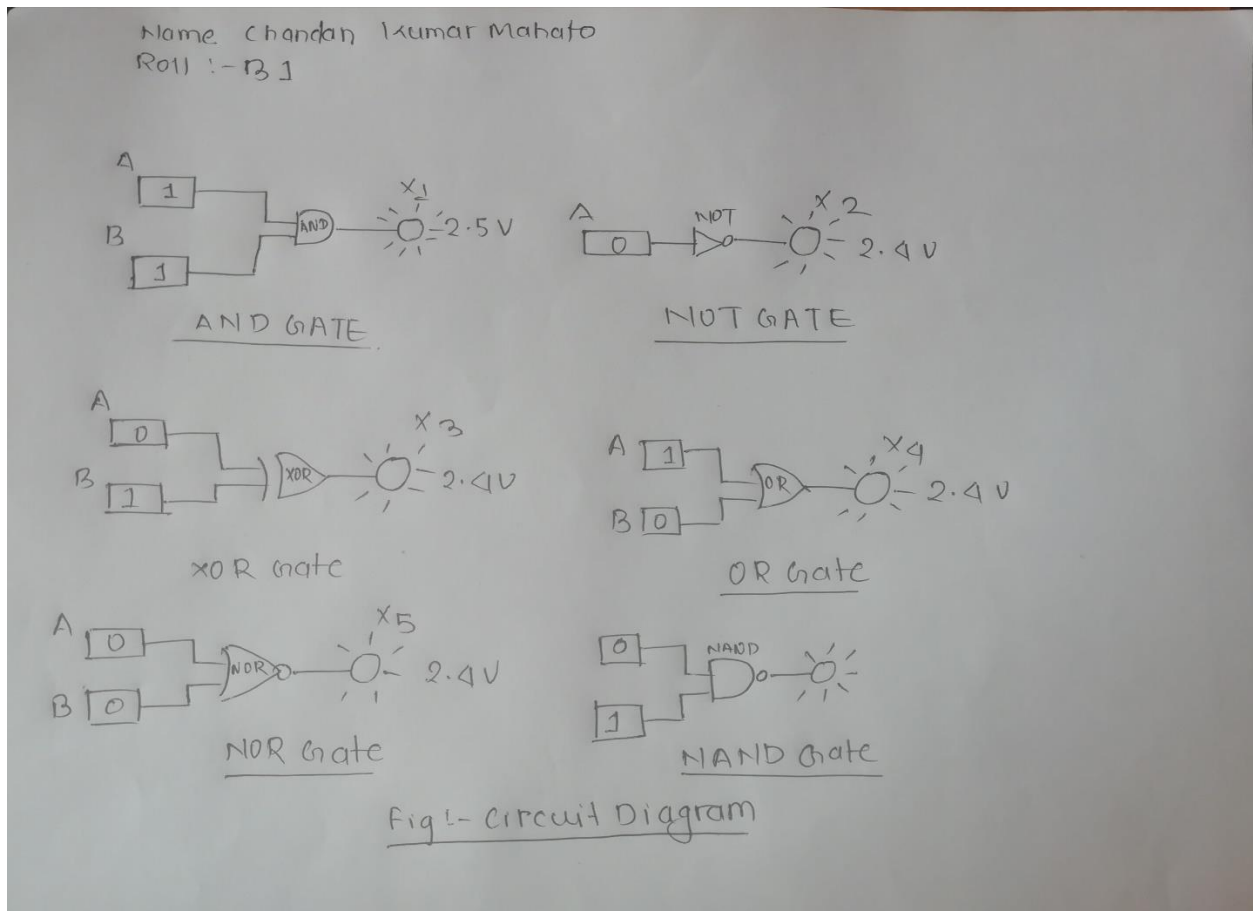


Fig: Circuit Diagram

Truth Table:

The truth table obtained for the different gates after varying their input parameters during simulation are shown in the table below:

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x ₁			x ₂			x ₃	
A	B	OUTPUT	A	B	OUTPUT	A	output
0	0	0	0	0	0	0	1
0	1	0	0	1	1	1	0
1	0	0	1	0	1		
1	1	1	1	1	1		

AND Gate OR Gate OR Gate

x ₄			x ₅			x ₆		
A	B	output	A	B	output	A	B	output
0	0	1	0	0	1	0	0	0
0	1	1	0	1	0	0	1	1
1	0	1	1	0	0	1	0	1
1	1	0	1	1	0	1	1	0

NAND Gate NOR Gate XOR Gate

Fig: Truth Table

Conclusion:

All Six gates were successfully simulated using proteus simulation and the truth table were determined by checking multiple combinations of inputs and their effect on the probe.

Screen Shots

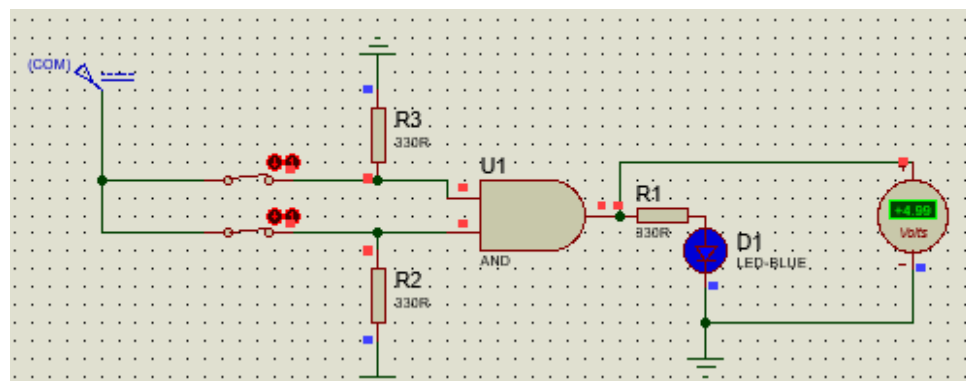
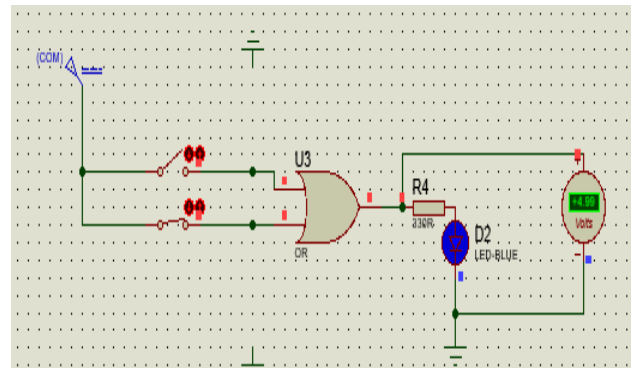
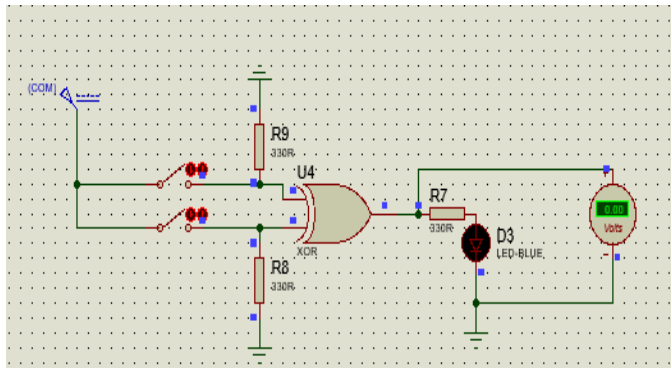
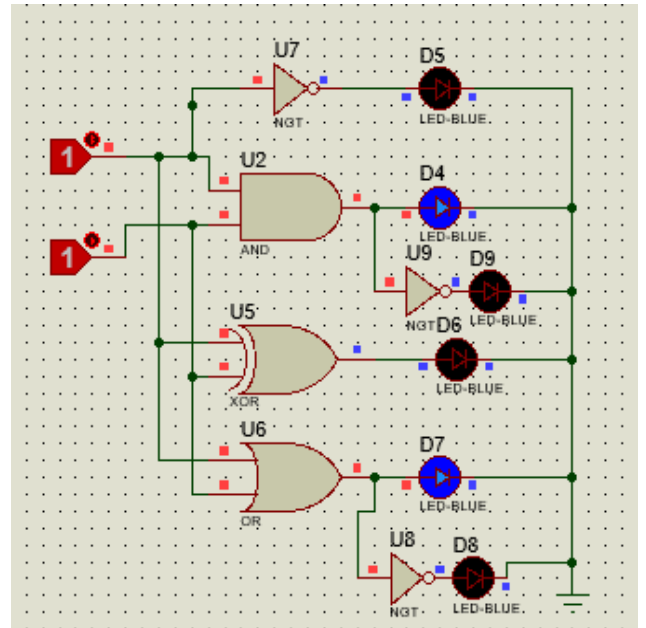
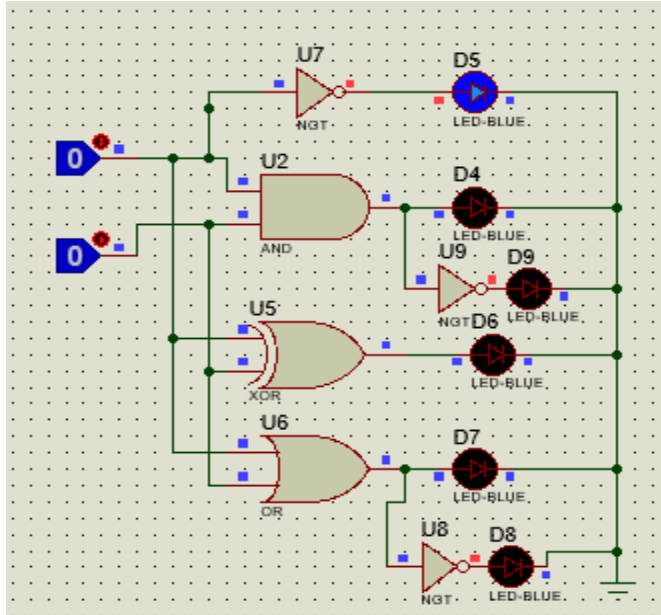


Fig: Circuit showing AND, OR, NOT, XOR, NAND, NOR GATES