Kathmandu University

Department of Computer Science and Engineering

Dhulikhel, Kavre

A Report on '**Lab Work 2** [COMP 306]

Half Adder and Full Adder

Submitted by:

Chandan Kumar Mahato (31)

III-year, II semester

Submitted to:

Prof. Dr. Sudan Jha

Department of Computer Science and Engineering

Submission Date: April 21, 2023

Qlab1

1. ***Design Half Adder and Full Adder using proteus simulation.***

Objective:

To Design Half Adder and Full Adder

Components Required:

- Probe
- Wire
- Gates (AND, XOR, OR)
- Digital Constant

Circuit Diagram

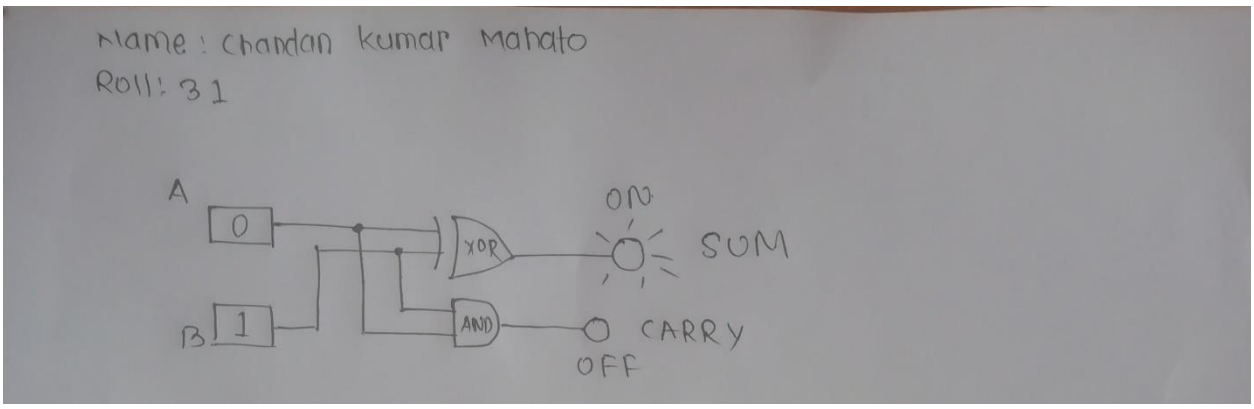


Fig 1: Half-Adder Circuit

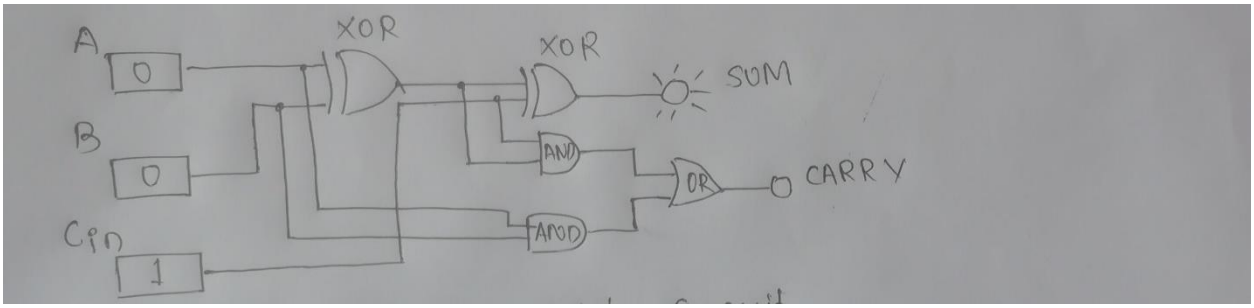
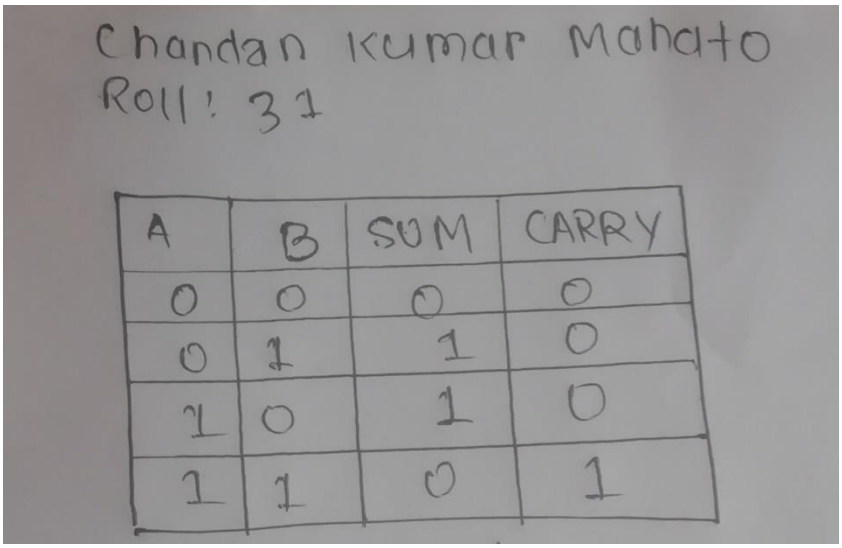


Fig 2: Full-Adder Circuit

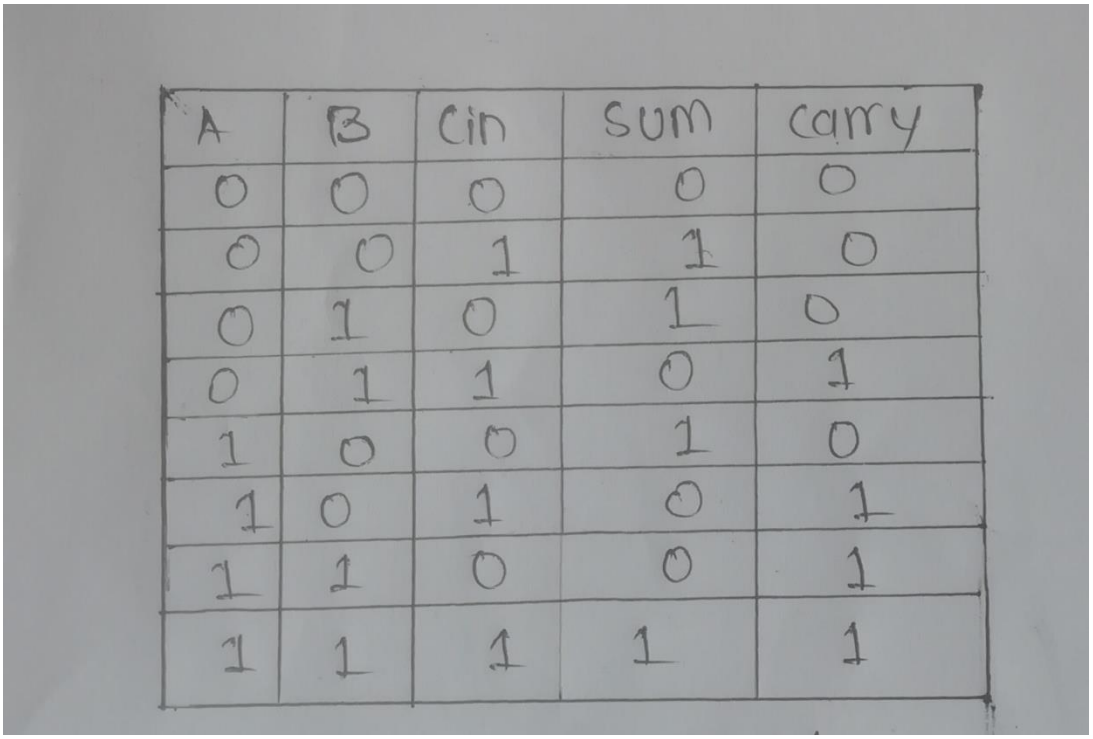
Truth Table:

The truth table obtained for the Half Adder and Full Adder after varying their input parameters during simulation are shown in the table below:


Chandan kumar Mahato
Roll: 31

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Fig 3: Truth Table Half-Adder



A	B	Cin	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig 4: Truth Table Full-Adder

Conclusion:

Both Half Adder and Full Adder were successfully simulated using Proteus Simulation and the truth tables were determined by checking multiple combinations of inputs and their effects on the probe.

Screenshots:

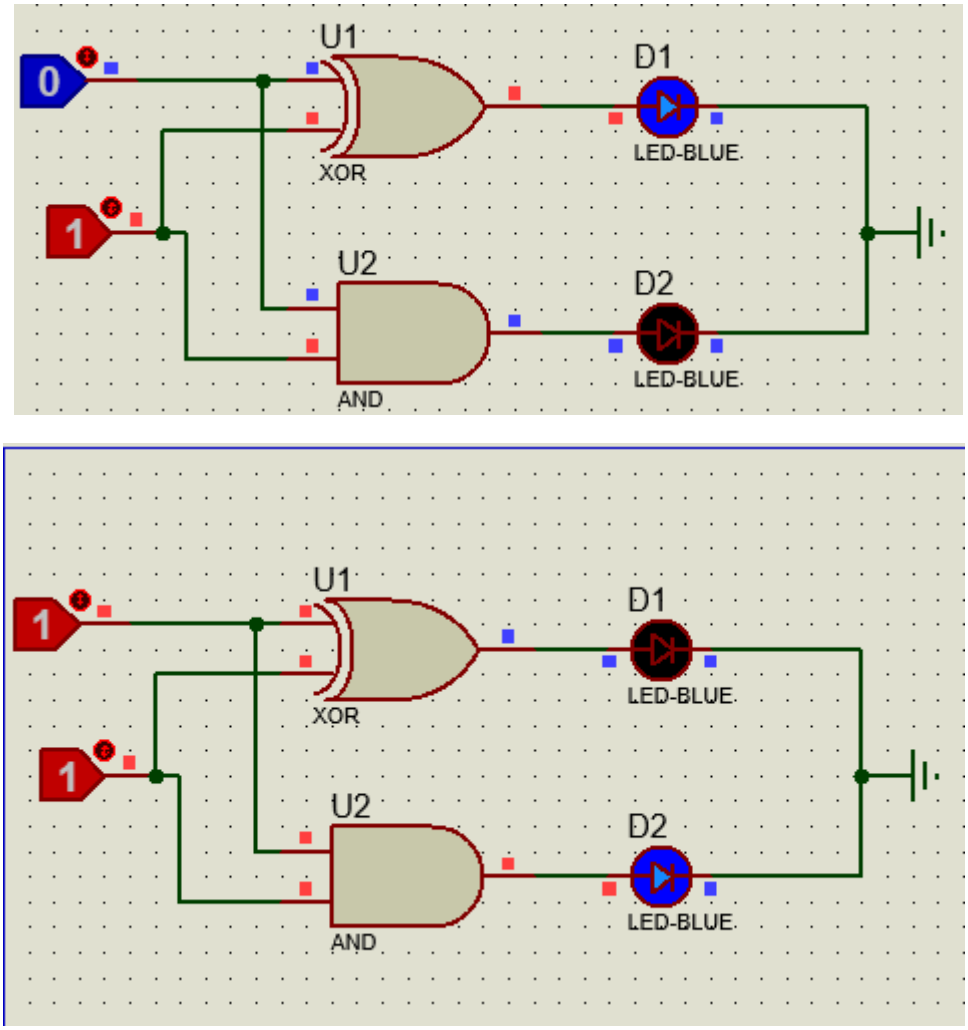


Fig 5: half-adder Circuit

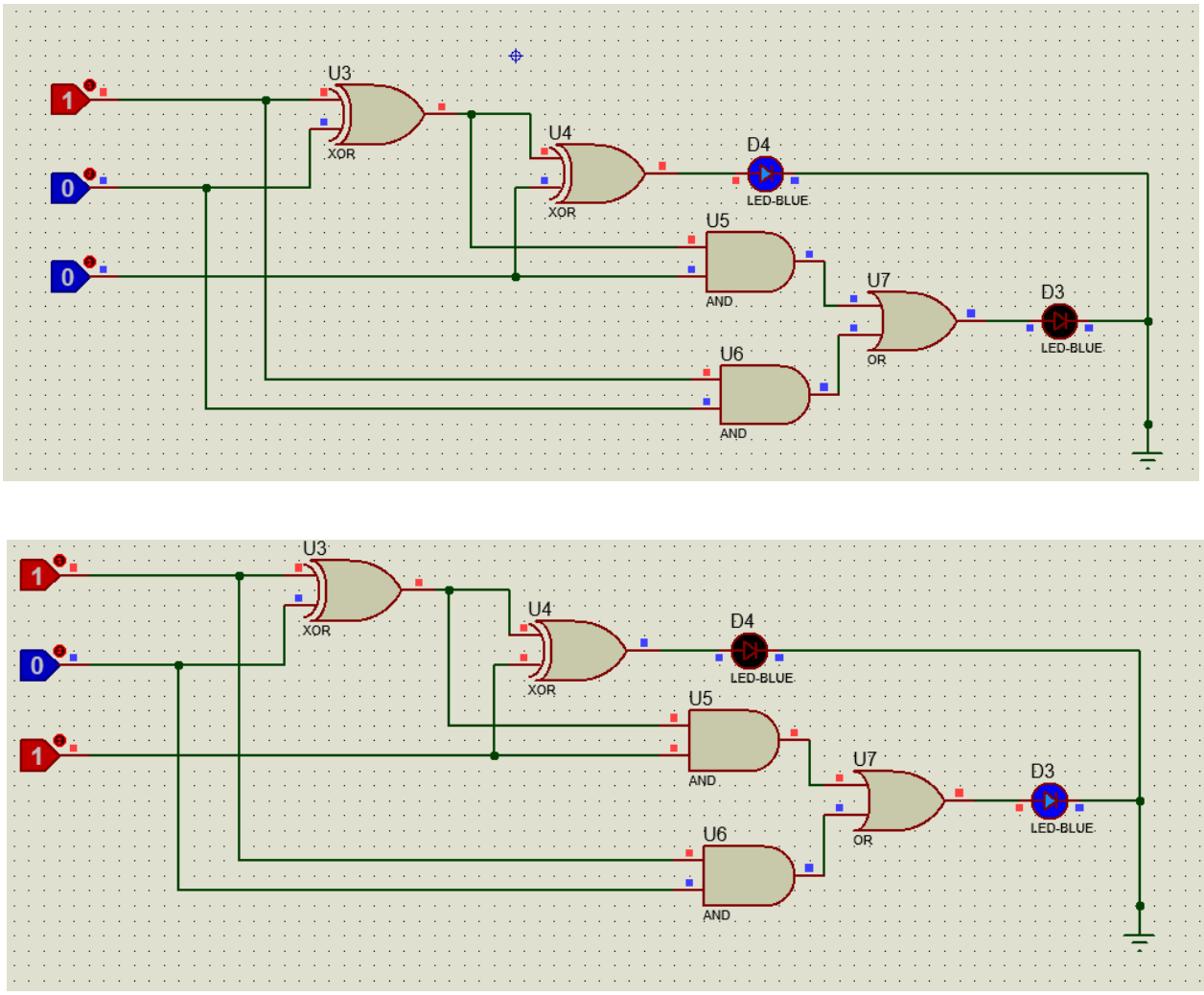


Fig 6: Full-adder Circuit