**Kathmandu University**

**Department of Computer Science and Engineering**

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A Report on ‘**Lab Work 2** [COMP 306]

**Half Adder and Full Adder**

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***Qlab1***

1. ***Design Half Adder and Full Adder using proteus simulation.***

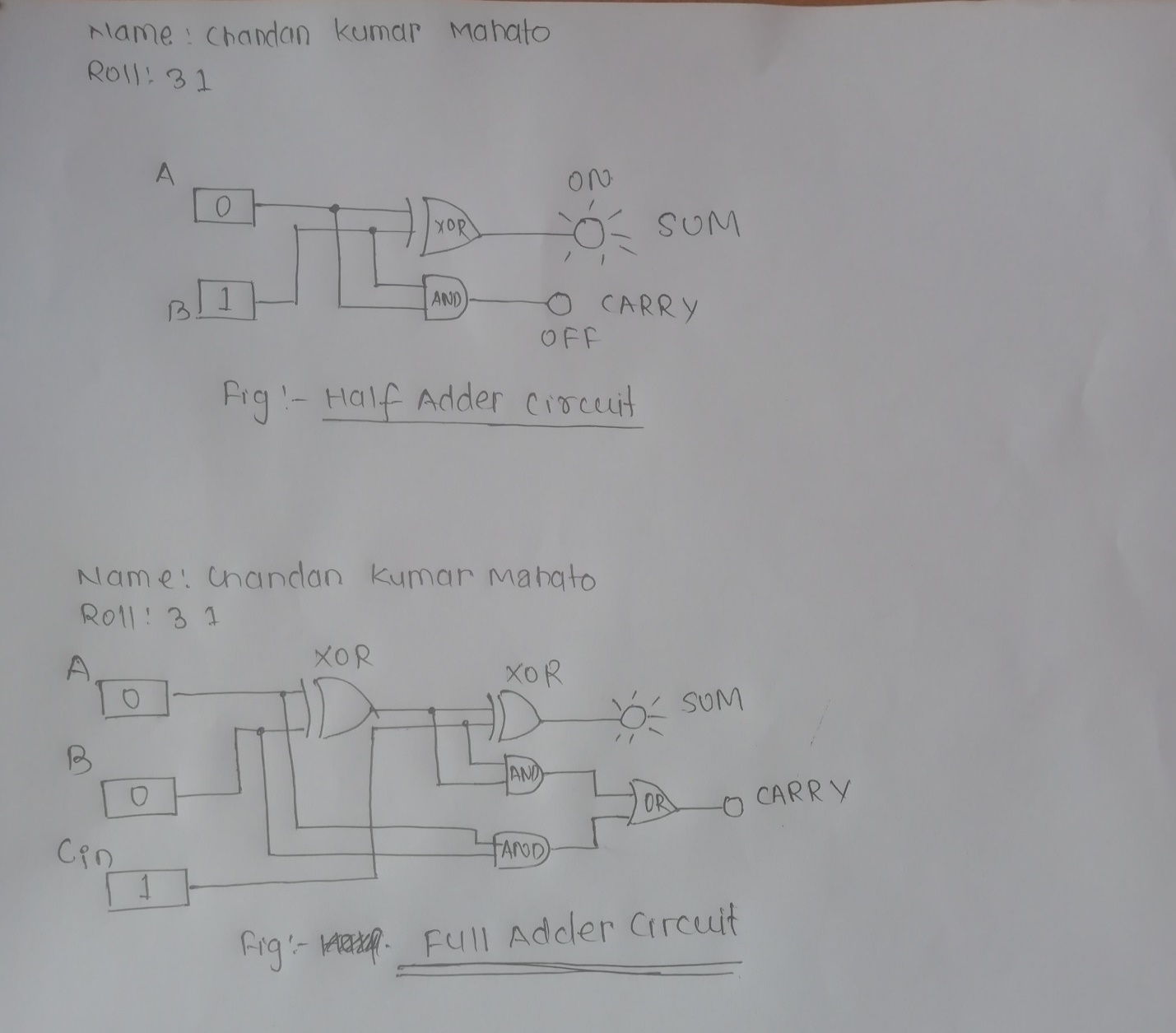
**Objective:**

To Design Half Adder and Full Adder

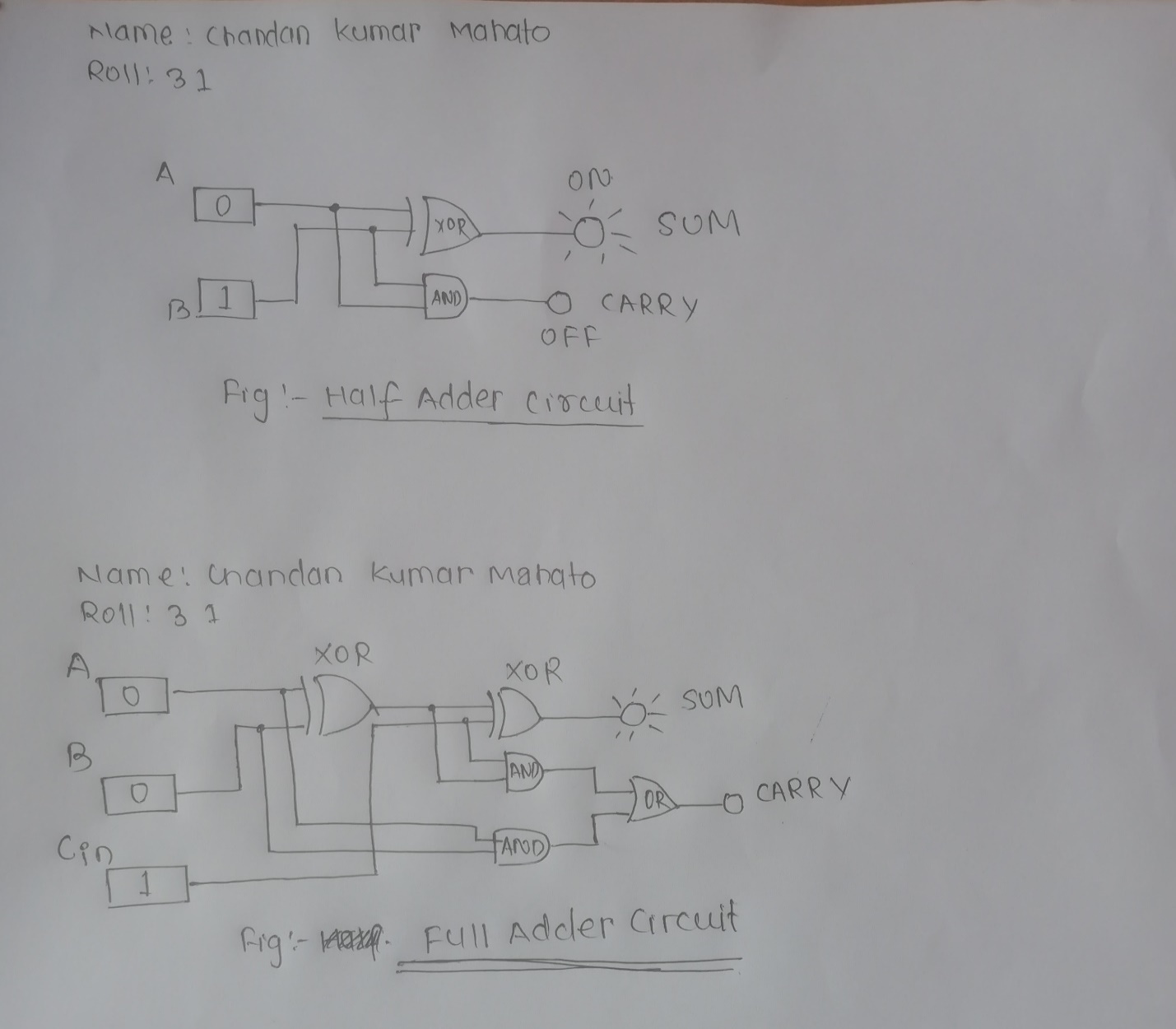
**Components Required**:

* Probe
* Wire
* Gates (AND, XOR, OR)
* Digital Constant

**Circuit Diagram**

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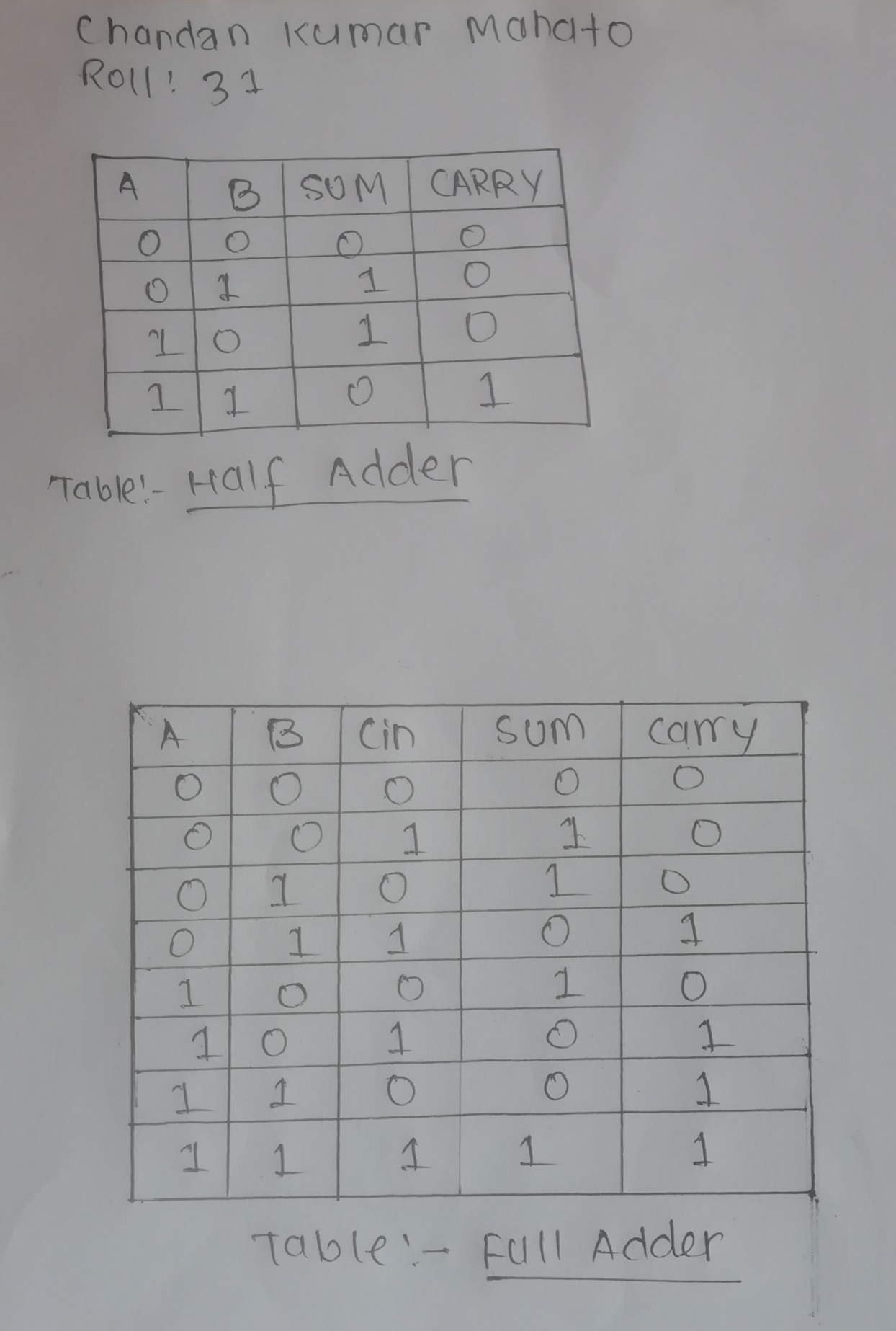
*Fig 1: Half-Adder Circuit*

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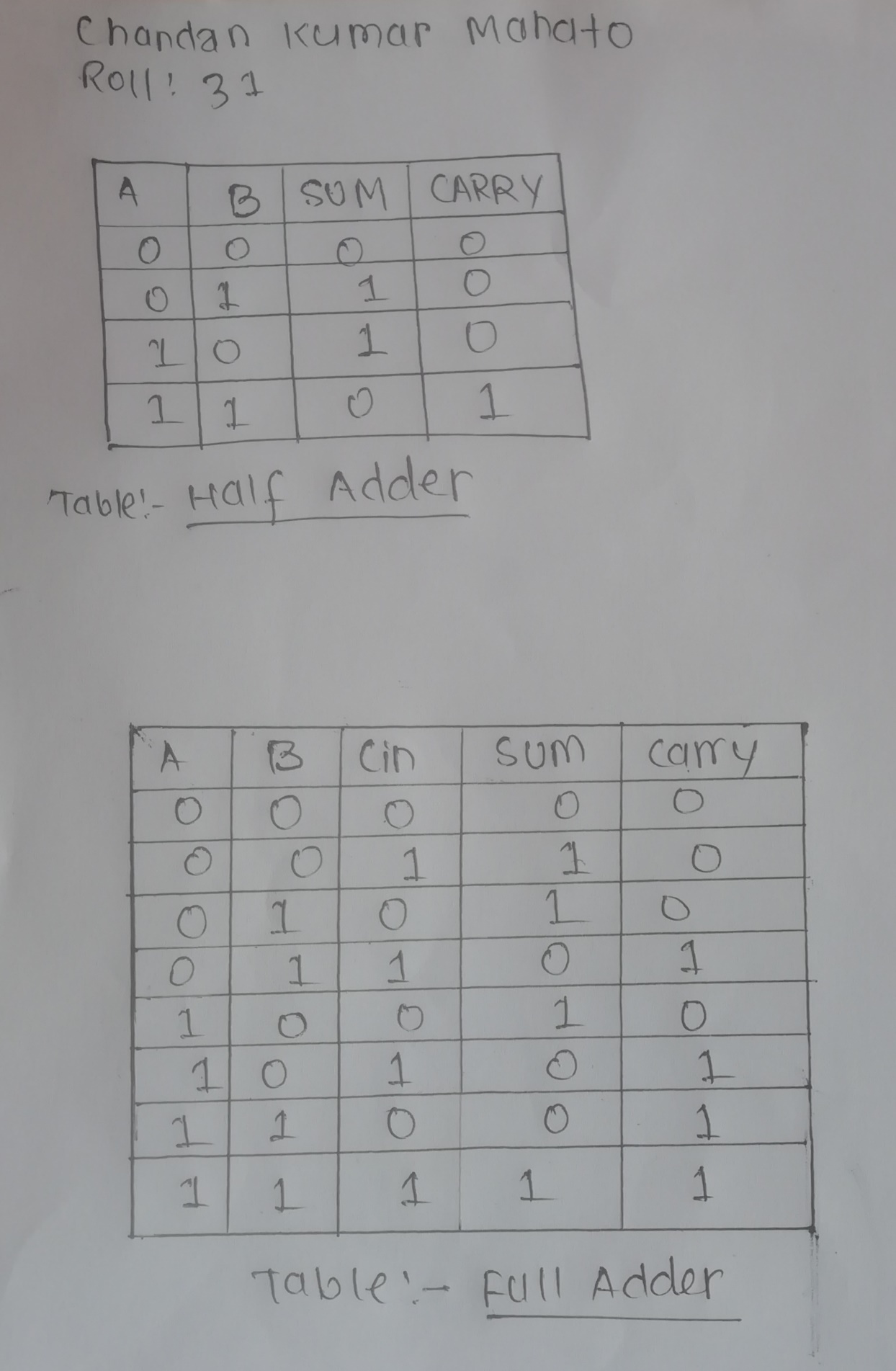
*Fig 2: Full-Adder Circuit*

**Truth Table:**

The truth table obtained for the Half Adder and Full Adder after varying their input parameters during simulation are shown in the table below:



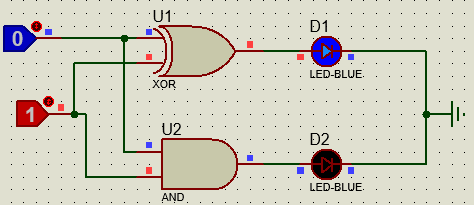
*Fig 3: Truth Table Half-Adder*

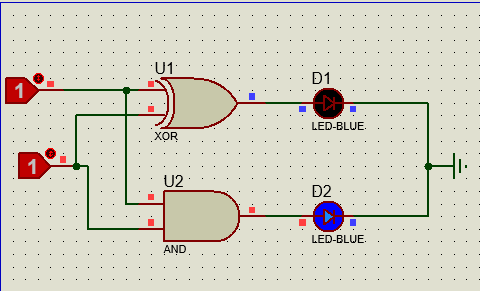
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*Fig 4: Truth Table Full-Adder*

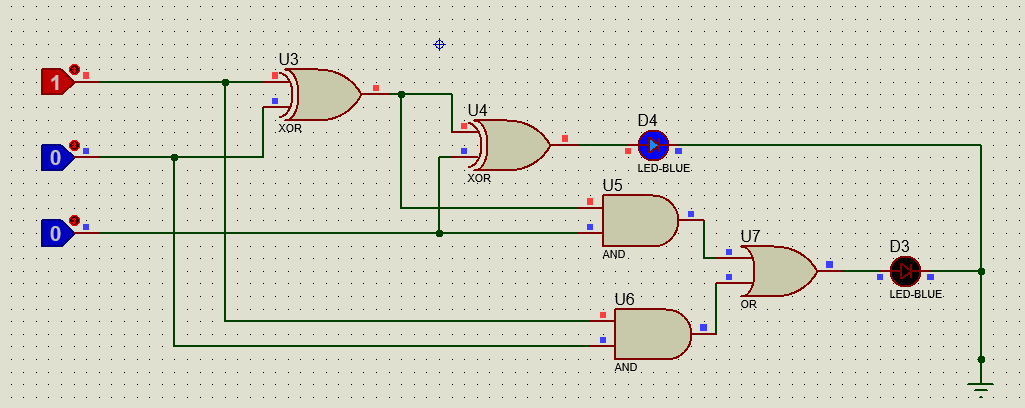
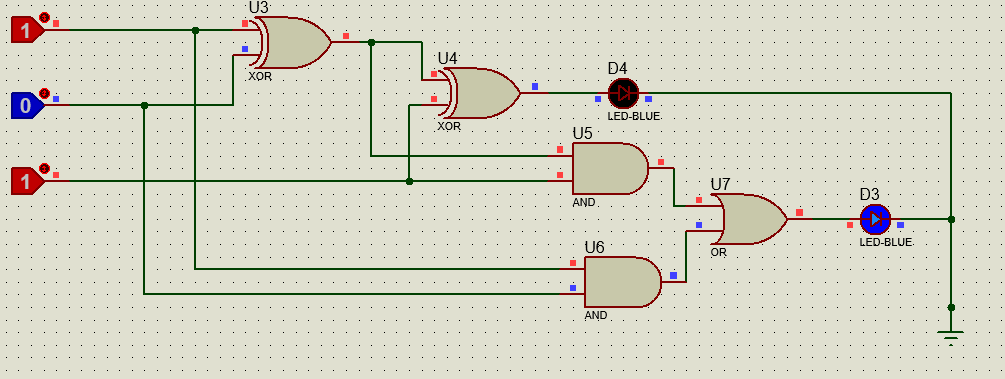
**Conclusion:**

Both Half Adder and Full Adder were successfully simulated using Proteus Simulation and the truth tables were determined by checking multiple combinations of inputs and their effects on the probe.

****Screenshots:**

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*Fig 5:**half-adder Circuit*

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*Fig 6: Full-adder Circuit*