Dayananda Sagar University
School of Engineering

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture
Course Code: 22CS2405
Assignment 2

Last date for Submission: 7th June 2024

Note:

1. All questions and its solutions must be written in A4 sheet and it must be handwritten.
2. Assignment 2 is evaluated for 10 Marks.
3. Upload the softcopy of the assignment in the ERP.
4. Before you start answering the assignment questions, write your details: Name, USN, Section, Semester, Subject and assignment no with date.

Q No	Question	CO
	Module 4	
1	**Write** the advantages of implementing a 5-stage pipelined processor in a simple RISC architecture. Provide the details of pipelining stages for "**Register-to-Register ALU instruction**" to illustrate your points.	CO 4
2	**Discuss** the significance of using six signals for managing **read and write operations** within the register file of a processor architecture.	CO 4
3	**Evaluate** the efficacy of a single-cycle datapath design for a MIPS processor, including **load and store** instructions.	CO 4
4	Analyze the following code for both data and structural hazards. Assume a processor with a single ALU and a single memory unit, with no forwarding. I1: LOD R1, 0(R2) I2: ADD R3, R1, R4 I3: STD R3, 4(R2) I4: MUL R5, R6, R7	CO 4

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5	Given the following sequence of instructions, use scoreboarding to schedule the instructions. Assume the following latencies: ADD takes 2 cycles, MUL takes 10 cycles, and SUB takes 2 cycles. The processor has a single functional unit for each type of operation and registers are not written until the end of execution. Trace the scoreboard till all the below instructions complete execution. I1: ADD R1, R2, R3 I2: MUL R4, R1, R5 I3: SUB R6, R4, R7 I4: ADD R8, R6, R9	CO 4
	Module 5	
6	Compare and Contrast Cache and Virtual Memory	CO 5
7	**Define** cache hit, cache miss, and miss rate in the context of cache memory	CO 5
8	Compare the Impact of Changing Cache Hit Ratio Given: Cache access time: 5 ns Main memory access time: 45 ns Calculate the average memory access time for hit ratios of 0.87, 0.95, and 0.98.	CO 5

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9	Suppose we have a computer system with a cache memory that has a hit ratio of 0.9. If the cache access time is 2 nanoseconds (ns), and the main memory access time is 20 ns, calculate the average access time for memory.	CO 5
10	Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache. What are the various miss rates? Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle, and there are 1.5 memory references per instruction. What is the average memory access time and average stall cycles per instruction? Ignore the impact of writes.	CO 5
11	Explore the fundamental cache optimization techniques used to improve memory hierarchy performance in computer systems.	CO 5
12	Define virtual memory and explain its role in computer systems. What is the need of Translation Look-aside Buffer. Explain with the neat diagram.	CO 5