

→ Introduction to Computer organization :-

- (i) Computer organization refers to the operational unit and their interconnection.
- (ii) It implements the provided computer architecture.
- (iii) Organization is how features are implemented.
 - (a) Control signals, Interfaces, management organization
 - (b) for ex :- Is there a hardware multiple unit or it done by repeated addition.

→ Computer Architecture :-

- (i) Computer architecture is a blue print for design and implementation of a computer system.
- (ii) It provides the functional details and behaviour of a computer system and comes before computer organization.

Notes :- i) Computer organization deals with how to do.

ii) Computer Architecture deals with what to do.

Comp. Organisation.

- i) It is concerned with the structure and behaviour of the computer system as seen by user.
- ii) Deals with the components of the connection in a system.
- iii) It tells us how exactly all the units in the system are arranged and interconnected.
- iv) Organization expresses the realization of architecture.
- v) An organization is done on the basis of architecture.
- vi) It deals with low level design issues.
- vii) Organization involves physical components (circuit, design, address signals, peripherals).

Comp. Architecture

- i) It is concerned with the way hardware components are connected together to form a Computer System.
- ii) Acts as the interface b/w Hardware and Software.
- iii) It helps us to understand the functionality of the system.
- iv) A programmer can view architecture in terms of instruction addressing mode of and registers.
- v) While designing a Computer system architecture is considered first.
- vi) It deals with high level design issues.
- vii) Architecture involves logic (instruction, set), addressing mode, data types, cache optimization.

→ Functional unit of digital system :-

- A General computer system is the best known example of a digital system.
- Other examples include telephone switching exchange, digital counter, electronic calculator and digital display etc.

Q Computer consist of five main component

Input

Output

Memory

CU (Control Unit)

ALU

Block diagram.

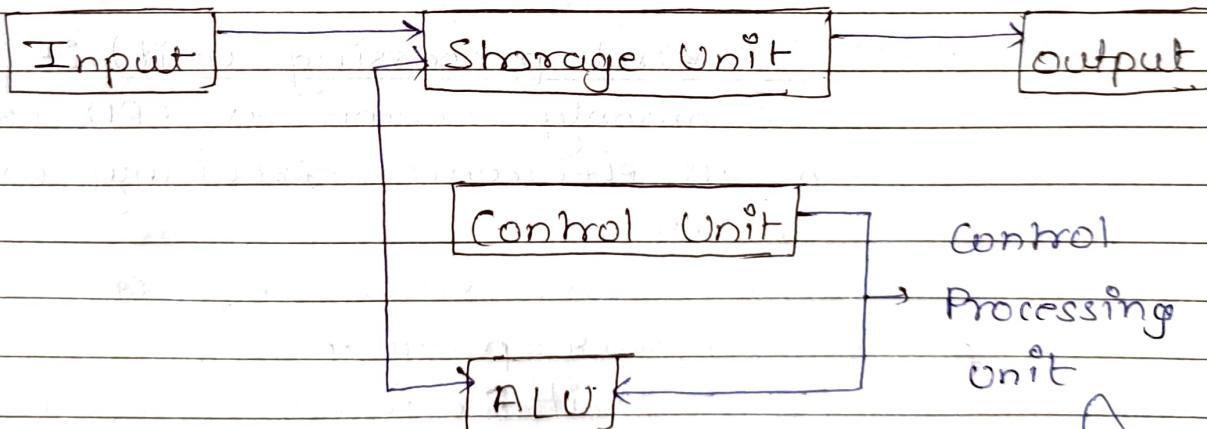


fig :- functional unit of dif digital system

⇒ Input Unit :-

- It is used by the computer by read the data.
- The most commonly used input devices are keyboard, mouse, joystick, Track balls, microphones etc.

(iii) Whenever a key is pressed the corresponding letter or digit is automatically translated into its corresponding binary code and transmitted over a cable to either the memory or the processor.

⇒ Control Unit :-

- i) It is a component of a computer CPU that co-ordinate the operation of the processor.
- ii) It tells the computer memory ALU and Input devices. How to respond to a program instruction.
- iii) The CU is also known as the nerve centre of a computer system.

⇒ CPU (Control processing unit) :-

- i) It is commonly known as CPU can be referred as electronic circuitry within a computer.
- ii) It carry carries out a instruction given by a computer program by performing the basic Arithmetic, logical, control and Input operations specified by the instruction.

Memory Unit :-

- i) It is referred as the storage area in which program are kept which are running and that contains data needed by the running program.

(ii) The primary (main) memory and secondary memory.

⇒ Primary Memory :-

i) Also known as volatile form of memory means when the computer is shut down anything contain in RAM is lose.

⇒ Secondary Memory :-

ii) It is used to when a large amount of data and program have to store for a long term basis.

iii) Also known as non-volatile memory i.e data is stored permanently irrespective of shut down computer.

⇒ ALU

i) Most of all the arithmetic and logical operation of a computer are executed in the ALU of the processor.

ii) It perform the arithmetic operation like addition, subtraction, multiplication, division and logical operation as AND, OR, NOT etc.

⇒ Output devices :-

i) Output devices displays information in a way that a user can be understand.

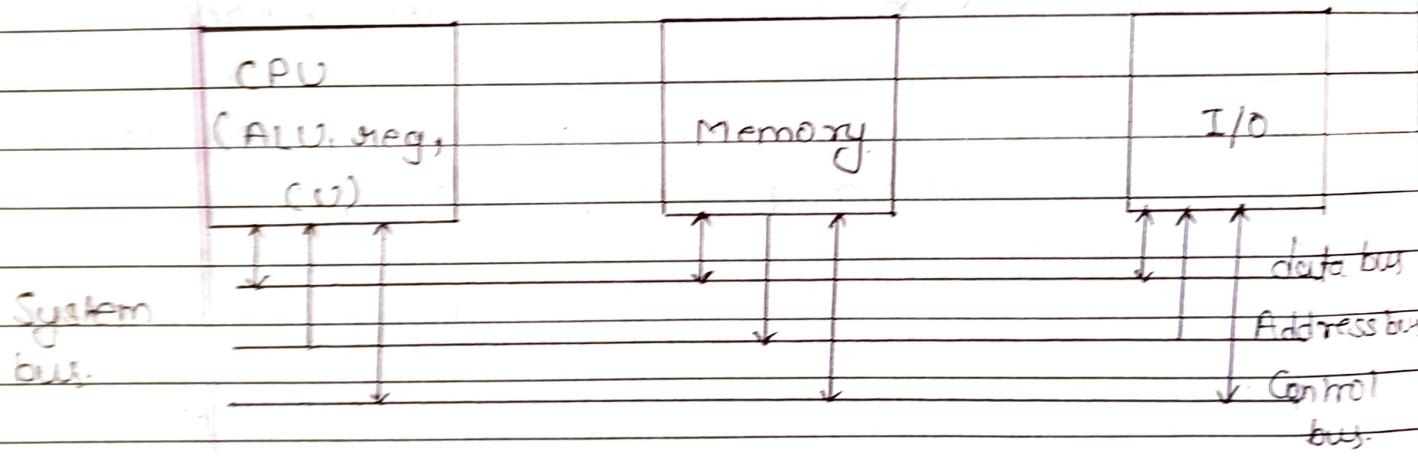
ii) The devices display information that has been held of as generated within a Computer.

iii) The most common example of a output devices is monitor, printer etc.

Bus :-

A communication path way connecting two or more devices. A collection of wire through which data is transmitted from one part of a computer to another part is known as Bus.

Bus architecture :-



A bus that connect major component (Processor, memory, I/O) is called system bus. A system bus contain about 5000 of separate lines in each line assign some function. System bus usually separated into three functional group.

- i) Data bus
- ii) Address bus
- iii) Control bus

- Data bus :- Carries the data.
- Address bus :- Collection of wires used to identify particular location in main memory.
- Control bus :- It regulate the activity of bus.

★ Bus Master :-

- i) Otherwise that initiate data transfer on the bus at any given time is called a bus master.
- ii) In Computer system, there may be more than one bus master such as a DMA controller or a processor etc.
- iii) This device share a System bus and when a current master bus recursive another bus acquire than control of the processor.

★ Bus Arbitration :-

- i) In a process by which next devices become the bus controller by bus mastership to another Bus. Bus arbitrator decided who would be the completely first bus master.
- ii) Bus arbitration schemes are usually based on places a two factor. Bus priority and fairness.

Bus priority :- It highest priority should be serviced first.

Fairness :- Even the lowest priority device should never be completely locked out from the bus.

Type of bus arbitration :-

- (i) Centralized bus arbitration :-
- (ii) Distributed bus arbitration :-

→ Centralise bus arbitration :-

- (i) In centralise bus arbitration a single bus arbiter perform the required arbitration.
- (ii) The bus arbiter may be the processor or a separate controller connected to the bus.

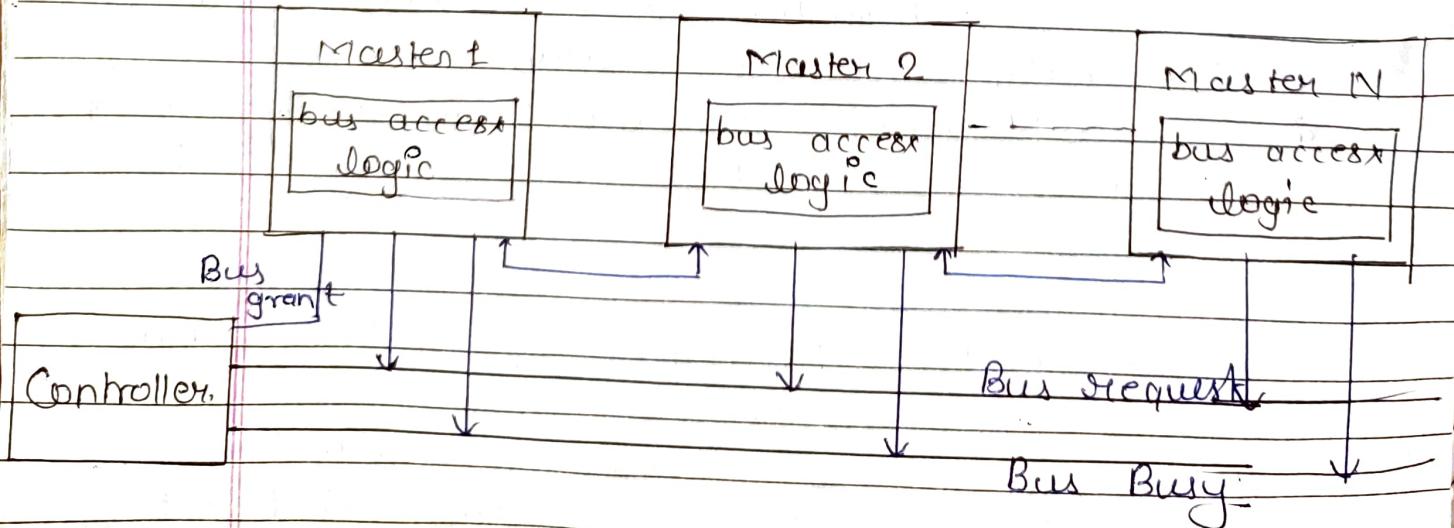
→ Distributive bus arbitration :-

- (i) In distributive arbitration all devices participate in the next bus master.

Methods of Centralise Bus arbitration

- (i) Daisy chaining method.
- (ii) Polling and rotating priority method.
- (iii) fixed priority or Independent request method

→ Daisy chaining method :-



It is a simple and cheaper method all the master use the same line for making Bus request.

WORKING :- All the bus master use the same time for Bus request.

- (i) If the bus busy line is inactive the bus controller give the bus grant signal.
- (ii) Bus grant signal is propagated serially through all master starting from nearest one.
- (iii) The bus master which requires system bus has stop the signal activate the bus busy line and take control the system bus.

Advantages :-

- (i) Simplicity.
- (ii) Less No. of control line.
- (iii) The user can add more device along the chain upto a certain maximum value.

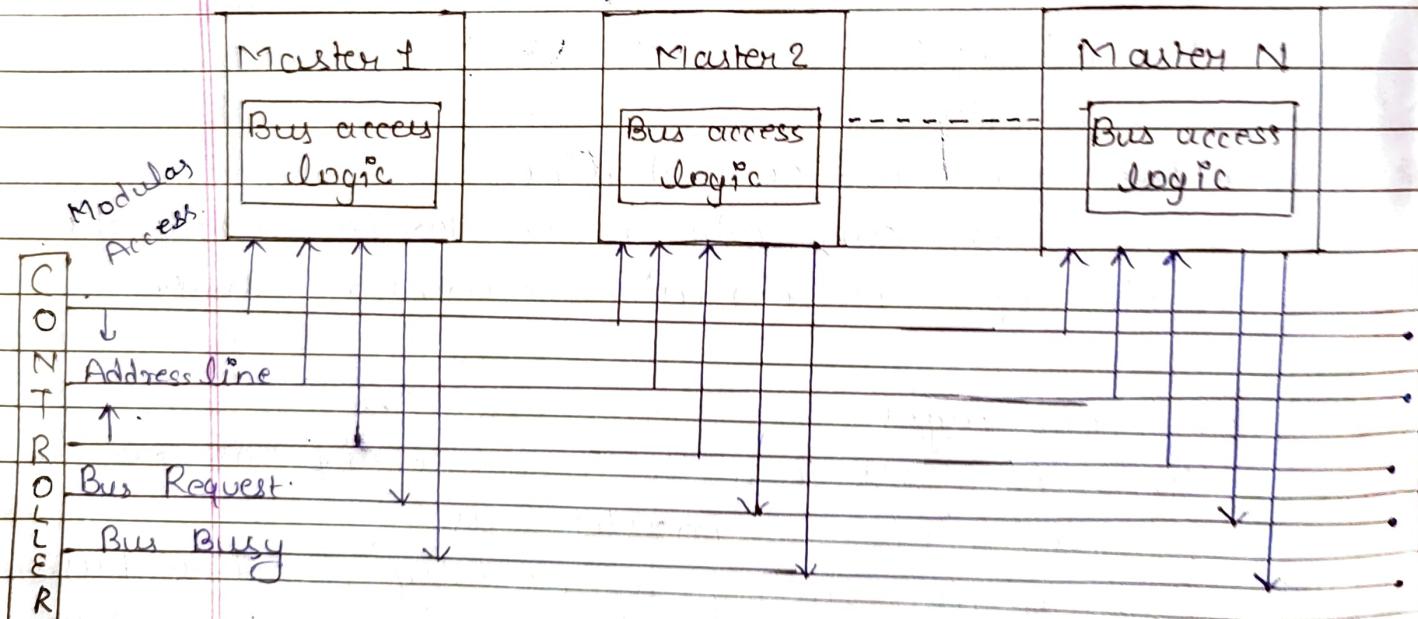
Disadvantages :-

- (i) Priority assigned to a device depends on the position of the master bus.
- (ii) Propagation delay to serially granting Bus. If one device fails than the entire system will stop working.

(2) Polling or Rotating priority method :-

- (i) Controller is used to generate a address line for the master.
- (ii) All bus master used the same lines for bus request.

- (iii) Ex :- If there are 8 master connected in a system atleast 3 address line are required.
- (iv) Controller generates binary address for the master (ex → To connect 8 bus master we need 3 address line [$2^3 = 8$])
 $[2^n = n \Rightarrow \text{No. of address line}]$
- (v) In response to a bus request the controller wholes the bus master by sending a sequence by bus master address on address line.
- (vi) When requesting master recognizes its address . it activate the bus busy line and take control of the bus.

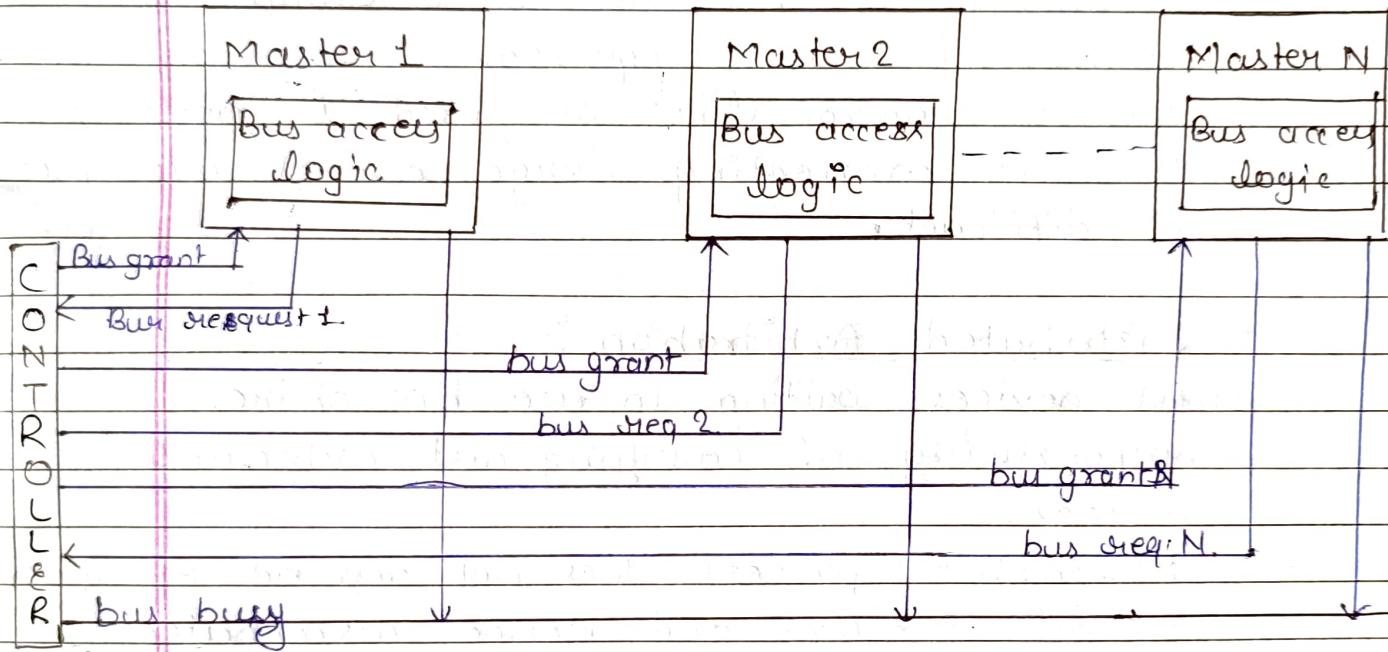


Advantages :-

- i) This method does not favour any particular device and processor.
- ii) Simple method.
- iii) If one device fail then whole system are not stop the working.

Disadvantages :-

- (i) Adding bus master is difficult as increases the number of address line of the circuit.
- fixed priority or independent request method.



WORKING

- (i) Each bus has its own bus request and a grant.
- (ii) The built-in priority decoder selects the highest priority request.
- (iii) All bus masters have their individual bus request and bus grant line.
- (iv) The controller thus knows which master has requested, so bus is granted to that master.
- (v) Priorities of the masters are predefined so - on simultaneous bus request, bus is granted based on the priority provided the bus line is not active.
- (vi) The controller consists of encoders and decoders logic for priorities.

Advantage :-

- (i) Fast response.
- (ii) Speed independent of no. of device connected.

Disadvantage :-

- i) Hardware cost is high as a large no. of control lines are required.
- ii) No. of control lines required is more therefore connecting large no. of bus masters is difficult.

Distributed Arbitration :-

- ii) All devices waiting to use bus share. The responsibility of carrying out arbitration process.
- iii) Arbitration process does not depend on upon Central arbitor. and Hence distributed arbitration has high ~~real~~ reliability
- iv) Each device is assign a 4-bit ID Number
- v) All the devices are connected using 5-lines 4-arbitration line, 2-transmit the ID, and one line for the start arbitration signal.

To request to bus a device.

1. Assert the ~~the~~ start arbitration signal placed it 4-bit Id number on the ~~the~~ arbitration lines.
2. The pattern that appear on the arbitration lines is the logical OR of all the 4-bit device placed on the arbitration lines.

3. Device A has the ID-5 and wants to request the bus transmit the pattern 0f01 on the arbitration line.
4. Device B has the ID-6 and wants to request the bus transmit the pattern 0f10 on the arbitration line.
5. Pattern that appears on the arbitration line is the logical OR of the pattern 0f11 appears on the arbitration line.

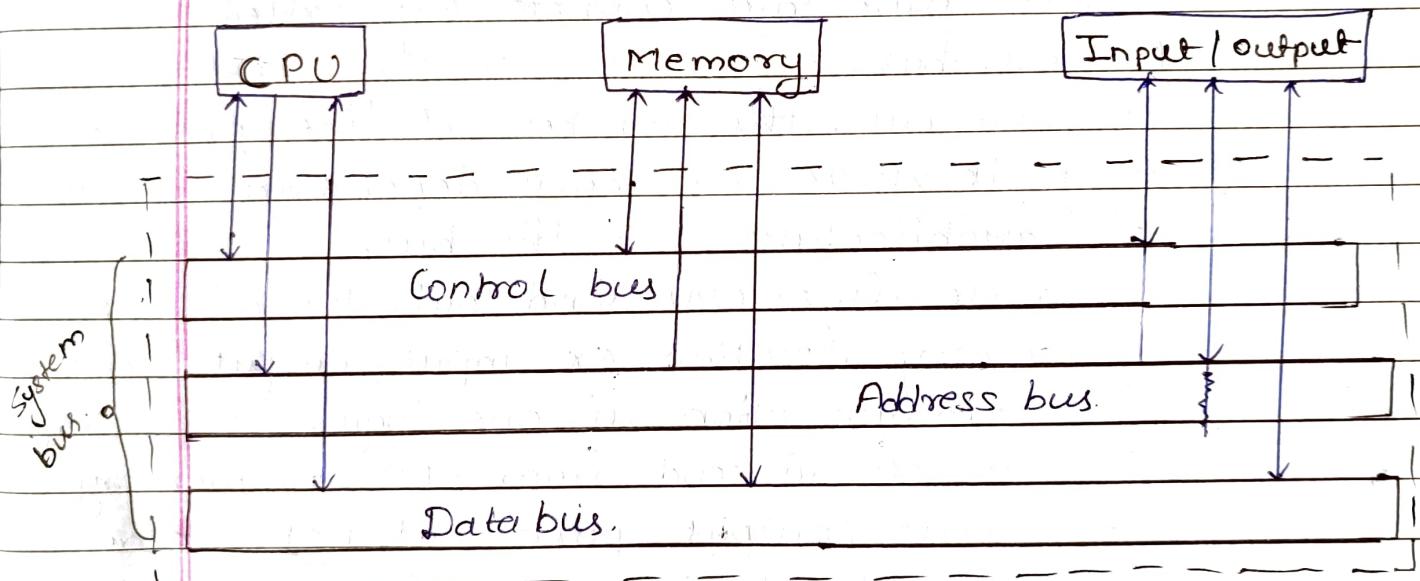
Arbitration process :-

- Each device compares the pattern that appears on the arbitration lines to its own ID starting with MSB (Most significant bit)
- If it detects a difference, it transmits 0s on arbitration line for that all lower bit position.
- Device 'A' compares its ID-5 with a pattern 010 to pattern 011.
- It detects a difference at bit position '0', as a pattern 0100 on the arbitration line.
- The pattern that appears all the arbitration line is the logical -OR of 0100, 0110 which is 0110.
- This pattern is the same as the device ID of B, hence B has 1 bit arbitration

Introduction to the Bus :-

- Bus is sub-system that is used to transfer the data and other information to b/w devices
- Various devices in a computer such that monitor, CPU, Input/output etc communicate to each other through bus.
- In general a bus is said to be as the communication path way connection two or more devices.
- A key-characteristic of a bus is that it is a shared transmission medium because multiple devices are attached to a bus.

- A bus consist by multiple communication path way on lines which are either in form of wires or metal line attach in a card or board.
- Each line is capable of transmitting binary 1 and binary 0.
- Computer system contains a number of different buses that provide path ways between components at various level of computer.



There are Three type of Buses :-

- i) Data bus
- ii) Address bus
- iii) Control Bus

→ Data bus :-

- Data line provides a path for moving data between the system module.
- It is bi-directional which means Data lines are used to data transfer in both

direction.

- o for Example CPU can read the data on these line system from the memory as well as send data to memory location to a port.
- o If any Bus number of line in data line are either (8, 16, 32) or more depending on size of Bus, These line connectively one called as Data Bus.

→ Address Bus :- collectively

- o Address line are connectively called as Address bus.
- o In any Bus, the number of line address are using 16, 20, 24 or more depending on type of architecture of the bus.
- o On these line CPU send out the address of memory location or input/output port.
- o The communication is one way. for example The address is send from CPU to memory and Input /output port but not memory and Input /output port send address to CPU on that line enhance these lines are unit directional.

→ Control Bus :- collectively.

- o Control lines are connectively called as control bus.
- o They have used by CPU for communicating with other devices within a Computer for for Example - CPU send signal on the control bus to enable the output of address memory devices and port devices.

- Typical Control Line Signals are memory read, memory written, Input / output read, Input / output written, bus request, bus grant.

Operation of Bus :-

The operation of Bus is as follows :-

- If one module which we to send data to another, it must do two thing :-
 - Obtain the use of module bus,
 - Transfer data to the bus.
- If one module which is request to data from another module it must :-
 - Obtain the new.
 - Transfer the request to other module over the appropriate control the address line and then it must wait for that second module to send to data.

Types of Bus :-

There are ~~are~~ variety of Buses, but some of widely use buses are system bus.

→ System Bus :-

- A bus that connect ~~connect~~ major component (Processor, memory, I/O) is a system bus.
- It is a single computer bus among all buses that connects all the components.
- It is ~~at~~ only bus in which data lines, address, control lines all are present. It is also known as front side Bus.

- It is faster than peripheral bus (PCI, ISA etc) but slower than back-side bus.

Peripheral bus :-

- It is also known as Input output bus.
- It is data pathway that connect peripheral device [keyboard, mouse] to the CPU.
- All in Computing, a peripheral bus is a computer bus design to support computer peripherals like - printer, hard drives etc.
- The PCI and USB buses are commonly used peripheral buses and are today used in commonly in PC.

PCI [Peripheral Component Interconnect] :-

- PCI Bus connects the CPU and expansion boards such as modem cards, Network cards and sound cards.
- These expansion boards are normally plugged into expansion slots on the motherboard.
- That is why PCI bus is also known as expansion bus or External bus.

USB [Universal serial bus] :-

- USB is used to attach USB devices like pendrive etc to CPU.

~~ISA~~ Local bus :-

- It is the traditional Input output (Peripheral bus such as ISA, MCA or EISA bus).
- ↳ ISA (Industry standard Architecture bus):-
- The ISA bus permit bus mastering that it enable peripheral connecting directly to the bus to communicate directly with other peripheral without going through the processor.
- One of the consequences of bus mastering is directing memory access.
- upto end of 1990's almost all PC's were equipped with ISA bus but it was progressively replaced by PCI bus which performing better performance.

~~MCA~~ MCA (Micro channel Architecture) :-

- It is an improved proprietary bus designed by IBM in 1987 to be used in their PS/2 lines of Computer.
- This 16 to 32 bit bus was incompatible with the ISA bus and could reach a throughput and 90 Mbps.

EISA : (Extended Industry standard Architecture)

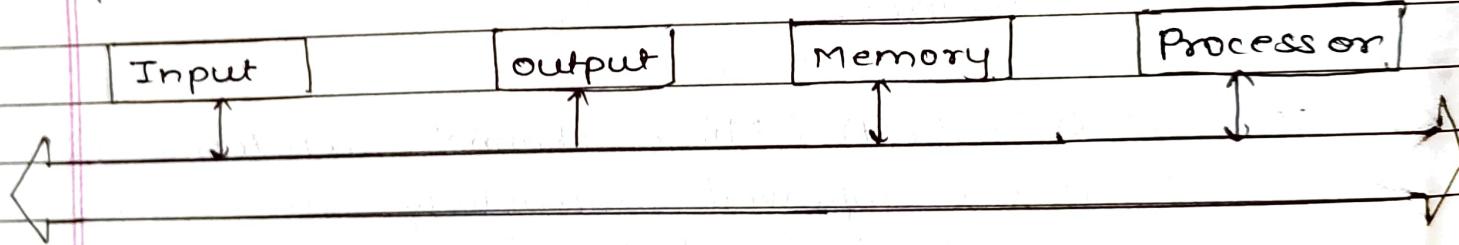
- It was developed in 1988 by a consortium company.
- The EISA bus used connector that were same size as the ISA co

- High speed bus are supporting high capacity I/O devices.
- High speed bus bring high demand device into closer integration with processor.
- This bus support connection of to high speed LANs such as fast ethernet 800 mbps, video and graphics, work station, fire wire.

Type of Bus structure :-

(1) Single Bus structure :-

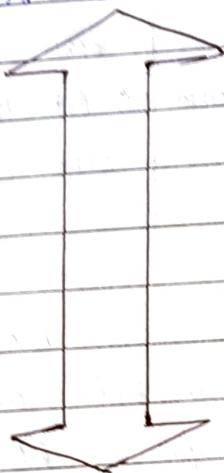
- All units are connected to a single bus, so it provides the sole means of interconnection.



- It has advantages of simplicity, low cost, many devices can be connected.
- It has disadvantages of limited speed since usually only two unit can participate in data transfer. If at any time therefore an arbitration system is required on that unit will be forced to wait.
- Bus control line are used to arbitrate multiple request for the use of the bus.

(2) Double bus structure:

- Double bus structure is used to overcome the bottleneck of single bus structure.
- It uses two buses - one bus is used to fetch instruction and other is used to fetch data required for execution.



- In the first configuration, the processor is placed b/w I/O unit and then memory unit.
- The processor is responsible for any data transfer b/w I/O using and the memory unit.
- The processor act as a messenger.

* Single Bus structure v/s Double bus structure:-

Single Bus

- One common bus is used for communication b/w peripherals and processor.
- Instruction and data both are transferred in the same bus.
- Its performance is low.

Double bus

- Two buses are used one for the communication from peripheral and other for processor.
- Instruction and data both are transferred in the different bus.
- Its performance is high.

- Cost of single bus structure is low.
- No. of cycle for structure execution is more.
- Execution process is slow.
- No. of Register associative are less.
- At the time single operand can be read from bus.

- Cost of double bus structure is high.
- No. of cycle for execution is less.
- Execution process is fast.
- No. of Register associative are more.
- At the time two operands can be read from bus.

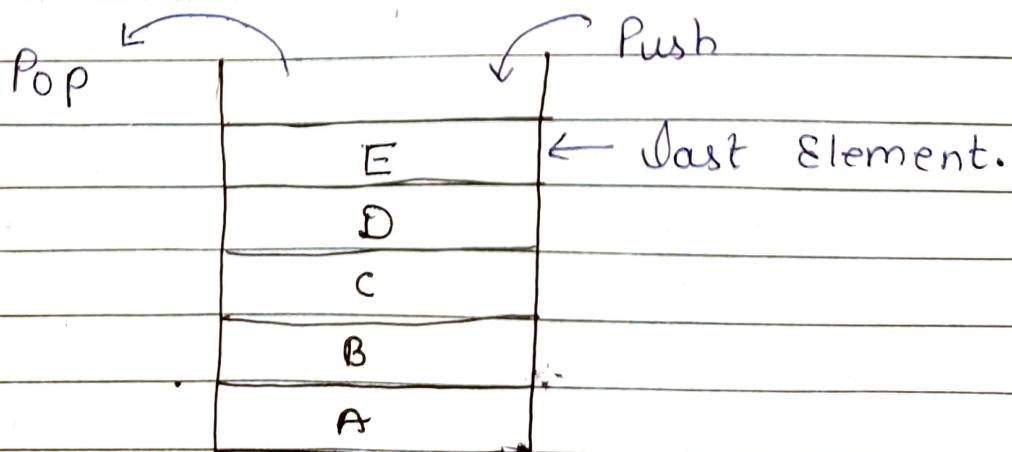
Registers :-

- Registers is very fast computer memory used to store data / Instruction in execution.
- A Register is a group of flip-flop if each capable of storing 1-bit of information.
- An 'N'-bit register has a group of 'N'-flip-flop and is capable of storing binary information of N-bits.
- A register is consist of group of flip-flop and Gates.
- The flip-flop holds the binary information and gates controls when it flow and gates control when a new information is transfer into a register.
- A various types of register are available commercially.
- The simplest register is one that consist of only flip flop with no external gate. Some of the commonly used register are :-
 - (a) Accumulator :- This is the most common register used to store data taking out from the memory.

data intermediate result during program execution it can be accessed by assembly programming.

STACK :-

Stack is also known as the LIFO (last In first Out). It is the most important feature of CPU it saves data such that the elements stored last is retrieve first. This stack is a memory unit with an address register. This register influences the address for the stack which is known as stack pointer. The stack pointer ~~can~~ influences the address of the element that is located at the top of the stack. It can insert an element into or delete an element from the set. The insertion operation is known as push operation and deletion operation is known as pop operation. In computer stack these operations are simulated by the incrementing or decrementing the stack pointer register.



- Stack is a storage device for storing information in manner of LIFO.
- Stack is the memory unit within address for register called stack pointer.
- Stack pointer always points of the top element in the stack.
- Two operation of the stack →
Push :- Insertion \Rightarrow Increment SP
pop :- Deletion \Rightarrow decrement SP.

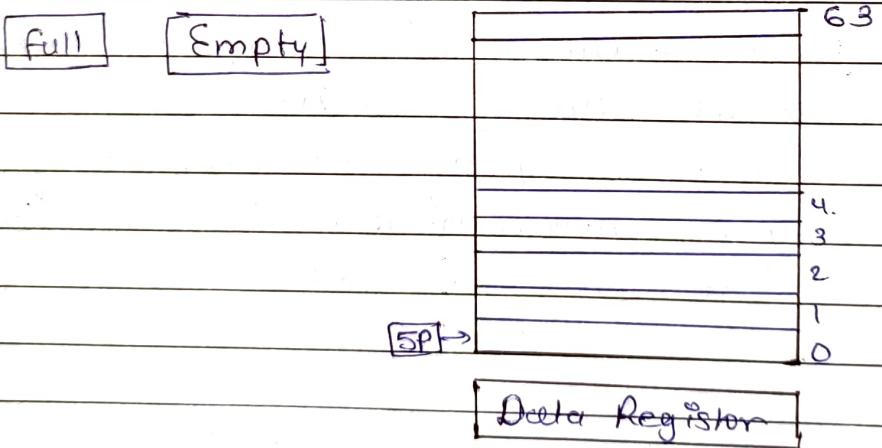
Type of Stack :- There are two type of stack.

Register stack :- Stack depth limited

Memory stack :- Stack depth flexible.

* Register stack organisation :-

Address



Push

$$SP \leftarrow SP + 1$$

$$M[SP] \leftarrow DR$$

if ($SP == 0$) then ($full \leftarrow 1$)

$$Empty \leftarrow 0$$

Pop

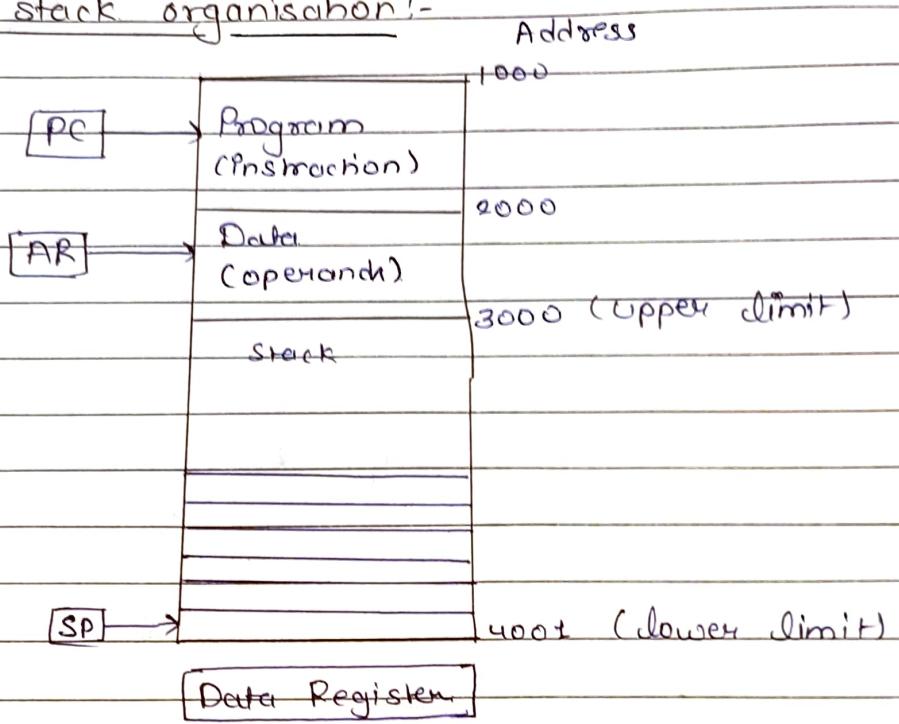
~~$M[SP] \leftarrow DR$~~

$$DR \leftarrow M[SP]$$

$$SP \leftarrow SP - 1$$

if ($SP == 0$) then ($Empty \leftarrow 1$)
($full \leftarrow 0$)

* Memory stack organisation:-



Push

$$SP \leftarrow SP - 1$$

POP

$$DR \leftarrow m[SP]$$

$$m[SP] \leftarrow DR$$

$$SP \leftarrow SP + 1$$

(CLA (Carry Look Ahead Adder))

- A digital computer must contain circuit to perform arithmetic operation like add, sub.
- Among these addition and subtraction are the basic operation where as multiplication and divide are the repeated addition and subtraction respectively.