

UNIT-1

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SYLLABUS:-

1. Functional unit of digital system and their interconnects
2. Buses: Architecture of Bus
Types of Busses
3. Register Transfer, Bus transfer, Memory Transfer
4. Processor organization
5. General Register organization.
6. Stack organization and addressing modes



1. FUNCTIONAL UNIT OF DIGITAL SYSTEM AND THEIR INTERCONNECTS:-

⇒ DIGITAL SYSTEMS:-

- A digital system is a system that stores the data in a discrete way
- Digital system stores the information in a binary form
 - i.e., either zero (0) or one (1)

- # When you are talking about digital system, a well known example i.e., general purpose computer come in a mind
- # A general purpose computer system is a best known example of a digital system
- # Other example include telephone switching exchange, digital voltmeter, digital counter, electronic counter and digital displays etc.

The functional unit :-

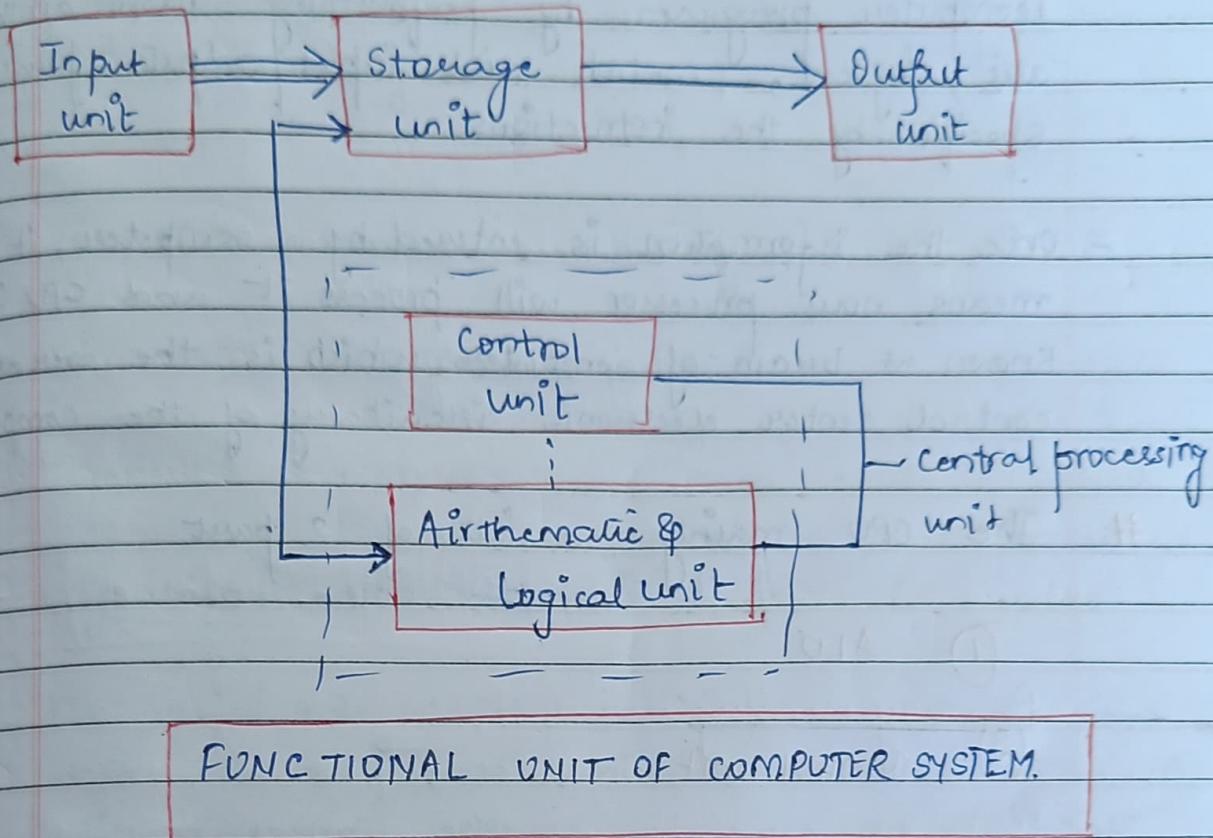
A computer consists of five main components

- Input
 - Output
 - Memory
 - Arithmetic and Logical unit }
 - control unit }
- Central processing unit

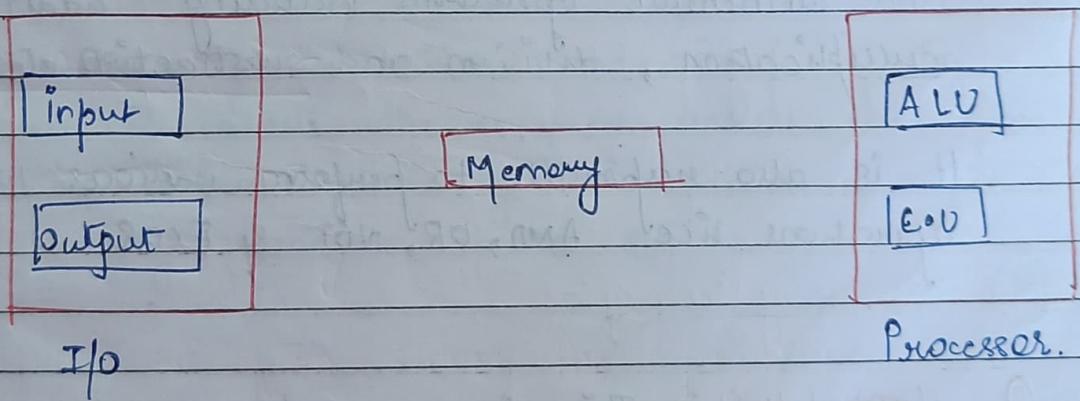
The Arithmetic and logical unit and control unit is a part of central processing unit

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Block diagram of a functional unit representation of computer system:-



or in a more broad way



CPU:- Central Processing unit

PROCESSOR PART

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1. Central Processing Unit (CPU):-

- It is an electronic circuitry within a computer which carries out the instruction given by a computer program by performing basic arithmetic, logical, control and input/output operations specified by the instructions.
- Once the information is entered by a computer, it means now processor will process it and CPU is known as brain of computer which is the overall control center electronic circuitry of the computer.

The CPU mainly consists of 2 parts

① ALU

② Control unit

① ALU: (Arithmetic and logic unit):-

As the name suggests it performs the logical and arithmetic operations including addition, multiplication, division and subtraction etc.

It is also responsible to perform various logical operations like AND, OR, NOT & XOR.

② Control unit: This is a component of computer's CPU that coordinates the operation of processor.

- It tells the computer memory, arithmetic/logical unit and input / output devices. how to respond to a program instructions.

- The control unit is also known as the nerve centre of computer system

[Input output PART]

Input / output Unit :-

- 1 - Input unit :- An input is a unit that will help to provide the data to CPU, where it get processed by CPU and the result is either sent to memory to store or it is presented to O/P (output) unit.
- One major role of input unit is to convert the raw data into a format which is readable by the CPU.
Mic, Keyboard, mouse, camera eg. of input devices.

- 2 - OUTPUT UNIT :- It is a unit which accepted the result produced by CPU in an encoded form
- now it convert the encoded result into form which it is understandable by human.
eg, printer, speaker etc

MEMORY :-

[MEMORY PART]

MEMORY :-

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- It is referred as the storage area in which the programs are kept which are running and contains data needed by running the programs.
- It is a unit which is hold the data, program the data and also stores the result of operations
- The memory unit is categorised as
 - Primary Memory (Volatile memory)
 - Secondary memory (Non Volatile memory)

Primary Memory :-

volatile

- It is known as the volatile form of memory means when the computer is shutdown, anything contained in RAM is lost.
- " small in capacity
eg: RAM & ROM, but high speed"

(2)

Secondary Memory :-

- It is used when a large amount of data and programs have to be stored in long term basis
- Also known as the non volatile memory form i.e. data is stored permanently irrespective of

Shut down

• Examples are magnetic disks, magnetic tapes, and optical disks

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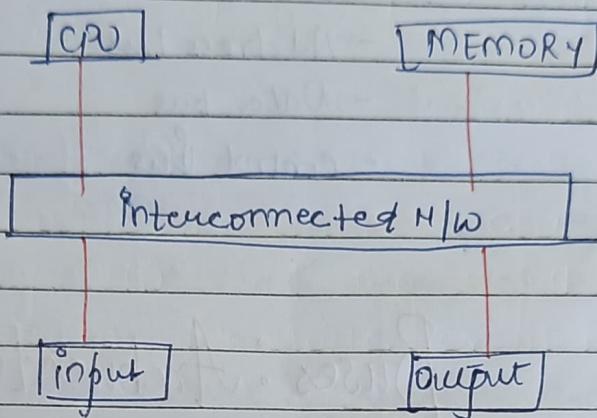
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"slow speed but store large data"

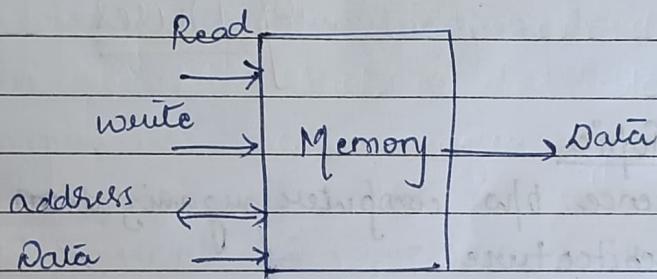
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INTERCONNECTIONS BETWEEN FUNCTIONAL COMPO-

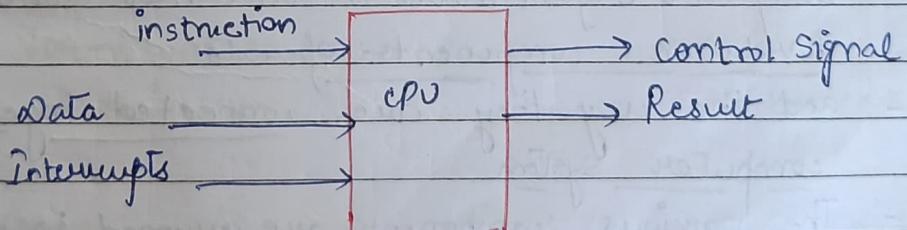
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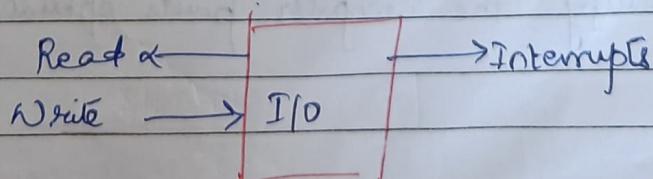
Memory :-



CPU :-



I/O :-



1. The major part of microcomputers are central processing unit (cpu), memory and I/O unit
2. To connect these part together through three set of parallel lines, called buses
3. Three types of buses are
 - Address bus
 - Data bus
 - Control bus

Buses : Architecture & Type

of Buses

Imp. Topic

Difference b/w computer organization & computer architecture.

- Computer organization is concerned with the way the hardware components operate
- and the way they are connected together to form a computer system
- The various components are assumed to be in place & task is to investigate the organizational structure to verify the computer parts operate as intended

Computer Architecture :-

It is concerned with the structure and behaviour of the computer as seen by the user.

It includes the information, formats, the instruction set and techniques of addressing memory.

- The architectural design of computer system is concerned with the specification of various functional modules such as processor and memories, structure them together to form computer system.

Two basic type of computer architecture

- Von Neumann architecture
- Harvard architecture
- Von Neumann architecture :- describe general framework that a computer H/w, programming and data should follow.

How CPU is accessing the data and code with memory i.e. case is described in von Neumann and Harvard architecture.

Von - Neumann
Architecture

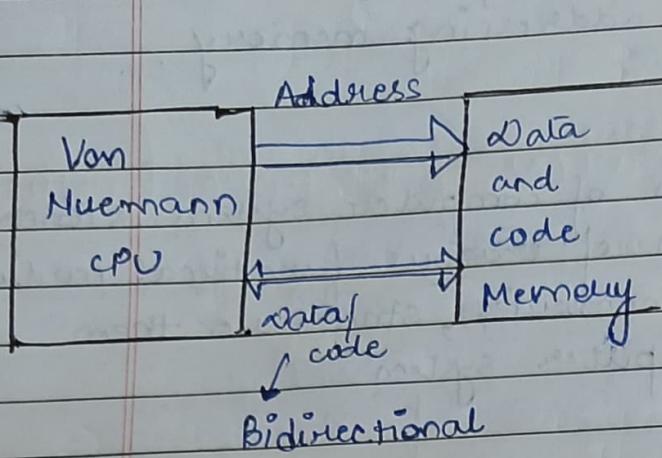
- For data and code we have single memory

Harvard
Architecture

For data and code we have separate memory

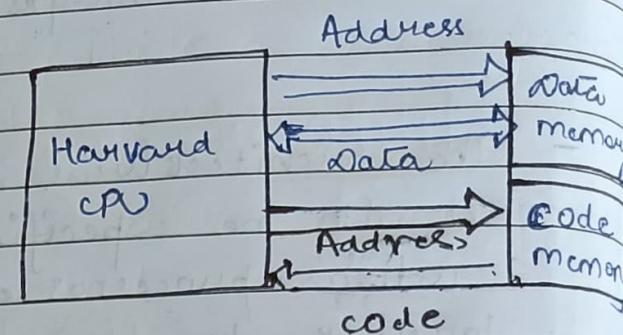
Von-Nuemann

Architecture



Harvard

Architecture



- ① Here data and code memory are separate
- ② Here addressing is also separate

Program

Memory Data and program (code) are stored in a same memory

Data and program are stored in a separate memory

Memory Type It has only RAM for data & code

It has RAM for data & ROM for code

Buses common bus for address and data

Separate bus address and data / code

Program Execution code is executed serially and takes more time cycles

code is executed in parallel with data so it takes less cycles

"either read or write operation is performed"

read and write operation performed parallelly

Von -

Niemann
Architecture

Howard

Parc
Data : G
Architecture

Data and
code transfer

Data or code
in one cycle

Data and code in
one cycle

control
signals

Less

More

As you have
data and code
memory with
separate address

Space Less requirement of
 Space

It need more space

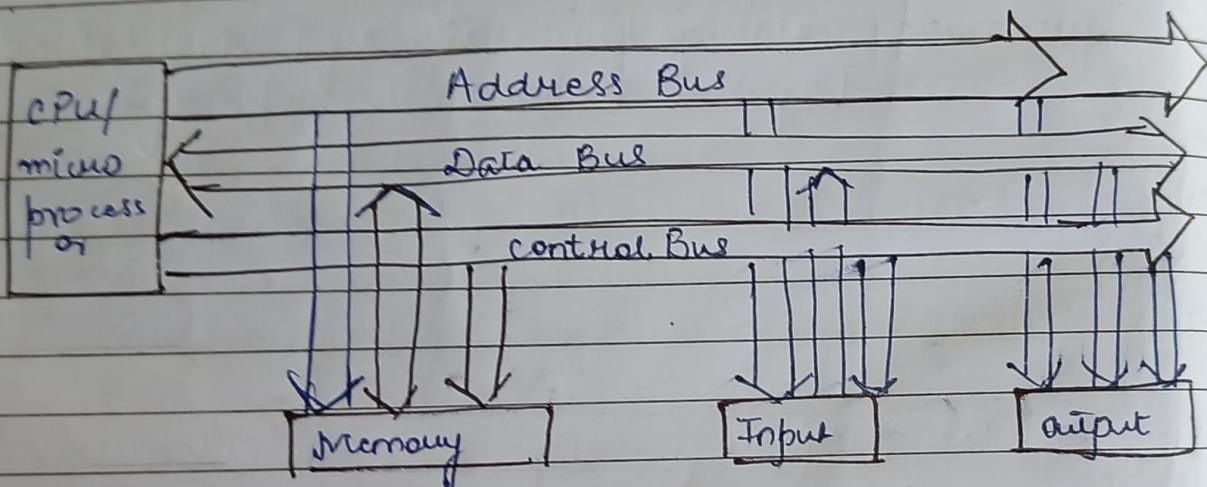
cost less

Costly

Buses:

- It is a group of conducting wires that carry the information.
- All the peripherals are connected to CPU or microprocessor through bus

"Diagram":



There are 3 types of Buses

1. Address bus:- generally used to carry the address
2. Data Bus:- carrying the data
3. Control Bus:- carrying the control of signal

Working of each buses:

Address Bus:-

Explanation:- Suppose, you want to fetch some data or any information at that time the CPU will generate an address, and via address bus, you will reach to that particular location from where you want to fetch the data and that location is present there at address bus.

⇒ Its length = 16 bits i.e., it can store up to 2^{16} locations data

An example:-

Suppose an address bus length = 3 bits so in total I have 8 locations

000		0
001		1
010		2
011		3
100	2	4
101		5
110		6
111		7

⇒ we can represent it via 3 bits and we have in total 8 location where you can store data

so, for 2^3 = we have 8 locations, from all those slots, from where you have to store data is there in address bus

In previous case, the address bus contains 100 value.

Address Bus :-

write up :- It is a group of conducting wires that carries address only. It is unidirectional because the information or address flow in one direction i.e., from μ P/CPU to memory or from microprocessor/CPU to I/O devices.

\Rightarrow The length of address bus (e.g.: 16 bit or 20 bit) determines amount of memory system can address.
ex :- System with 32 bit address bus can have 2^{32} memory location. If each location holds one byte the addressable memory space is $4GB = (2^{32} = 2^{16} \times 2^{16}) = 4GB$)

#

2. Data Bus :-

Explanation :- How you want your data to read suppose you fetch anything from data bus or suppose you perform any task and how the result will display \rightarrow determined by data bus.

\Rightarrow # as data go from μ P to data bus to I/O

\Rightarrow The size of data should be considered from the address location

word :- Suppose you are using 2 byte word so in total = 16 bits

The data come from I/P
= 1 byte i.e.

= v

Suppose you are using
2 Byte word = 16 bits.

i.e., data bus use to represent
16 bits

000	
001	
010	
011	
100	
101	
110	
111	

Write up :-

Data bus :- It is a group of conducting wires,
which carries data only. It is Bidirectional
because data flow in both direction

For write operation, processor will put data on data
bus for read operation, memory controller will
get date from specific memory block and put it
on data bus

→ n bit data bus can represent 2^n unique values
→ 8 bit data bus can have $2^8 = 256$ or FFH
values in register to be processed

Control Bus :- For this we have a dedicated hard
ware and it is used to generate
timing and control signals to control all the
associated peripherals.

Some control signals are:

- Memory read
- Memory write
- I/O Read
- I/O write
- opcode fetch

#

Bus Arbitration in Computer

Organization

The bus arbitration is a decision of who get access of bus for reading and writing.

→ why we need arbitration?

We need arbitration because a multiple device at a same time need to access the bus. The bus arbitration refers to a process by which the current bus master access and then leaves the control of bus and passes it to another bus requesting processor unit.

- The bus arbitrator is a master, which is deciding which data has to be accessed first. As the data cannot be read at a same time only one device can be served at one time.
- Bus arbitration scheme usually try to balance the

- Bus priority

and

fairness (whether it provides service to all the device)

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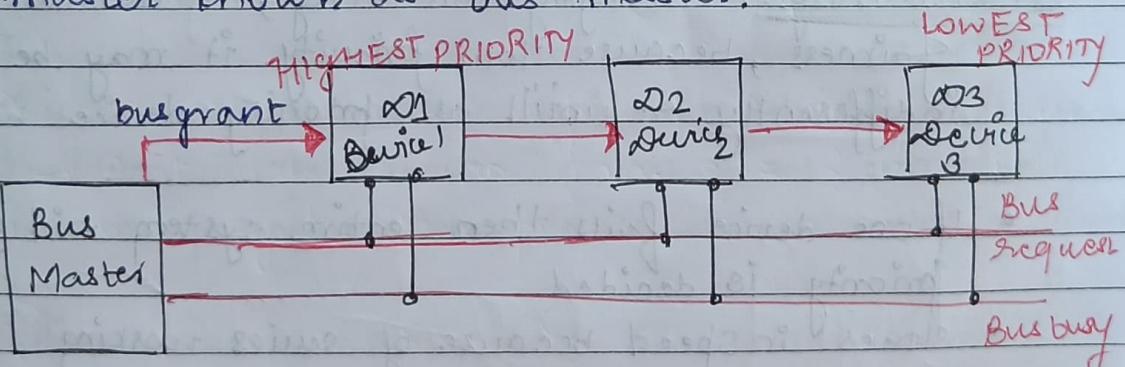
- There are three arbitration mechanism.

- Daisy chain mechanism
- Polling
- Independent request

To serve the device based on the priority is the main objective of these arbitration mechanism

Daisy Chaining Method:

- ① Every system or component is having only one master known as bus master.



Whenever the bus sending the bus request to the bus master the bus master will check that whenever the bus is free, the bus master first check the "highest priority device", i.e. D1, so bus master first sent the bus grant signal to D1 and whenever, D1 takes the

signal, "it sends the busy signal on the bus so that no other device can ask for the bus grant"

- After the work of D1 is over, it releases the bus, the D2 will take the bus request and the same process is performed.

So, after the completion of 1 device work, the device 2 can ask for bus request. It works like a chain

- The grant signal is passed from one device to another if the 1st device is not requesting the bus. Hence device near the arbiter have priority & stores the and it start or initiate bus request to other device.

Disadvantage :- Propagation delay, It cannot assure fairness, because low priority it may be locked indefinitely until all priority device will work

- If one device fails then entire system will fail, priority is decided.
- slower in speed because of series working

Advantage :- Simple

2. Polling or Rotating Priority Method

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