Assignment 4 Report
ELEC 4700

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1 Part 3: Report on the work done in PA 7

1.1 Part A: Write out the matrices C and G

```
%X = [V1,V2,IL,V3,V4,V0]

G =[1   0           0  0           0   0;
    G_1 -(G_1+G_2) -1  0           0   0;
    0   -1          0  1           0   0;
    0   0           1  -G_3        0   0;
    0   0           0  -alpha*G_3  1   0;
    0   0           0  0           G_4 -(G_4+G_0)];


C =[0         0          0 0 0 0;
    Capacitor -Capacitor 0 0 0 0;
    0         0          L 0 0 0;
    0         0          0 0 0 0;
    0         0          0 0 0 0;
    0         0          0 0 0 0];
%F = [Vin;0;0;0;0;0];
```

Figure 1: G and C matrices for modelling the circuit from PA 7

1.2 Part B: DC and AC sweeps of the circuit

1.2.1 Section i. DC sweep for input voltages -10 to 10V

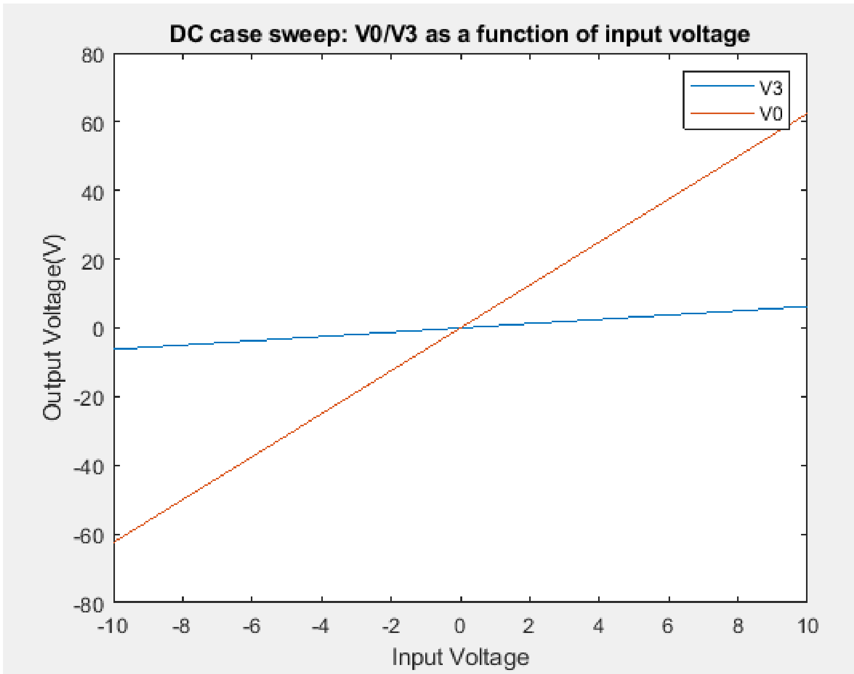

Figure 2: Sweep of the input voltage Vin from -10V to 10V and a plot of the output voltage VO and the voltage at V3

1.2.2 Section ii. AC sweep for output voltage as a function of frequency ω and a plot of gain

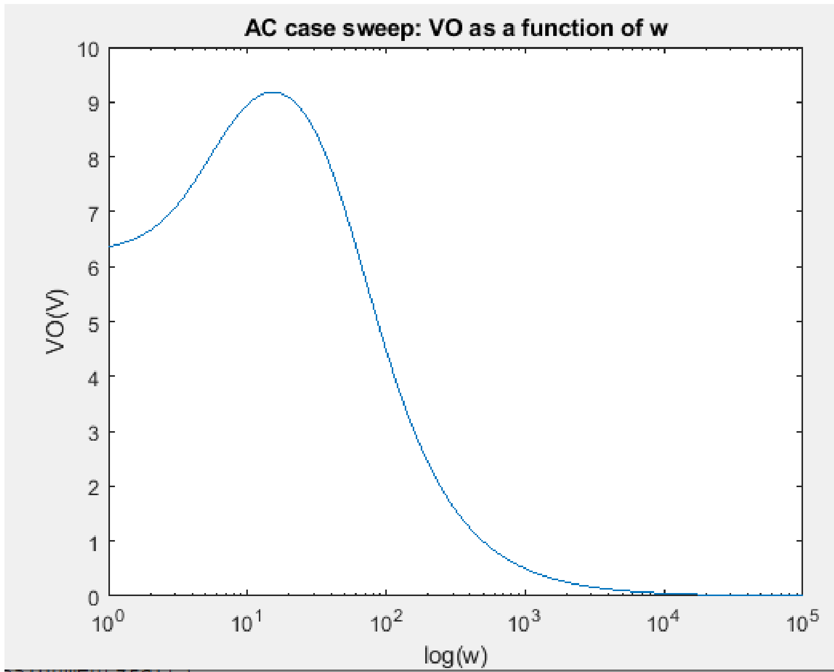

Figure 3: Plot for the AC case of the output voltage V0 as a function of log(ω)

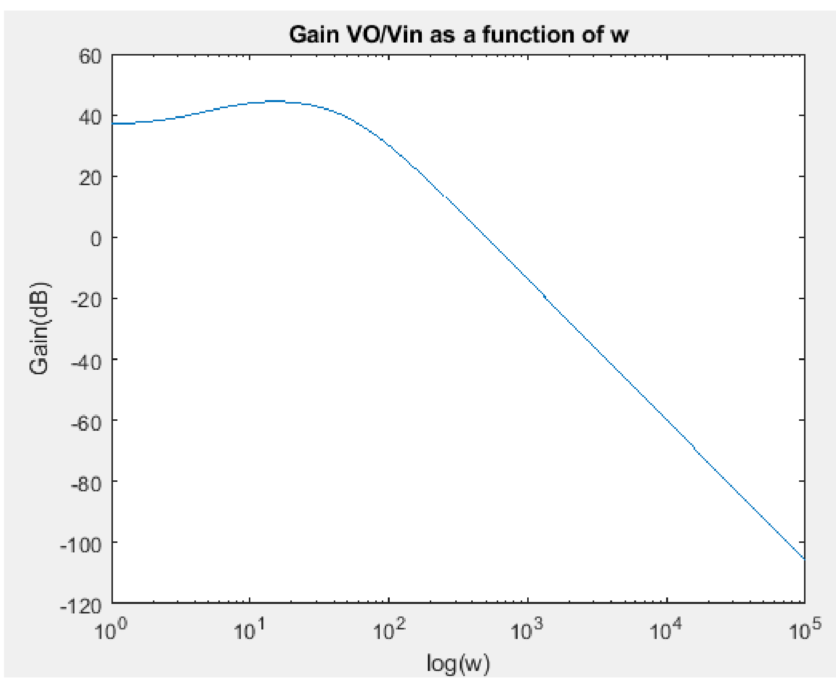

Figure 4: Plot of the gain V0/Vin as function of log(ω)

1.2.3 Section iii. AC gain as a function of random perturbations on C plotted on a histogram

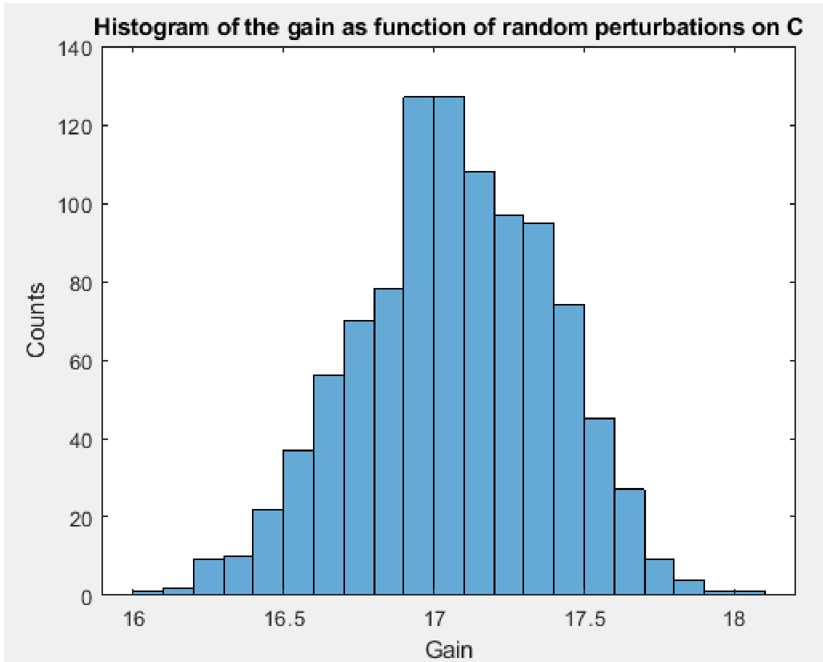

Figure 5: Histogram of the gain with random perturbations on the capacitor (C) using a normal distribution

2 Part 4: Transient circuit simulation

2.1 Part A: What type of circuit is this?

By inspection this circuit appears to be a low pass filter because the gain and output voltage is high at low frequencies. The gain/output voltage approach zero as the frequency increases.

2.2 Part B: What sort of frequency response would you expect?

Since this is a low pass filter we would expect the frequency to respond by being rejected/attenuated at higher frequencies while allowing the low frequencies to pass.

2.3 Part C: Derive a formulation using finite difference for the numerical solution of this equation in the time domain

Given the formula given to describe the circuit in the time domain,

$$C\frac{dV(t)}{dt} + GV(t) = F \tag{1}$$

this can be rearranged using finite difference to get the numerical solution to the equation in the time domain,

$$C\left[\frac{V(t+dt)+V(t)}{dt}\right] + GV(t) = F$$

$$V(t) = \left[\frac{C}{dt} + G\right]^{-1}\left[F + C\frac{V(t)}{dt}\right] \tag{2}$$

2.4 Part D: Simulation

2.4.1 Plots of Vin and Vout from numerical solution in time domain

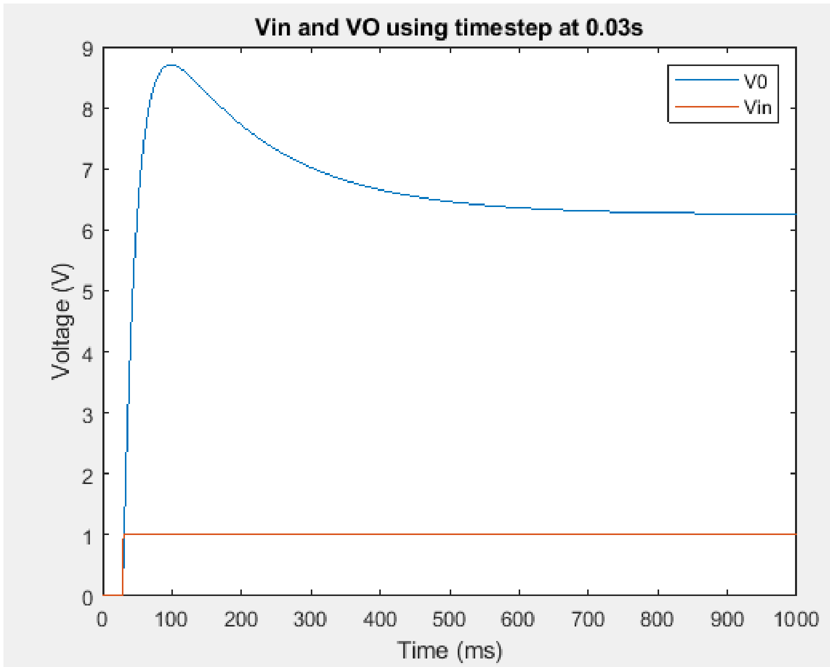

Figure 6: Plot of time step input signal that transitions from 0 to 1 at 0.03s. in the time domain

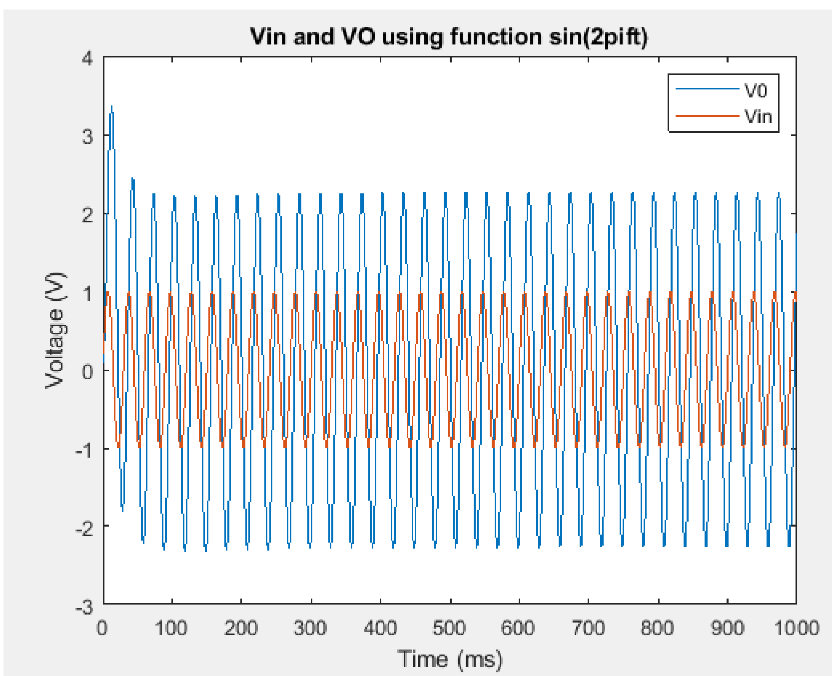

Figure 7: An input signal that is a sin(2πf t) function with f = 1/(0.03) 1/s in the time domain

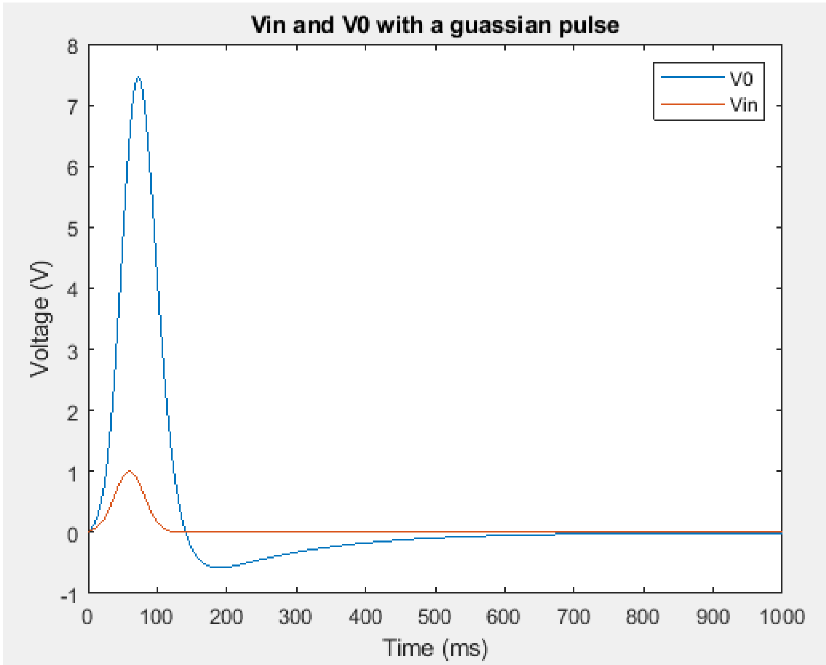

Figure 8: A Gaussian pulse with a magnitude of 1, std dev. of 0.03s and a delay of 0.06s in the time domain

2.4.2 Plots of the frequency content of Vin and Vout from Fourier Transform plots of Frequency response

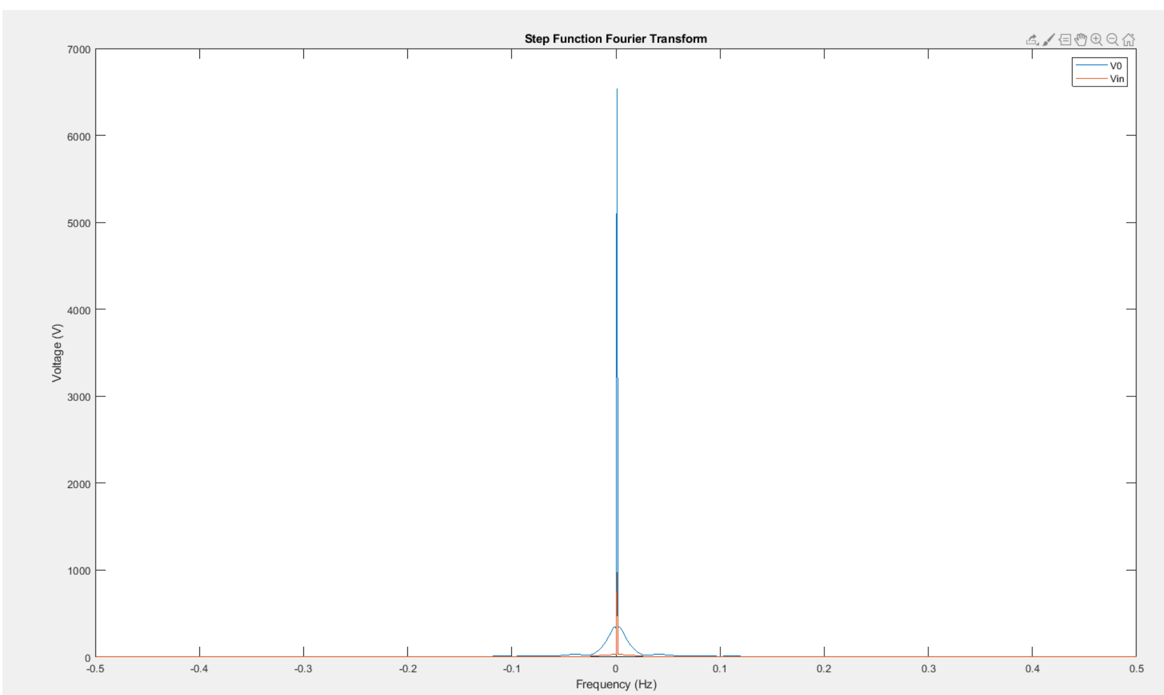

Figure 9: Fourier transform result of the time step

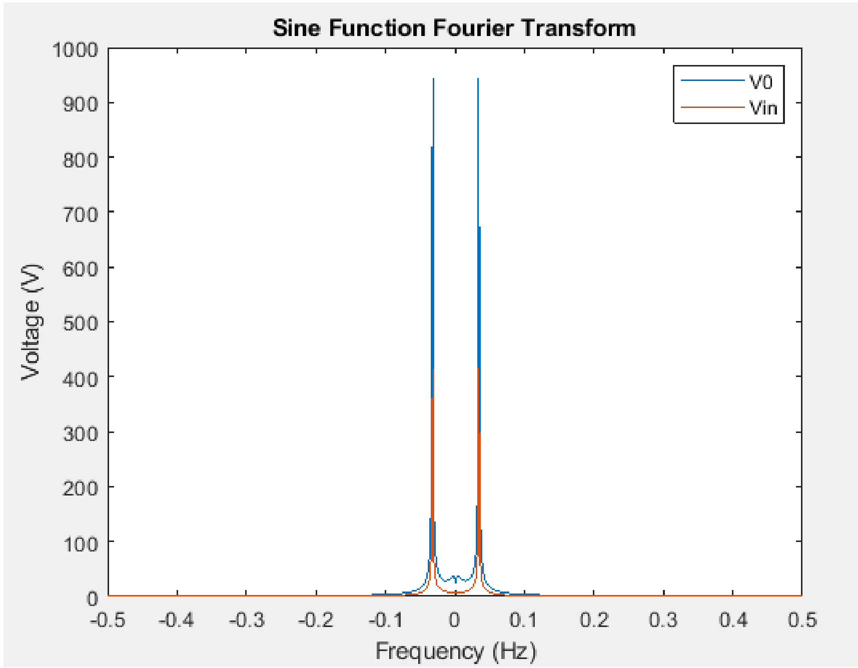

Figure 10: Fourier transform result of the sine wave input signal

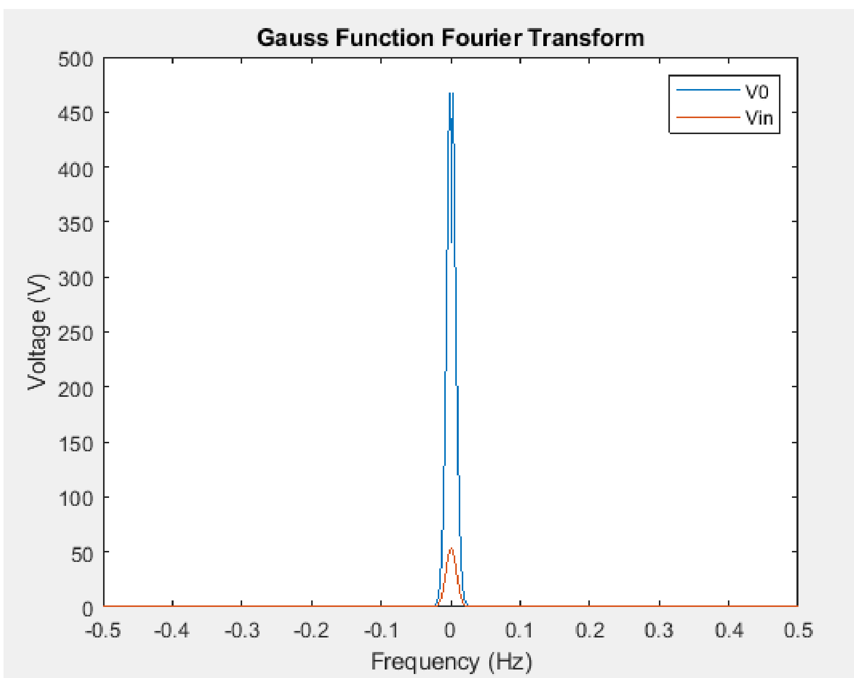

Figure 11: Fourier transform result of the Gaussian input signal

3 Part 5: Circuit with Noise

3.1 Part A/B: Updated matrix due to added capacitor in circuit

```
%X = [V1,V2,IL,V3,V4,V0]

G =[1    0           0   0           0    0;
    G_1  -(G_1+G_2)  -1  0           0    0;
    0    -1          0   1           0    0;
    0    0           1   -G_3        0    0;
    0    0           0   -alpha*G_3  1    0;
    0    0           0   0           G_4  -(G_4+G_0)];


C =[0         0          0 0    0 0;
    Capacitor -Capacitor 0 0    0 0;
    0         0          L 0    0 0;
    0         0          0 -C_n 0 0;
    0         0          0 0    0 0;
    0         0          0 0    0 0];

F = [Vin;0;0;0;0;0];
```

Figure 12: Updated matrix to include the new capacitor C_n that is in parallel with the R_3 resistor

3.2 Part C: Simulation

3.2.1 Section iv. New output of V0

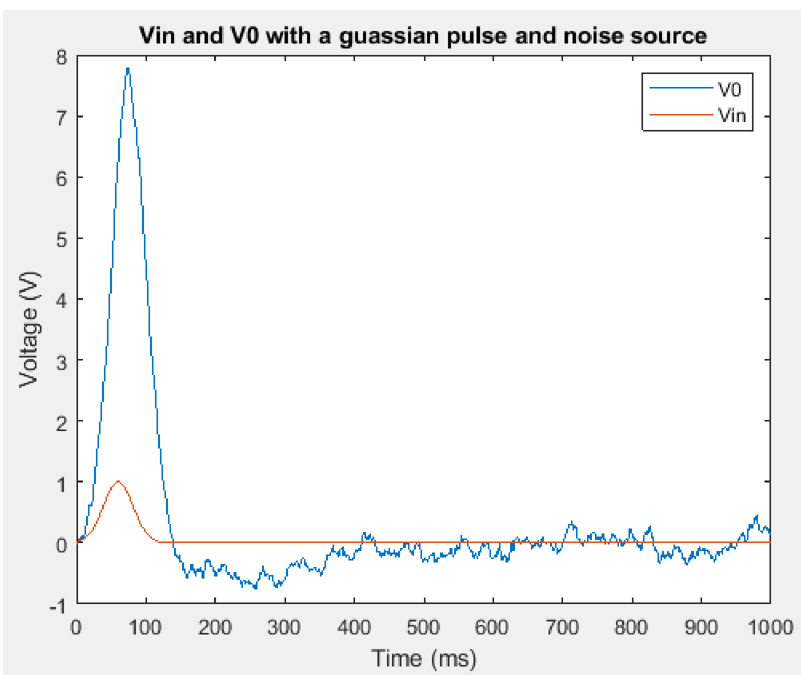

Figure 13: Model the output voltage (V0) signal with noise using the Gaussian excitation

3.2.2 Section v. Fourier transfer of V0

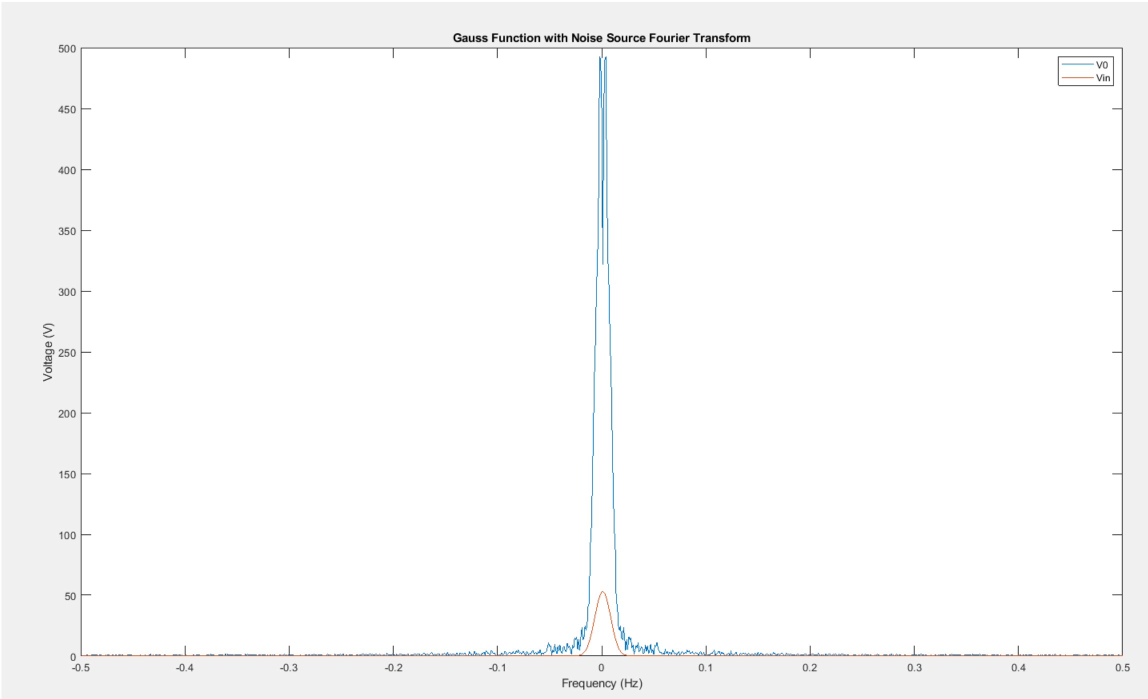

Figure 14: The Fourier transform of the noise plot

3.2.3 Section vi. Varying C_n to see how the bandwidth changes

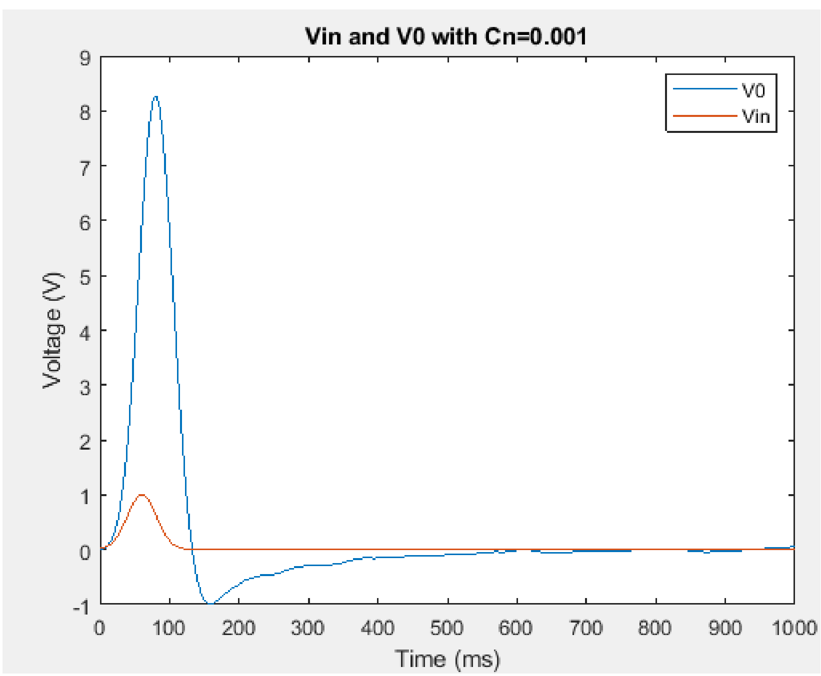

Figure 15: Plot of the output voltage using a capacitor of Cn=0.001

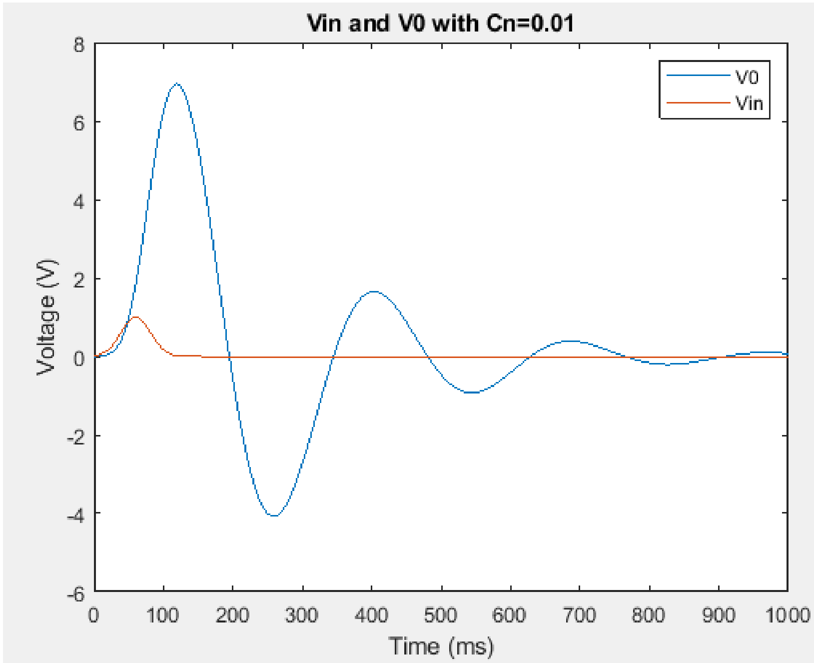

Figure 16: Plot of the output voltage using a capacitor of Cn=0.01

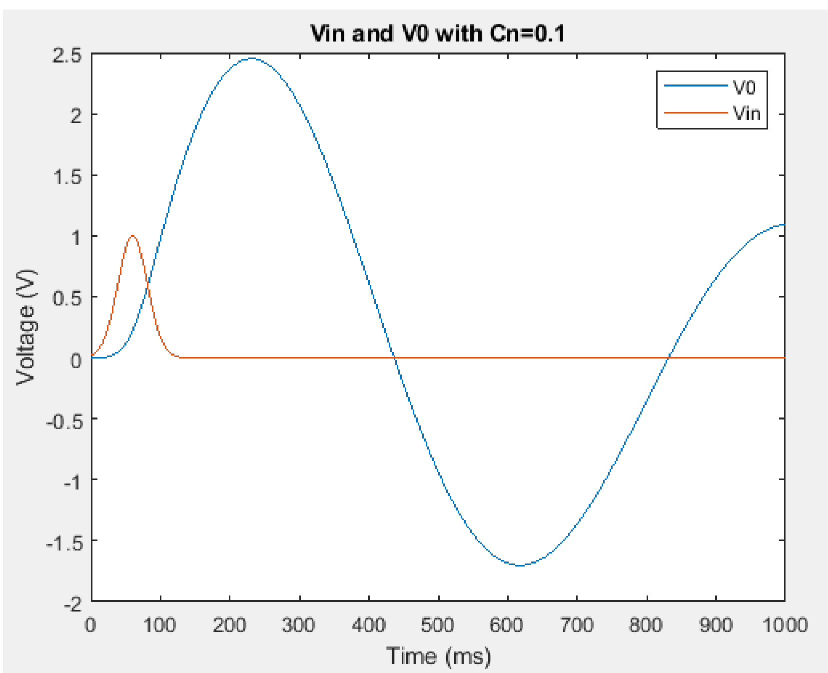

Figure 17: Plot of the output voltage using a capacitor of Cn=0.1

Varying the capacitor seems to widen the bandwidth of the low pass filter to let more of the signal through, the signal becomes even more sinusoidal at higher capacitance.

3.2.4 Section vii. Varying time step

Lowering the time step seems to slow the rise and fall of the signal, increasing the timestep creates a sharper rise and fall in the signal.

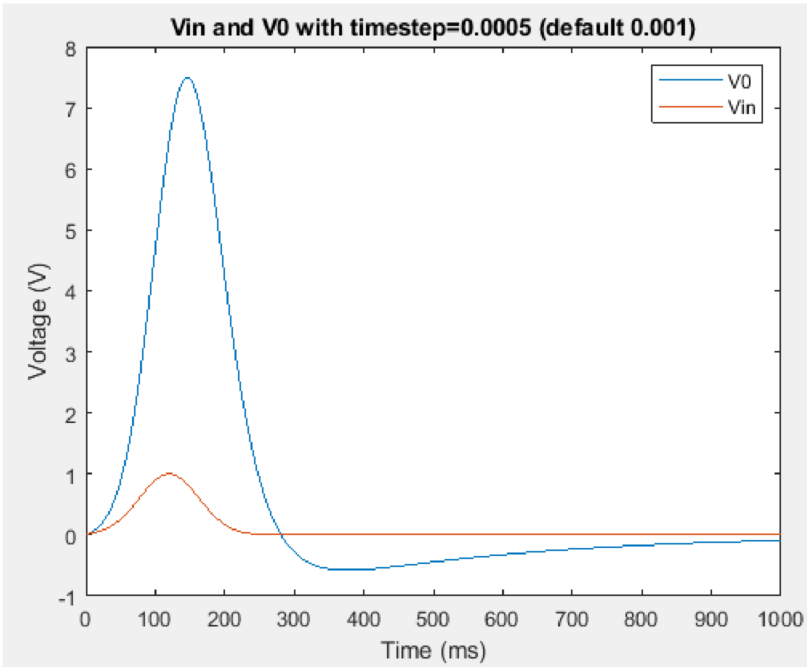

Figure 18: Output voltage with a time step of 0.0005s

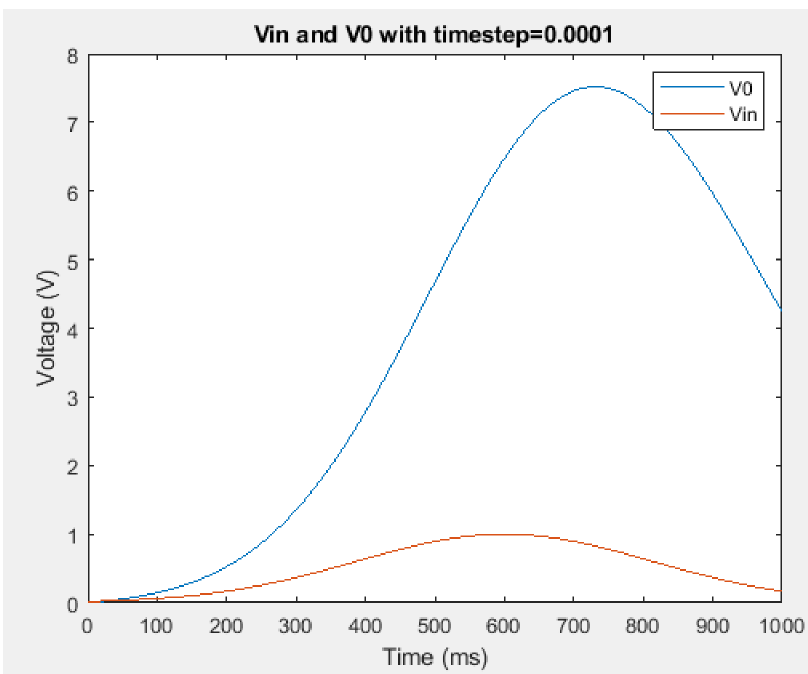

Figure 19: Output voltage with a time step of 0.0001s

4 Part 6: Non-linearity

If the voltage source on the output stage was instead modeled by $V=\alpha I_3+\beta I_3^2+\gamma I_3^3$ we would need to use a non-linear method to solve the output voltage. This would need to be done iteratively using something like the Newton-Raphson method. Additionally we would need a non-linear vector B to describe the non-linear part and the solution would need to be found using a Jacobian.