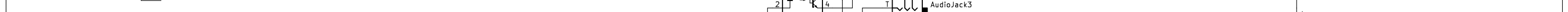


1	2	3	4	5	6	7	8
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1	2	3	4	5	6	7	8
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prevents high VBUS pin leakage current, even though the VIO + 2.5 V specification is not strictly met while GND

the device is not powered.

Power Input

Power Input

Size: A3	Date: 2020-08-24	Rev: A02
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KiCad E.D.A. eeschema (5.1.6)-1	
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	7	8
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[illegible]
