**Analog Filter Board HIGH LEVEL DESIGN(hld)**

**Created by**

**Chandrashekhar V**

|  |  |
| --- | --- |
| **Prepared by** | **Suchitra, Raghunath, Mahesh, Chandrashekhar V** |
| **Reviewed by** | **-** |
| **Approved by** | **-** |
| **Revision** | **V1.0** |
|  | |

**Contents**

[**1** **Introduction:** 3](#_Toc157260692)

[**2** **System Requirement:** 4](#_Toc157260693)

[**3** **Block Diagram** 6](#_Toc157260694)

[**4** **Power Architecture** 7](#_Toc157260695)

[**5** **Power Supply Design** 8](#_Toc157260696)

[**5.1** **Major Power Component Selection** 8](#_Toc157260697)

[**6** **Clock Tree** 9](#_Toc157260698)

[**6.1** **System Clock Generation for system synchronization** 9](#_Toc157260699)

[**6.2** **FPGA Independent CLOCKs:** 10](#_Toc157260700)

[**7** **Backplane Connector** 11](#_Toc157260701)

[**8** **ADC Interface** 13](#_Toc157260702)

[**9** **DAC Interface** 17](#_Toc157260703)

[**10** **DDR4 Memory Interface** 18](#_Toc157260704)

[**11** **Board Dimensions & PCB Specifications** 19](#_Toc157260705)

[**12** **Boot Mode** 22](#_Toc157260706)

[**13** **Environmental Requirement** 23](#_Toc157260707)

[**14** **Appendix A: References** 24](#_Toc157260708)

[**15** **Appendix B: Queries** 25](#_Toc157260709)

# **Introduction:**

This document details the high-level design documentation for Analog Filter Board (P-AFB23). It includes both the electrical and FPGA RTL design development architecture.

# **System Requirement:**

Below are the system requirement table along with the requirement IDs for each.

|  |  |  |
| --- | --- | --- |
| **Req ID** | **Details of Requirement** | **Category** |
| HW\_01 | P-AFB23 Shall host a INTEL CYCLONE V 5CGXFC5C6U19I7N FPGA | System |
| HW\_02 | P-AFB23 shall have one main external interface connector 89007-110LF (Amphenol FCI) 5 X 12 60 Position 2mm, male, straight, press fit. | System |
| HW\_03 | P-AFB23 shall have enough nonvolatile memory to store the coefficients for 4 fir filters with 512 taps | System |
| HW\_04 | P-AFB23 shall have nonvolatile memory to store configuration data for each filter and the ADC. Configuration data will include calibration data, control data, amplifier gain, and sample rate. | System |
| HW\_05 | P-AFB23 shall be capable of up to 512 taps each and are individually programmable | System |
| HW\_06 | P-AFB23 shall have four independent ADC (16 bit), individually programmable Sample rate. | ADC |
| HW\_07 | P-AFB23 shall have 2x DAC outputs, AD7303 DAC's | DAC |
| HW\_08 | P-AFB23 shall have 2x AD7303 DAC's SPI line connected to back plane connector, control interface will be done by back plane. | DAC |
| HW\_09 | P-AFB23 shall have 2x AD7303 DAC's output of DAC must be connected on board test points along with one ground point each. | DAC |
| HW\_10 | P-AFB23 shall have 1x DAC AD5724, 4 channel DAC. | DAC |
| HW\_11 | P-AFB23 shall have 1x DAC AD5724, 4 channel DAC SPI line connected to back plane connector, control interface will be done by back plane. | DAC |
| HW\_12 | P-AFB23 shall have 1x DAC AD5724, 4 channel DAC must be connected on board test points along with one ground point each. | DAC |
| HW\_13 | P-AFB23 shall have separate Analog Ground plane for all DAC outputs | DAC |
| HW\_14 | P-AFB23 shall have ESD Protection for all external interface lines. | ESD |
| HW\_15 | P-AFB23 shall power on with 5V power supply Voltage | Power |
| HW\_16 | P-AFB23 shall have power management control to meet CYCLONE V power supply sequencing.   * Configuration Management (See configuration section) * Command & Telemetry interface * Clock components control. | Power |
| HW\_17 | P-AFB23 shall have reset button, and a reset controller on the board that can reset the processor/ FPGA under the following conditions.   * Undervoltage * Reset switch pressed. * External Reset signal | System |
| HW\_18 | P-AFB23 shall have one on board 100Mhz Oscillator to synchronize all FPGA clocks. | Clock |
| HW\_19 | P-AFB23 shall have OLED interface over SPI, Resolution 128 X 32, 2”. must be driver is capable of driving controllers such as the SH1101A, SH1106, SH1107, SSD1303, and SSD1305 | Display |
| HW\_20 | P-AFB23 shall have on Board Switch with SPDT momentary switch. Red button, SER-RD-AU-OA (C&K Components) | Keypad |
| HW\_21 | P-AFB23 shall have on Board Switch with SPDT momentary switch. Green button, SER-GN-AU-OA (C&K Components) | Keypad |
| HW\_22 | P-AFB23 shall have on Board Switch with SPDT, Rocker Switch, Black, T101-J1-V3-BE (C&K Components) | Keypad |
| HW\_23 | P-AFB23 shall have on Board Switch with Switch, SPST, push button, SMT, KSC442J70SHLFS (C&K Components) | Keypad |
| HW\_24 | P-AFB23 shall have on Board Switch with Rotary dip hex switch, A6R-161RS (Omron Electronics) | Keypad |
| HW\_25 | P-AFB23 shall have Configuration of the Cyclone V FPGA over serial NOR Flash. | Config |
| HW\_26 | P-AFB23 shall have JTAG interface with Cyclone V FPGA. | Config |
| HW\_27 | P-AFB23 shall incorporate a thermistor, placed in the hottest area of the card to monitor board temperature. | Power |
| HW\_28 | P-AFB23 card shall incorporate with test points and LEDs to ease the debugging process. | Bring-up |
| HW\_29 | P-AFB23 card shall not have any Via on pad | PCB |
| HW\_30 | P-AFB23 card BGA breakout shall be made in a “dog bone” fashion | PCB |
| HW\_31 | P-AFB23 card PCB thickness cannot be greater than 2.4mm. | PCB |
| HW\_32 | P-AFB23 shall have the card edges coated with copper and thermal vias be spread around all edges area. | PCB |

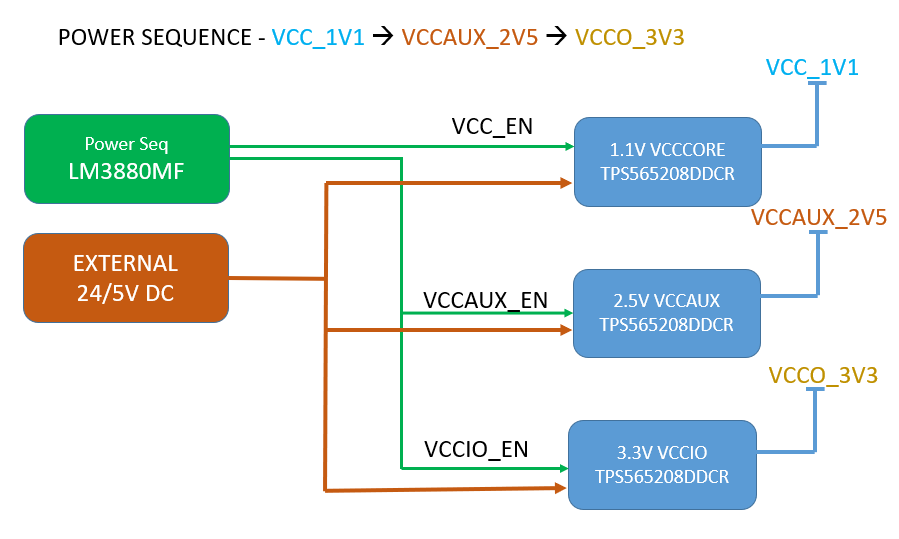
# **Block Diagram**

Below is the P-AFB23 block diagram explaining each interface and its connections,



# **Power Architecture**

Below is the cost-effective Industrial grade solution for P-AFB23. Components are available in stock.



# **Power Supply Design**

# **Major Power Component Selection**

Below are some of the power regulators which are chosen to meet the power requirement of P-AFB23.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **System** | **POWER Supply Name** | **Power Sequence** | **Voltage(V)** | **Power Supply ICs** |
| FPGA | VCC\_1V1 | 1 | 1.1 VOLTS | TPS565208DDCR |
| VCCAUX\_2V5 | 2 | 2.5 VOLTS | TPS565208DDCR |
| VCCO\_3V3 | 2 | 3.3 VOLTS | TPS565208DDCR |

# **Clock Tree**

# **System Clock Generation for system synchronization**

P-AFB23 must have the option to synchronize the external clock of 100Mhz by using on board.

A diagram of a blue square with white text

Description automatically generated

# **FPGA Independent CLOCK TREE:**

# **Backplane Connector**

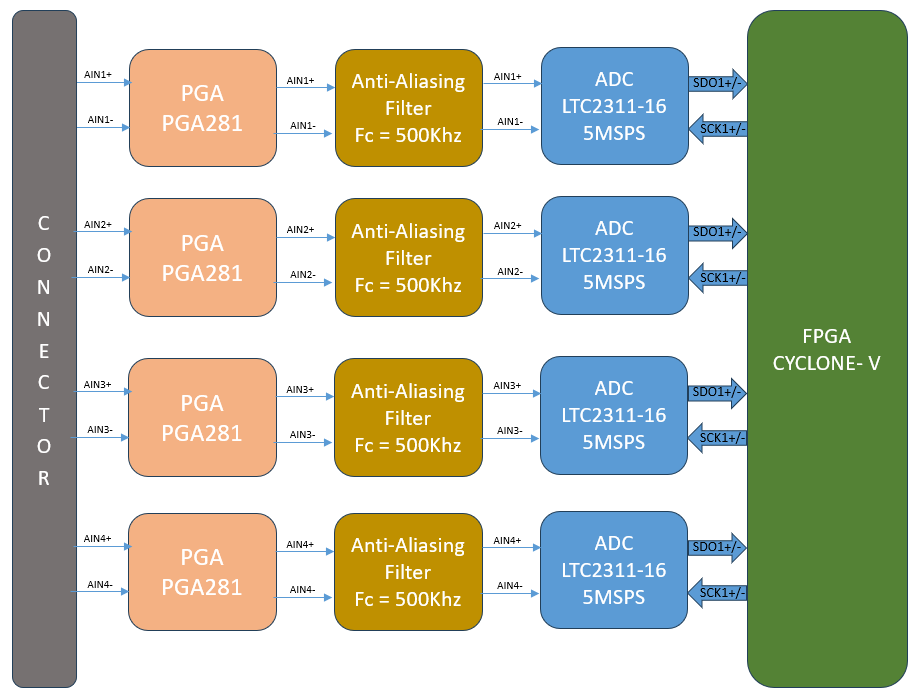
Connector Type:

Following is an interface list for the BACLPLANE Connector:

| Pin No.: | Signal Name | In | Out | Remarks |
| --- | --- | --- | --- | --- |
| ← | → |
| A1 | FRSTP | X |  | Filter Reset, LVDS Pos |
| A2 | FRSTN | X |  | Filter Reset, LVDS Neg |
| A3 | SDIP | X |  | Filter Slave In, LVDS Pos |
| A4 | SDIN | X |  | Filter Slave In, LVDS Neg |
| A5 | SDOP |  | X | Filter Slave Data Out, LVDS Pos |
| A6 | SDON |  | X | Filter Slave Data Out, LVDS Neg |
| A7 | DRDYP |  | X | Filter Data Ready Signal, LVDS Pos |
| A8 | DRDYN |  | X | Filter Data Ready Signal, LVDS Neg |
| A9 | SSP | X |  | Filter Slave Select, LVDS Pos |
| A10 | SSN | X |  | Filter Slave Select, LVDS Neg |
| A11 | CLKP | X |  | Filter Clock Out, LVDS Pos |
| A12 | CLKN | X |  | Filter Clock Out, LVDS Neg |
| B1 | FDAC\_SSn | X |  | Filter DAC Serial Slave Select |
| B2 | FDAC\_SDO |  | X | Filter DAC Serial Out |
| B3 | FDAC\_SDI1 | X |  | Filter DAC Serial Data1 In |
| B4 | FDAC\_SDI2 | X |  | Filter DAC Serial Data2 In |
| B5 | FDAC\_ SCLK |  | X | Filter DAC Serial Clock |
| B6 |  |  |  |  |
| B7 |  |  |  |  |
| B8 |  |  |  |  |
| B9 |  |  |  |  |
| B10 |  |  |  |  |
| B11 |  |  |  |  |
| B12 |  |  |  |  |
| C1 | AGND | X |  | Analog Ground |
| C2 | AGND | X |  | Analog Ground |
| C3 | AGND | X |  | Analog Ground |
| C4 | AGND | X |  | Analog Ground |
| C5 | V0P | X |  | Input DC Voltage Negative |
| C6 | V0P | X |  | Input DC Voltage Negative |
| C7 | V0P | X |  | Input DC Voltage Negative |
| C8 | V0P | X |  | Input DC Voltage Negative |
| C9 | FV5P | X |  | Input Fused 5V Positive |
| C10 | FV5P | X |  | Input Fused 5V Positive |
| C11 | FV5P | X |  | Input Fused 5V Positive |
| C12 | FV5P | X |  | Input Fused 5V Positive |
| D1 | DAC\_SSn | X |  | DAC Serial Slave Select |
| D2 | DAC\_SDO |  | X | DAC Serial Out |
| D3 | DAC\_SDI | X |  | DAC Serial Data In |
| D4 | DAC\_ SCLK | X |  | DAC Serial Clk |
| D5 | DAC\_CLR | X |  | DAC Clear |
| D6 | DAC\_BIN | X |  | DAC BIN/2sCOMP |
| D7 | DAC\_LDAC | X |  | DAC Load DAC |
| D8 |  |  |  |  |
| D9 |  |  |  |  |
| D10 |  |  |  |  |
| D11 |  |  |  |  |
| D12 |  |  |  |  |
| E1 |  |  |  |  |
| E2 |  |  |  |  |
| E3 |  |  |  |  |
| E4 |  |  |  |  |
| E5 |  |  |  |  |
| E6 |  |  |  |  |
| E7 |  |  |  |  |
| E8 |  |  |  |  |
| E9 |  |  |  |  |
| E10 |  |  |  |  |
| E11 |  |  |  |  |
| E12 |  |  |  |  |

# **ANALOG Interface: -**

Below is the block diagram for ADC interface with FPGA,



# **PGA Interface:**

PGA281 is Precision, Zero-Drif, High-Voltage Programmable Gain Instrumentation Amplifier with wide input +/-18V supply, 5uV at Gain =128, Excellent CMRR of 140dB. Below is the block diagram of PGA.

A diagram of a circuit

Description automatically generated

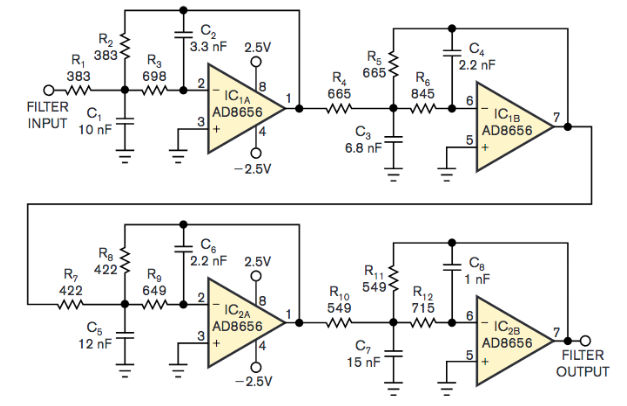
Each Gain control signal will be connected to FPGA IOs to control the gain as listed in the table below.

A table with numbers and symbols

Description automatically generated

# **Anti-Aliasing Filter:**

Below is an example of a 30Khz cut-off frequency anti-aliasing filter. We must design to have 500Khz cutoff frequency antialiasing filter.



# **ADC interface:**

ADC is 16-bit, 5MSPS, 8Vpp differential input with typical 81dB SNR. A 105Mhz external clock must be applied at SCK+/- pin to achieve 5Msps throughput. Below is the interna block diagram of ADC LTC2311-16

A diagram of a computer

Description automatically generated

Below is the data pattern of ADC interface over serial interface,

A diagram of a computer

Description automatically generated

# **DAC Interface**

# **AD5724 Interface**

P-AFB23 must have one AD5724 quad, 12bit, SPI, unipolar/bipolar voltage output interface. The AS5724 can be configured for +5 V, +10 V, +10.8 V, ±5 V, ±10 V, or ±10.8 V outputs through SPI interface connected to backplane. The following signals will be routed out to the backplane connector and a 22 ohm impedance matching resistor will be added as indicated below:

|  |  |  |
| --- | --- | --- |
| DAC\_SSn | DAC Slave Select | Place 22 ohm resistor in series near backplane connector |
| DAC\_SDO | DAC Slave Data Out | Place 22 ohm resistor in series near backplane connector |
| DAC\_SDI | DAC Slave Data In | Place 22 ohm resistor in series near backplane connector |
| DAC\_SCLK | DAC Slave Clock | Place 22 ohm resistor in series near backplane connector |
| DAC\_CLR | DAC Clear | Place 22 ohm resistor in series near backplane connector |
| DAC\_BIN | DAC BIN/2sCOMP | Place 22 ohm resistor in series near backplane connector |
| DAC\_LDAC | DAC Load DAC | Place 22 ohm resistor in series near backplane connector |

# **AD7303 Interface**

P-AFB23 must have two AD7303 DAC's that will be used to view the output data from the filters. The SPI port will be connected to the backplane connector. There will be one White test point terminal, and one black analog ground test point terminal for each FDAC output. The signal and ground test terminal will be side by side and have FDAC1 AGND, FDAC2 AGND.

The two DACs will have the SCLK pins connected in series and will also have the SSn pins connected in series. When routing the SSn and SCLK signals, the route should be in series with no stubs or "T's" in the trace

The following signals will be routed out to the backplane connector and a 22-ohm impedance matching resistor will be added as indicated below:

|  |  |  |
| --- | --- | --- |
| FDAC\_SSn | DAC Slave Select | Place 22 ohm resistor in series near backplane connector |
| FDAC\_SDi1 | DAC Slave Data Out | Place 22 ohm resistor in series near backplane connector |
| FDAC\_SDI2 | DAC Slave Data In | Place 22 ohm resistor in series near backplane connector |
| FDAC\_SCLK | DAC Slave Clock | Place 22 ohm resistor in series near backplane connector |

# **Nonvolatile Memory Interface**

P-AFB23 must have a dedicated non-volatile memory interface with CYCLONE V to store the FR co-efficient, filter control data. A QSPI flash will be interfaced with Cyclone V FPGA to meet this requirement.

A diagram of a computer network

Description automatically generated

P-AFB23 must have a dedicated configuration flash interface to support power on system boot. This configuration flash will be programmed though JTAG interface for PC.

A diagram of a phone

Description automatically generated

# **Display Interface.**

P-AFB23 must have a 128 X 32, 2", OLED display interface over SPI. SPI interface directly connected to backplane connector. The SPI OLED display driver must be SH1101A, SH1106, SH1107, SSD1303 or SSD1305.

# **Switched Interface**

P-AFB23 must have switches interface as listed in below table. The push button and rocker switch will have their NO contact grounded, and their common contact pulled up with a 10K ohm resistor. The hex rotary switches will be wired with their common contact to ground, and their NO contact pulled up with a 10K ohm resistor

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Item | Qty | Körber PN | Vendor | Vendor PN | Description |
| 1 | 1 | 320.862997 | C&K Components | SER-RD-AU-OA | SPDT momentary switch. Red button |
| 2 | 1 | 665.000614 | C&K Components | SER-GN-AU-OA | SPDT push button switch. Green button |
| 3 | 1 | 665.000616 | C&K Components | T101-J1-V3-BE | SPDT, Rocker Switch, Black |
| 4 | 1 | 665.000615 | C&K Components | KSC442J70SHLFS | Switch, SPST, push button, SMT |
| 5 | 2 | 665.000518 | Omron Electronics | A6R-161RS | Rotary dip hex switch |

# **Board Dimensions & PCB Specifications**

* No via in pad.
* BGA breakout shall be made in a "dog bone" fashion.
* PCB thickness: <2.4mm : In case larger thickness is needed, consult with MBT (this case will present a challenge to adhere with requirements 2-3.4 & 2-3.5).
* Aspect ratio: 1:10
* Annular ring: 1mil
* Recommended dielectric material: Isola I-Tera MT40.
* Thermal vias: The card edges shall be coated with copper and thermal vias shall be spread around all edges area.

# **Boot Mode**

# P-AFB23 must have boot mode selectable option to boot from configurable flash as well as boot from external JTAG interface. Corresponding mode selection must be done over DIP switch selection.

# **Environmental Requirement**

P-AFB23 must meet all component selection with respect to Industrial grade.

# **Appendix A: References**

**740-xxxxx Analog Filter Board.docx**

**QF4A512revD6.pdf**

**QFAN001-Interfacing to the QF4A512 Digital SPI port.pdf**

# **Appendix B: Queries**