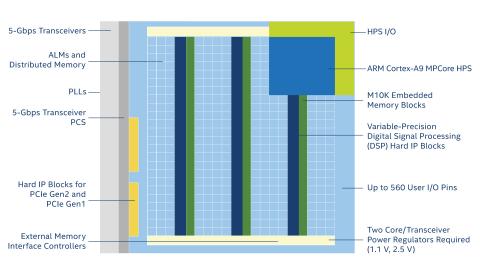
**Cyclone V 5CGXC5 FPGA**

**Architecture**

* Cyclone® V FPGAs continue the Intel® Cyclone® device family tradition of an unprecedented combination of low power, high functionality, and low cost.
* The Cyclone® V FPGA now includes an optional integrated hard processor system (HPS) – consisting of processors, peripherals, and memory controller – with the FPGA fabric using a high-bandwidth interconnect backbone.
* The combination of the HPS with Intel's 28 nm low-power FPGA fabric provide the performance and ecosystem of an applications-class ARM\* processor with the flexibility, low cost, and low power consumption of the Cyclone® V FPGAs.



**Key Features of Cyclone V 5CGXC5 FPGA:**

* Dual-core ARM\* Cortex\*-A9 MPCore\* processor
* Variable-precision DSP blocks
* M10K memory blocks.
* Clock networks and PLLs
* Configuration, design security, and remote system upgrades.
* Single event upset (SEU) mitigation

**Specifications of Cyclone V 5CGXC5 FPGA:**

|  |  |
| --- | --- |
| **Resources** |  |
| Logic Elements (LE) | 77000 |
| Adaptive Logic Modules (ALM) | 116320 |
| Fabric and I/O Phase-Locked Loops (PLLs) | 6 |
| Maximum Embedded Memory | 4.884 Mb |
| Digital Signal Processing (DSP) Blocks | 150 |
| Digital Signal Processing (DSP) Format | Variable Precision |
| External Memory Interfaces (EMIF) | DDR2, DDR3, LPDDR2 |
| Maximum User I/O Count | 336 |
| Maximum Non-Return to Zero (NRZ) Transceivers | 6 |
| Maximum Non-Return to Zero (NRZ) Data Rate | 3.125 Gbps |
| Transceiver Protocol Hard IP | PCIe Gen1 |
| Package Options | M301, M383, U484, F484, F672 |

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