**Name**: Chandra Nikhita M

**Batch**: BRN 39 MS/21-22/5978

# ROUTER RISC V (REPORT)

## Report before rectifying the violation:

Forgot to take ss

```
-----------------------------------------------------------------------------
Product Info
  Name    : VC Static Master Shell
  Version : T-2022.06 -- May 30, 2022

Report Info
  Created : Oct 18, 2023  10:15:59

  TopLevelModule: raven_soc

-----------------------------------------------------------------------------
Management Summary
-----------------------------------------------------------------------------
Stage             Family      Fatals    Errors  Warnings     Infos
-----             --------  --------  --------  --------  --------
LANGUAGE_CHECK    CODING           0         8       606         3
STRUCTURAL_CHECK  CODING           0         3         1        47
-----             --------  --------  --------  --------  --------
Total                              0        11       607        50


-----------------------------------------------------------------------------
Tree Summary
-----------------------------------------------------------------------------
Severity  Stage             Tag                  Count
--------  -----             -------------------  -----
```

# Report after rectifying the violation:

report_cleanlint_riscv.txt (~/VLSI_RN/Verilog_labs/RISCV_SOC_lint) - GVIM@mavenserver-RH2

File Edit Tools Syntax Buffers Window Help

```
--------------------------------------------------------------------------------
Report Summary
--------------------------------------------------------------------------------
Product Info
  Name    : VC Static Master Shell
  Version : T-2022.06 -- May 30, 2022

Report Info
  Created : Oct 25, 2023  18:25:30

  TopLevelModule:

--------------------------------------------------------------------------------
Management Summary
--------------------------------------------------------------------------------
Stage           Family     Fatals    Errors  Warnings    Infos
-----           --------  --------  --------  --------  --------
LANGUAGE_CHECK  CODING           0         1       582         3
-----           --------  --------  --------  --------  --------
Total                            0         1       582         3


--------------------------------------------------------------------------------
Tree Summary
--------------------------------------------------------------------------------
Severity  Stage           Tag                  Count
--------  -----           -------------------  -----
error     LANGUAGE_CHECK  W71                      1
warning   LANGUAGE_CHECK  STARC05-2.1.4.5        14
warning   LANGUAGE_CHECK  STARC05-2.1.5.3         9
warning   LANGUAGE_CHECK  STARC05-2.10.2.3       13
warning   LANGUAGE_CHECK  STARC05-2.11.3.1        5
warning   LANGUAGE_CHECK  STARC05-2.2.3.3       189 *
warning   LANGUAGE_CHECK  W116                     1
warning   LANGUAGE_CHECK  W224                     9
warning   LANGUAGE_CHECK  W240                     3
warning   LANGUAGE_CHECK  W287a                    4
warning   LANGUAGE_CHECK  W287b                   31
warning   LANGUAGE_CHECK  W415a                  258 *
warning   LANGUAGE_CHECK  W486                     1
                                                                    1,0-1         Top
```

report_cleanlint_riscv.txt (~/VLSI_RN/Verilog_labs/RISCV_SOC_lint) - GVIM@mavenserver-RH2

File Edit Tools Syntax Buffers Window Help

```
--------------------------------------------------------------------------------
Severity  Stage           Tag                  Count
--------  -----           -------------------  -----
error     LANGUAGE_CHECK  W71                      1
warning   LANGUAGE_CHECK  STARC05-2.1.4.5        14
warning   LANGUAGE_CHECK  STARC05-2.1.5.3         9
warning   LANGUAGE_CHECK  STARC05-2.10.2.3       13
warning   LANGUAGE_CHECK  STARC05-2.11.3.1        5
warning   LANGUAGE_CHECK  STARC05-2.2.3.3       189 *
warning   LANGUAGE_CHECK  W116                     1
warning   LANGUAGE_CHECK  W224                     9
warning   LANGUAGE_CHECK  W240                     3
warning   LANGUAGE_CHECK  W287a                    4
warning   LANGUAGE_CHECK  W287b                   31
warning   LANGUAGE_CHECK  W415a                  258 *
warning   LANGUAGE_CHECK  W486                     1
warning   LANGUAGE_CHECK  W528                    45
info      LANGUAGE_CHECK  ReportPortInfo-ML        1
info      LANGUAGE_CHECK  W240                     1
info      LANGUAGE_CHECK  W528                     1
--------  -----           -------------------  -----
Total                                            586

* The following detailed reports have been limited to 100 per tag.


--------------------------------------------------------------------------------
W71  (1 error/0 waived)
--------------------------------------------------------------------------------
Tag           : W71
Description   : Case statement does not have a default clause and is not preceded by assignment of target signal [NodeType][Hierarchy: '[HIERARCHY]']
Violation     : Lint:287
Goal          : lint_rtl
Module        : picorv32
FileName      : ./cleanrtl/picorv32.v
LineNumber    : 329
Statement     :     case (mem_wordsize)
NodeType      : in combinational block
HIERARCHY     : :raven_soc:cpu@picorv32

--------------------------------------------------------------------------------
                                                                    61,1          0%
```