# **Assignment 2- Report**

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## **Overview:**

We were asked to implement a MIPS Processor (non-pipelined) using any programming language. We used Python to implement the various features of a MIPS

processor, like control signals, MUX to decide inputs and outputs conditionally, ALU,

Hazard Detection and forwarding unit, and pipeline flush. The program for nonpipelined processors takes machine code, here a sorting algorithm, and executes the

code in 5 phases: Instruction Fetch, Instruction Decode, Execute, Memory and Write Back.

# **Non-Pipelined Processor**

The machine\_code dictionary has the instruction memory address as the key and the

instruction as the value. When the program calls the fetch function it fetches the instructions

from the dictionary one by one and returns it to main. From there the instruction is passed on

to decode phase where the decode function identifies the type of instruction and decodes the

binary instruction into fields like rs, rt, rd, funct, etc. The control unit is also called in the

decode phase which generates control signals according to which the flow of the

Assignment 2- Report

program is

decided. Depending on the control signals, the execute phase performs the various operations

and forwards them to mem and write back phase. The ALU control unit generates ALU

control signal which decides which operation is performed in the ALU. In the mem phase

data is written to memory or extracted from memory which is later written back to the

register file.

The program also prints the number of clock cycles taken to execute all instructions.

### **Assumptions and Limitations:**

The number of inputs and outputs is restricted to 10.

We are initializing the input to specific registers as done in Assignment-1

#### **Result:**

Assignment 2- Report 2

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PS C:\Users\subha\OneDrive - iiit-b\College docs\semester 3\Computer Architecture\ python -u "c:\Users\subha\OneDrive - iiit-b\College docs\semester 3\Computer Architecture\A signment Availagement 2 incomputer Architecture\A signment Availagement 2 incomputer Architecture\A signment availagement 2 incomputer Architecture\A signment 2 incomputer 3 incomputer Architecture\A signment 2 incomputer 3 incomputer Architecture\A signment 2 incomputer 3 incomputer 4 incomputer
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Assignment 2- Report 3