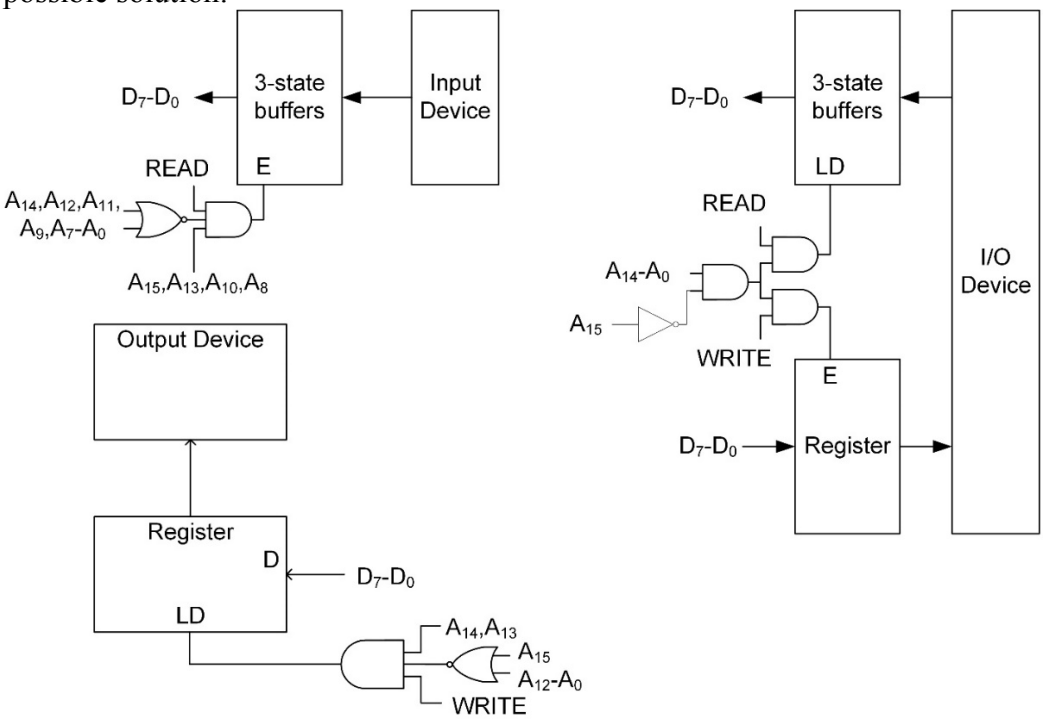
ECE 353-001: Computer Architecture and Organization
Final Exam Solutions
December 19, 2019

1. One possible solution:



2. i) The input to the counter should be IR_1,IR_0,IR_1',IR_1 instead of IR10.
   ii) The input to LD should be **1**, not **2**.
   iii) The input to the OR gate driving the INC input of the counter should not include **12**.
   iv) The input to the OR gate driving the CLR input of the counter should include **8**.

3. (a) Logical address 2571H is not currently in physical memory. It is on Page 2, which has its valid bit set to 0.
   (b) Physical address 2571H is assigned to logical address 3571H.

4.

2. D ← E + F	or	2. D ← E + F
1. A ← B + C		1. A ← B + C
3. C ← D + E		3. C ← D + E
5. E ← D + F		NOP
4. B ← C + F		4. B ← C + F
NOP		5. E ← D + F
6. F ← B + C		6. F ← B + C

5.

Field 1	µop	Field 2	µop	Field 3	µop
000	NOP	00	NOP	00	NOP
001	**D**	01	**I**	01	**H**
010	**F**	10	**C**	10	**E**
011	**B**	11	**A**	11	**G**