<Expt. No. 4 - Design CMOS amplifier and obtain a gain equal to the last 2 digit of roll number	
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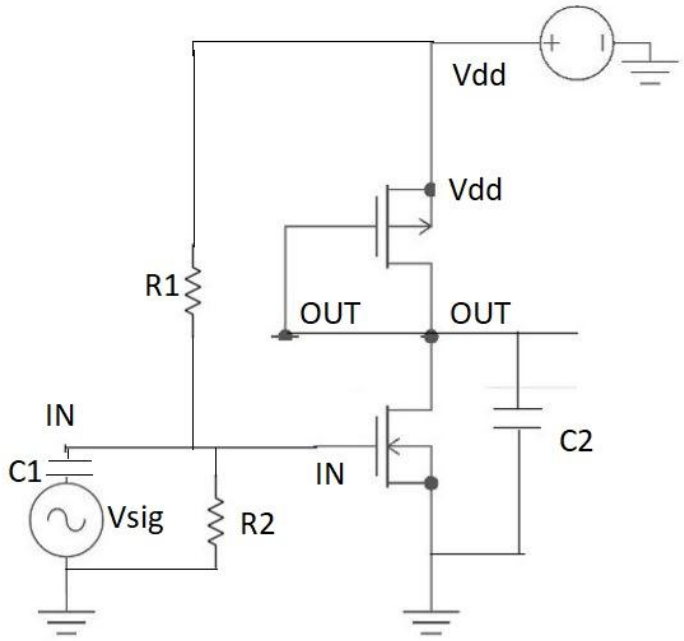
ROLL No.: CB.EN.P2VLD21016	**Marks : out of 10**

AIM:

To Design and obtain a CMOS amplifier (choose configuration on your own), the amplifier should deliver a gain equal to the last 2 digits of your roll number. With and without capacitive loads to be analyzed

BLOCK/CIRCUIT DIAGRAM:



CODE:

CMOS Amplifier with capacitive load:

*AC analysis HSPICE example

.MODEL PCH PMOS LEVEL=54

.MODEL NCH NMOS LEVEL=54

M2 OUT IN VDD VDD PCH W=560n L=600n

M1 OUT IN 0 0 NCH W=250n L=570n

C1 VSIG IN 1u

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CL OUT 0 10p

R1 VDD IN 6k
R2 IN 0 6k

VDC VDD 0 DC 1.5
VAC VSIG 0 AC 0.01
.AC DEC 5 0.001 2000MEG
.PRINT AC V(OUT)
.OPTIONS LIST NODE POST
.END
```

CMOS Amplifier without capacitive load:

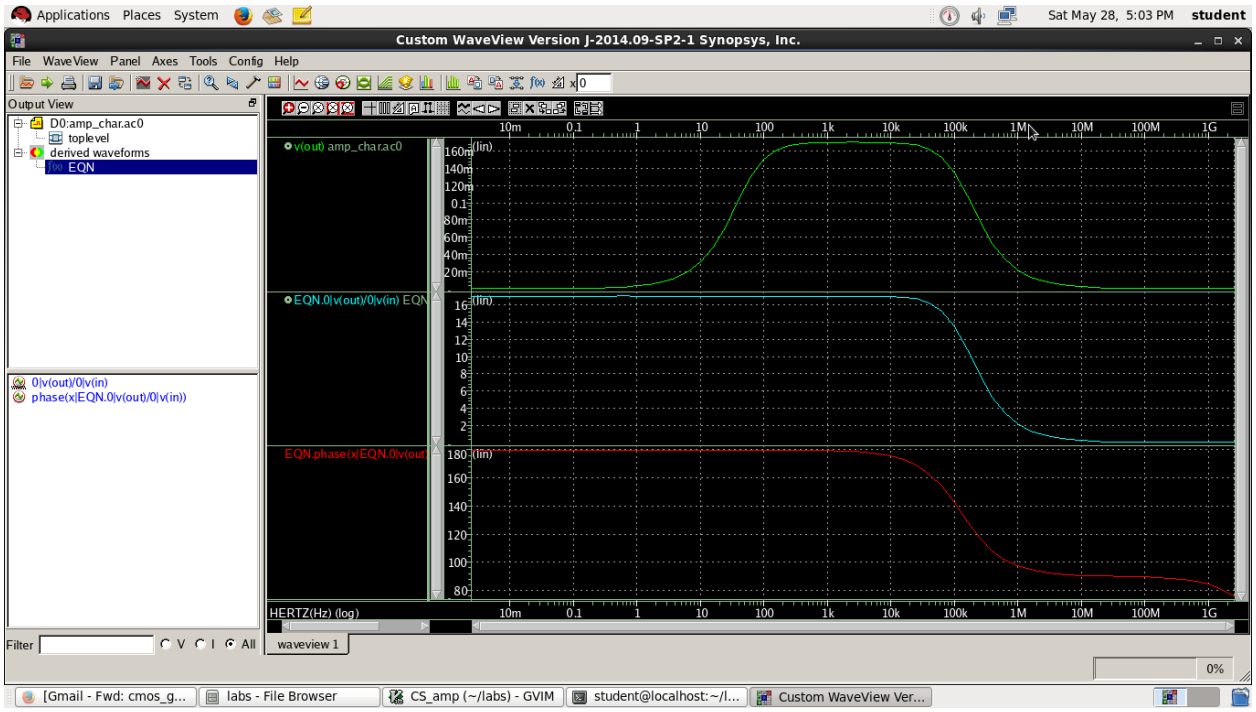
```
*AC analysis HSPICE example
.MODEL PCH PMOS LEVEL=54
.MODEL NCH NMOS LEVEL=54
M2 OUT IN VDD VDD PCH W=560n L=600n
M1 OUT IN 0 0 NCH W=250n L=570n

C1 VSIG IN 1u
R1 VDD IN 6k
R2 IN 0 6k

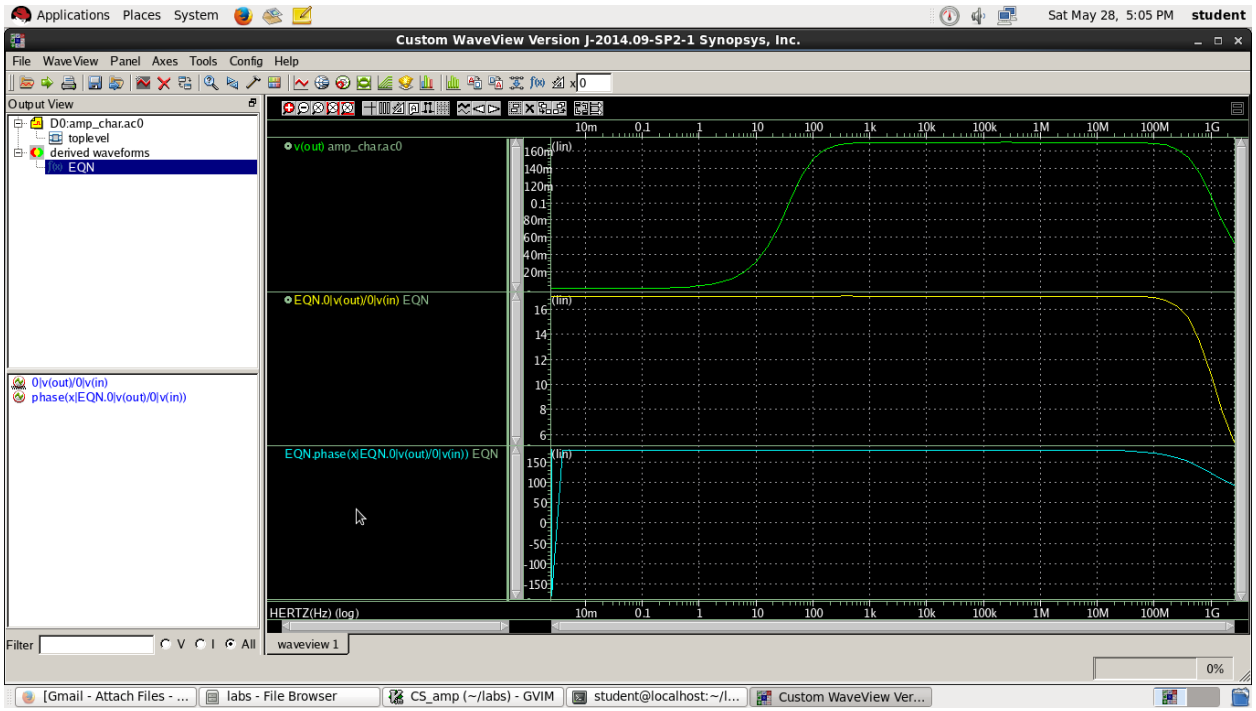
VDC VDD 0 DC 1.5
VAC VSIG 0 AC 0.01
.AC DEC 5 0.001 2000MEG
.PRINT AC V(OUT)
.OPTIONS LIST NODE POST
.END
```

OUTPUT:

CMOS Amplifier with capacitive load:



CMOS Amplifier without capacitive load:



INFERENCE:

With this experiment, we were able to obtain the gain of CMOS amplifier using HSpice tool. Here are a few things I learned from this experiment:

- Using the HSpice tool, analyzed the CMOS amplifier and obtained the gain of 16V/V.
- Manually wrote the netlist for the devices (so the schematic is not needed) in order to realize the circuit.
- Gain of the amplifier is varying by changing the W/L ratio, as the W/L ratio of NMOS increases to get the higher gain.
- Manually written the netlist for the devices, so schematic is not required
- Since node names were assigned, connections can be easily monitored
- Analyzed the output characteristics of the CMOS inverter device with three different W and L values keeping the W/L ratio as 2.5 for all W, L values respectively