<Expt. No. 2a- NAND/NOR Characteristics using HSPICE	
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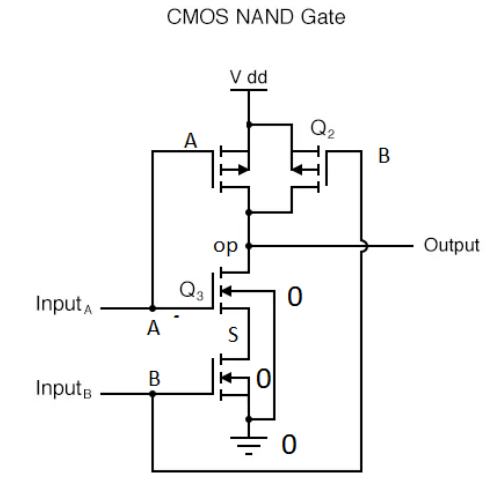
ROLL No.: CB.EN.P2VLD21016	**Marks : out of 10**

AIM:

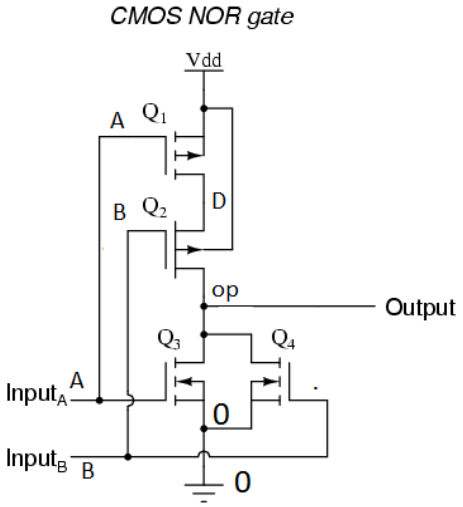
To Obtain the CMOS NAND/NOR characteristics for three different aspect ratios and compare the characteristics using HSPICE

BLOCK/CIRCUIT DIAGRAM:

NAND Gate:



NOR Gate:



CODE:

NAND Gate:

```
*NAND gate
.MODEL PCH PMOS LEVEL=54
.MODEL NCH NMOS LEVEL=54
MPA op A DD DD PCH L=L W=W
MPB op B DD DD PCH L=L W=W
MNA op A S S NCH L=L W=W
MNB S B 0 0 NCH L=L W=W
vdd DD 0 3
va A 0 3
vb b 0 2
.DC vb 0 3 0.1 SWEEP DATA=d1
.DATA d1
L        W
90n      225n
100n     250n
120n     280n
.ENDDATA
.plot DC V(va) V(vb) V(op)
.option post
.end
```

NOR Gate:

```
*NOR gate
.MODEL PCH PMOS LEVEL=54
.MODEL NCH NMOS LEVEL=54
MPA D A DD DD PCH L=L W=W
MPB op B DD DD PCH L=L W=W
MNA op A 0 0 NCH L=L W=W
```

MNB op B 0 0 NCH L=L W=W

vdd DD 0 3

va A 0 0

vb b 0 2

.DC vb 0 3 0.01 SWEEP DATA=d1

.DATA d1

L	W
90n	225n
100n	250n
120n	280n

.ENDDATA

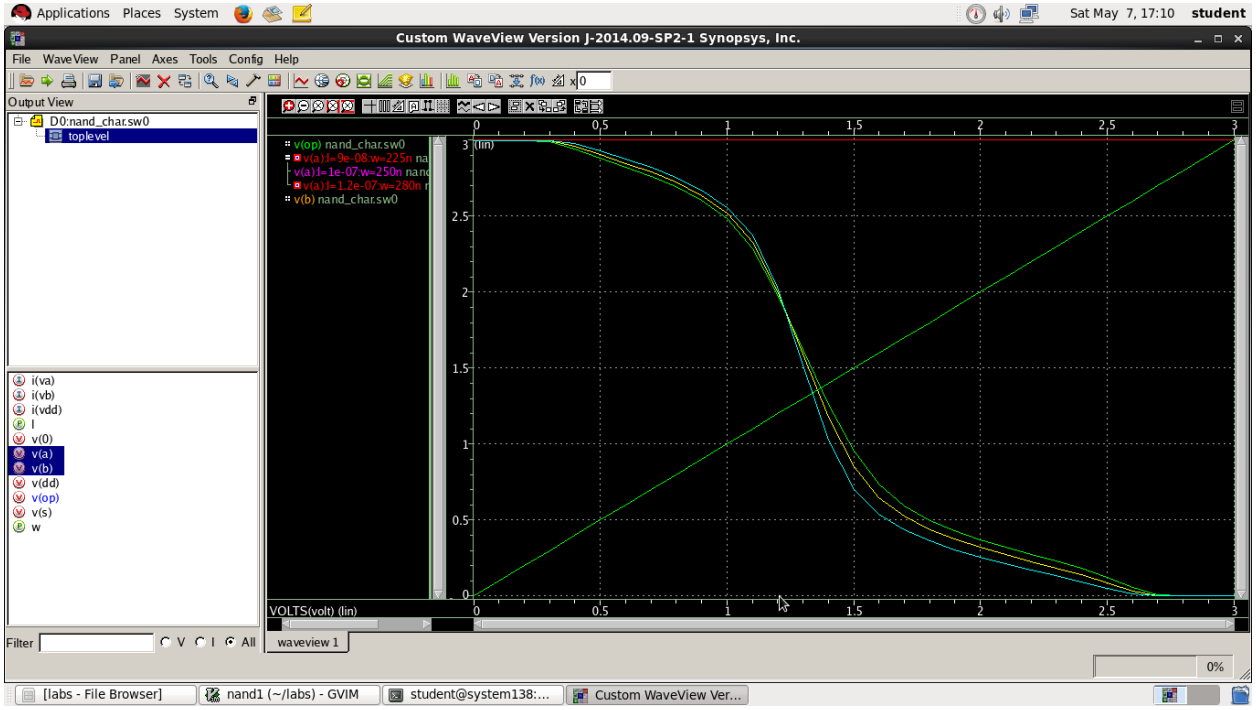
.plot DC V(A) V(B) V(op)

.option post

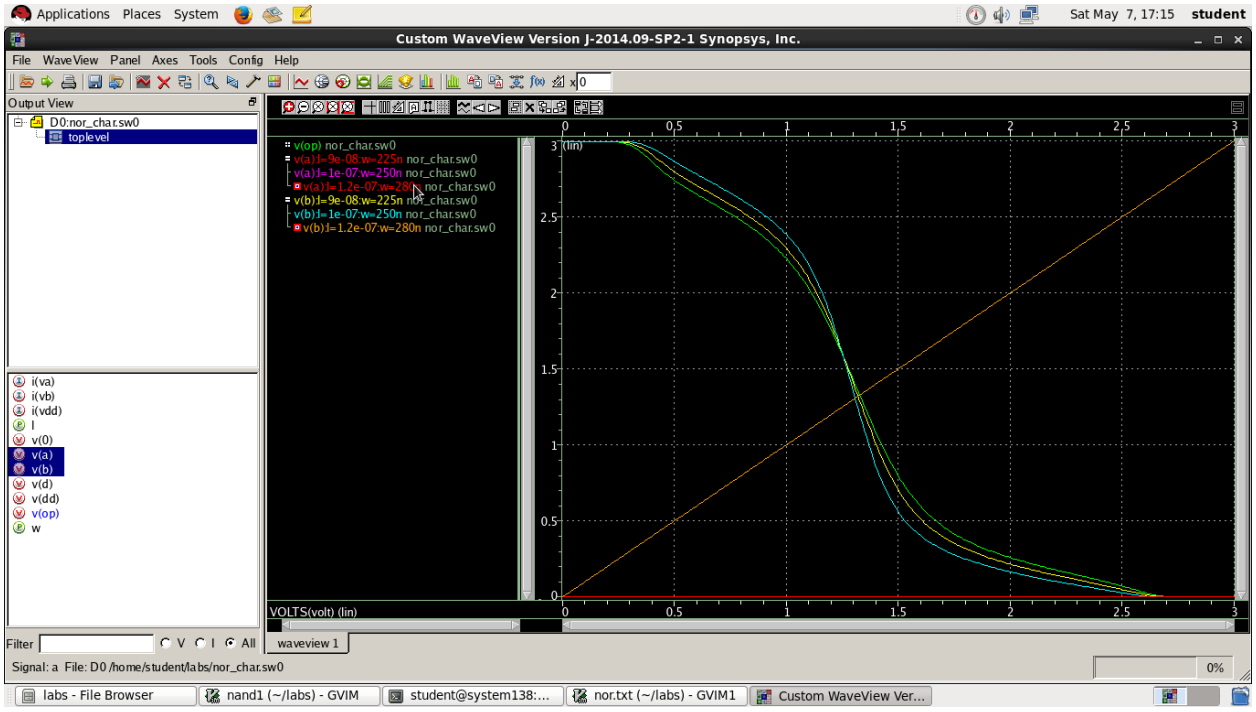
.end

OUTPUT:

NAND Gate:



NOR Gate:



INFERENCE:

- Analyzed the NAND and NOR characteristics implemented using CMOS using HSPICE tool
- Modeled the devices only by designing netlist for the operation
- Assigned node names for the MOSFET devices and provided input and analyzed the output
- Manually written the netlist for the devices, so schematic is not required
- Since node names were assigned, connections can be easily monitored
- Transistor sizing is provided based on the series and parallel connections of MOSFETs
- Analyzed the output characteristics of NAND and NOR with three different aspect ratios