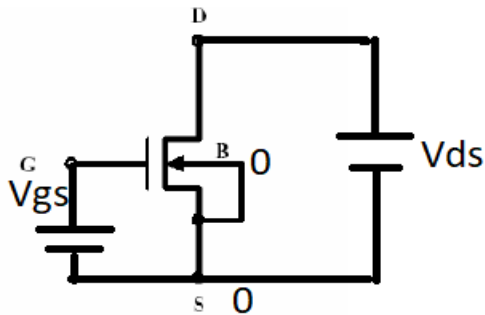
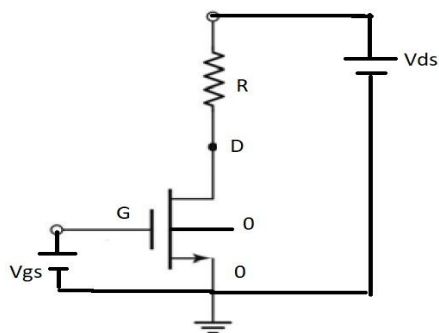


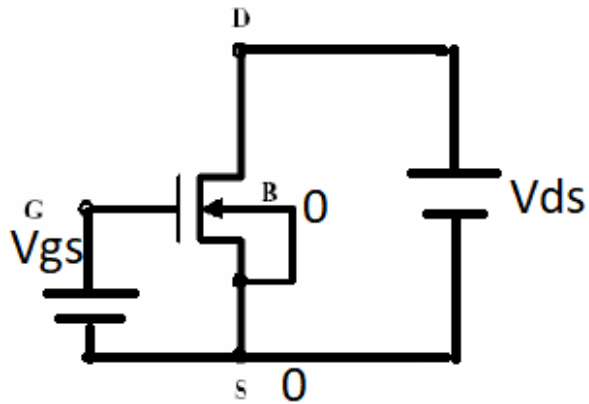
Expt. No. 3 - NMOS, PMOS Characteristics using HSpice		
NAME :	S. Chandra Moulee	Date : 07/05/2022
ROLL No.:	CB.EN.P2VLD21016	Marks : out of 10

AIM:

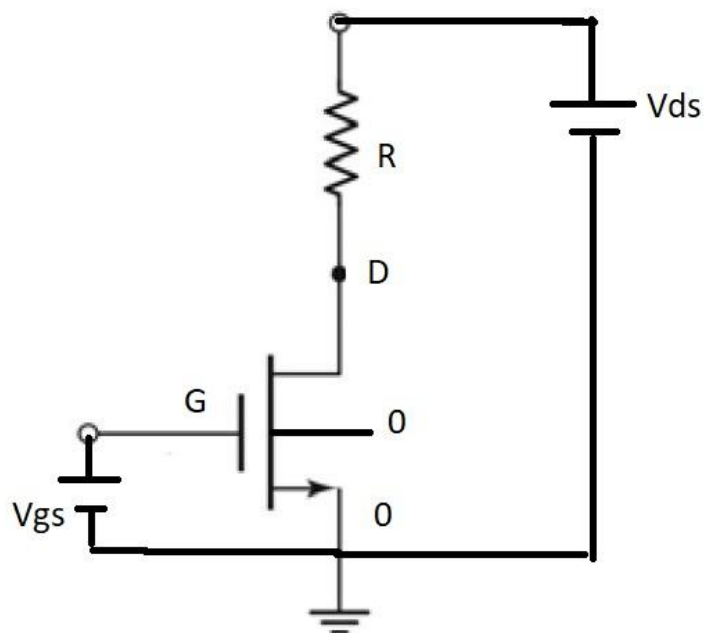
To Perform AC and DC analysis for an enhancement type n channel and p channel MOSFET for different gate, drain and substrate potential, with and without resistive or capacitive loads to be analyzed and find transconductance and V_{th}

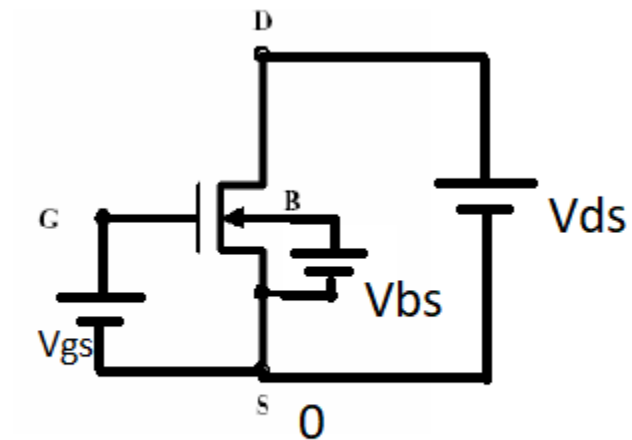
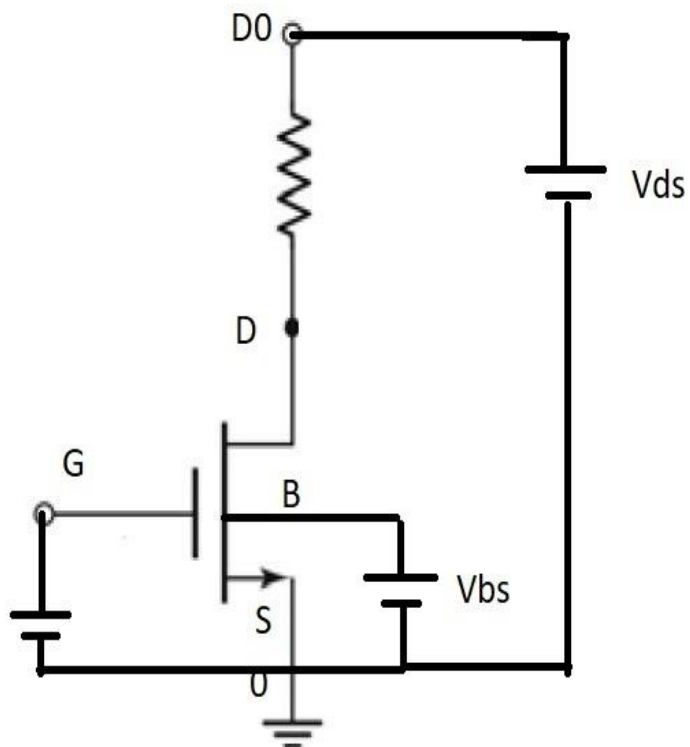
BLOCK/CIRCUIT DIAGRAM:**NMOS V_{ds} :****NMOS V_{ds} with Resistance:**

NMOS V_{gs} :

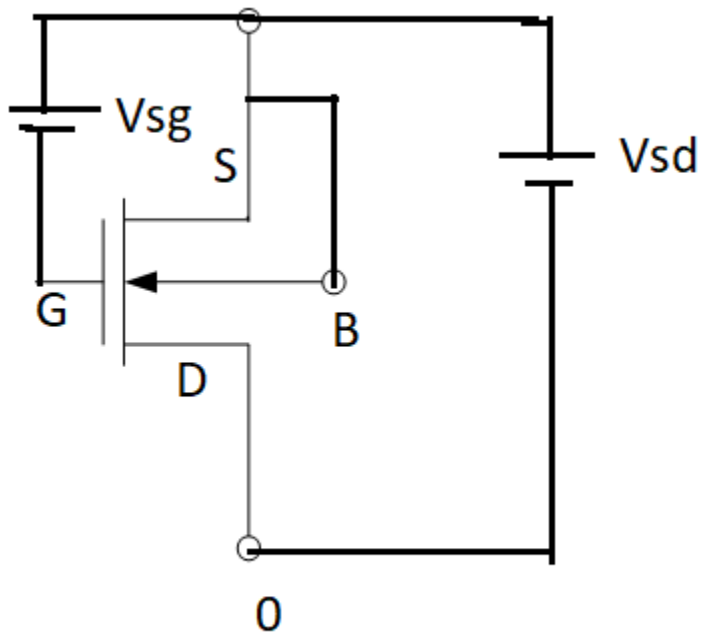


NMOS V_{gs} with resistance:

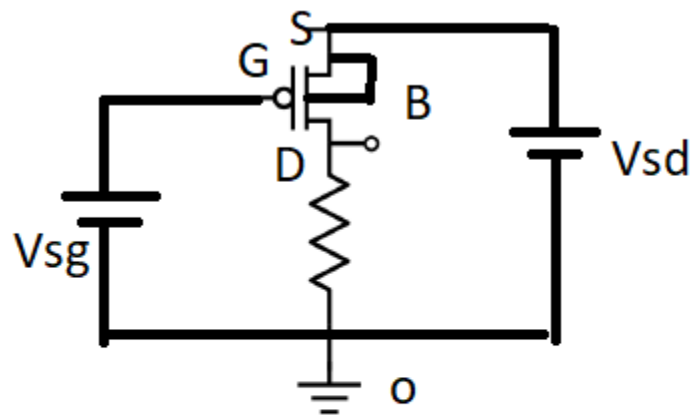


NMOS Vbs:**NMOS Vbs with resistance:**

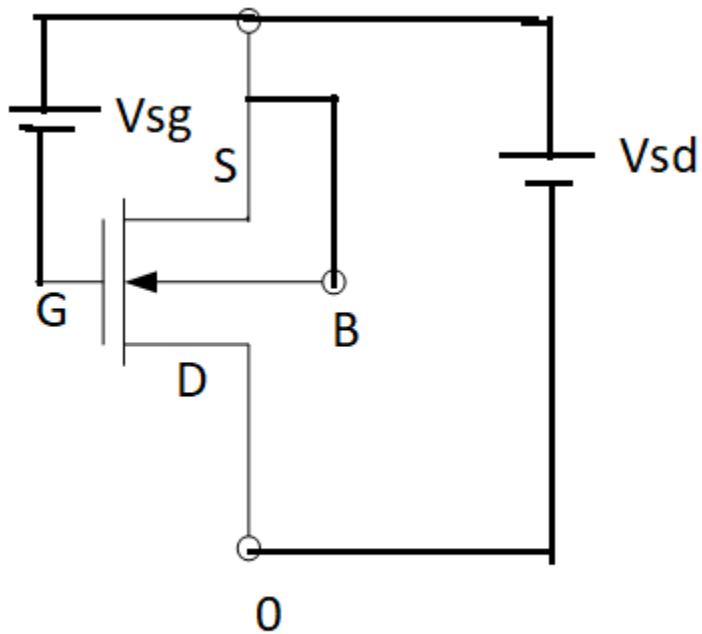
PMOS Vsd:



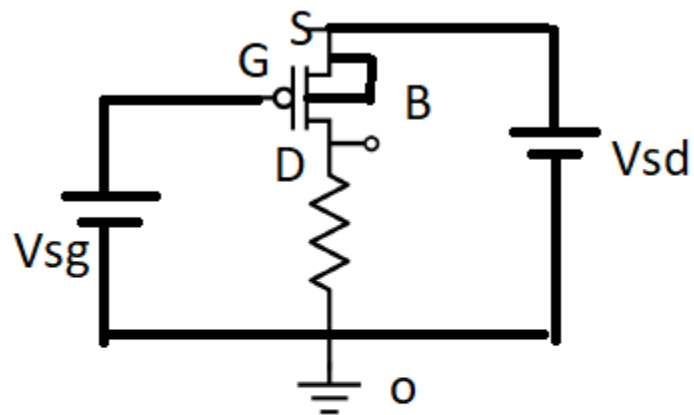
PMOS Vsd with resistance:

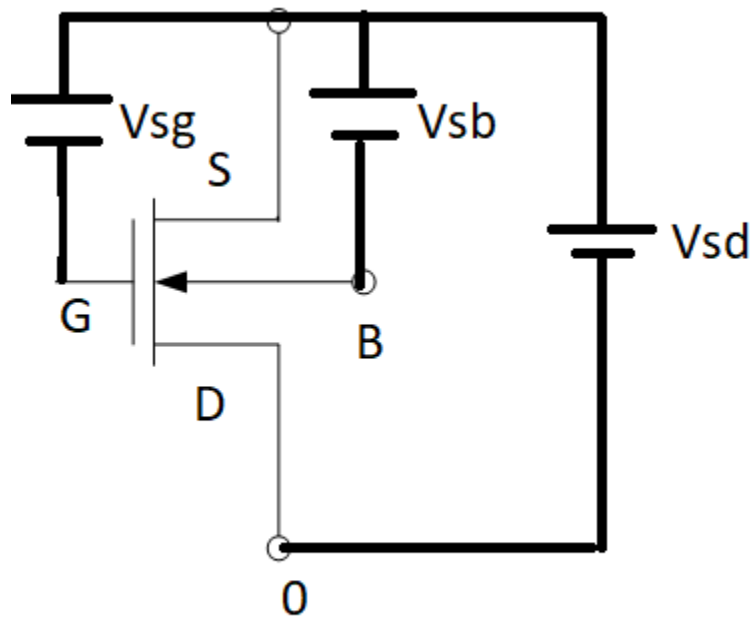
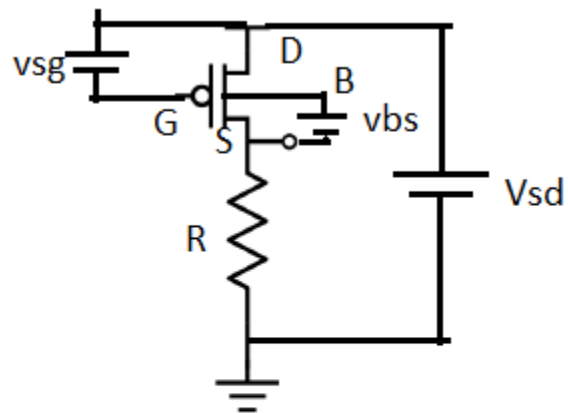


PMOS V_{sg} :



PMOS V_{sg} with resistance:



PMOS Vbs:**PMOS Vbs with resistance:**

CODE:**NMOS Vds:**

```
*NMOS CHARACTERISTICS
.MODEL NCH NMOS LEVEL=54
M1 d g 0 0 NCH L=90n W=170n
vds d 0 dc 3
vgs g 0 dc 2
*.PARAM L=60n
.DC vds 0 3 0.01 SWEEP vgs 0 5 1
.ENDDATA
.plot DC IX4(M1)
.option post
.end
```

NMOS Vds with Resistance:

```
*NMOS CHARACTERISTICS
.MODEL NCH NMOS LEVEL=54
M1 d g 0 0 NCH L=90n W=170n
R d0 d 100
vds d0 0 dc 4
vgs g 0 dc 2
*.PARAM L=60n
.DC vds 0 5 0.01 SWEEP vgs 0 5 1
.ENDDATA
.plot DC IX4(M1)
.option post
.end
```

NMOS Vgs:

*NMOS CHARACTERISTICS

.MODEL NCH NMOS LEVEL=54

M1 d g 0 0 NCH L=90n W=225n

vds d 0 dc 3

vgs g 0 dc 0

*.PARAM L=60n

.DC vgs 0 3 0.01

.ENDDATA

.plot DC IX4(M1)

.option post

.end

NMOS Vgs with resistance:

*NMOS CHARACTERISTICS

.MODEL NCH NMOS LEVEL=54

M1 d g 0 0 NCH L=90n W=225n

R d0 d 1K

vds d0 0 dc 3

vgs g 0 dc 0

*.PARAM L=60n

.DC vgs 0 3 0.01

.ENDDATA

.plot DC IX4(M1)

.option post

.end

NMOS Vbs:

*NMOS CHARACTERISTICS

.MODEL NCH NMOS LEVEL=54

M1 d g 0 s NCH L=90n W=170n

vds d 0 dc 3

vgs g 0 dc 0

vbs s 0 dc 0

*.PARAM L=60n

.DC vbs 0 -3 -0.01

.ENDDATA

.plot DC IX4(M1)

.option post

.end

NMOS Vbs with resistance:

*NMOS CHARACTERISTICS

.MODEL NCH NMOS LEVEL=54

M1 d g 0 s NCH L=90n W=170n

R d0 d 10K

vds d0 0 dc 3

vgs g 0 dc 0

vbs s 0 dc 0

*.PARAM L=60n

.DC vbs 0 -3 -0.01

.ENDDATA

.plot DC IX4(M1)

.option post

.end

PMOS Vsd:

*PMOS VDD sweep

.MODEL PCH PMOS LEVEL=54

M1 0 g s s PCH L=90n W=225n

vsd s 0 DC 3

vsg s g DC 3

.DC vsd 0 3 0.01 SWEEP vsg 0 5 1

.plot DC lx4(M1)

.option post

.end

PMOS Vsd with resistance:

*PMOS VDD sweep

.MODEL PCH PMOS LEVEL=54

M1 0 g s s PCH L=90n W=225n

R s0 s 1K

vsd s0 0 DC 3

vsg s g DC 3

.DC vsd 0 3 0.01 SWEEP vsg 0 5 1

.plot DC lx4(M1)

.option post

.end

PMOS Vsg:

*PMOS VDD sweep

.MODEL PCH PMOS LEVEL=54

M1 0 g s s PCH L=90n W=235n

vsd s 0 DC 3

```
vsg s g DC 3
```

```
.DC vsg 0 3 0.01
```

```
.plot DC lx4(M1)
```

```
.option post
```

```
.end
```

PMOS Vsg with resistance:

```
*PMOS VDD sweep
```

```
.MODEL PCH PMOS LEVEL=54
```

```
M1 0 g s s PCH L=90n W=225n
```

```
R s0 s 1K
```

```
vsd s0 0 DC 5
```

```
vsg s g DC 3
```

```
.DC vsg 0 -5 -0.01
```

```
.plot DC lx4(M1)
```

```
.option post
```

```
.end
```

PMOS Vbs:

```
*PMOS VDD sweep
```

```
.MODEL PCH PMOS LEVEL=54
```

```
M1 0 g s b PCH L=90n W=225n
```

```
vsd s 0 DC 3
```

```
vsg s g DC 3
```

```
vsb s b DC 3
```

```
.DC vsb 0 -3 -0.01
```

```
.plot DC lx4(M1)
```

```
.option post
.end
```

PMOS Vbs with resistance:

*PMOS VDD sweep

```
.MODEL PCH PMOS LEVEL=54
```

```
M1 d g s b PCH L=90n W=190n
```

```
R d 0 1K
```

```
vds s d DC 3
```

```
vsg s g DC 3
```

```
vsb s b DC 3
```

```
.DC vsb 0 -5 -0.01
```

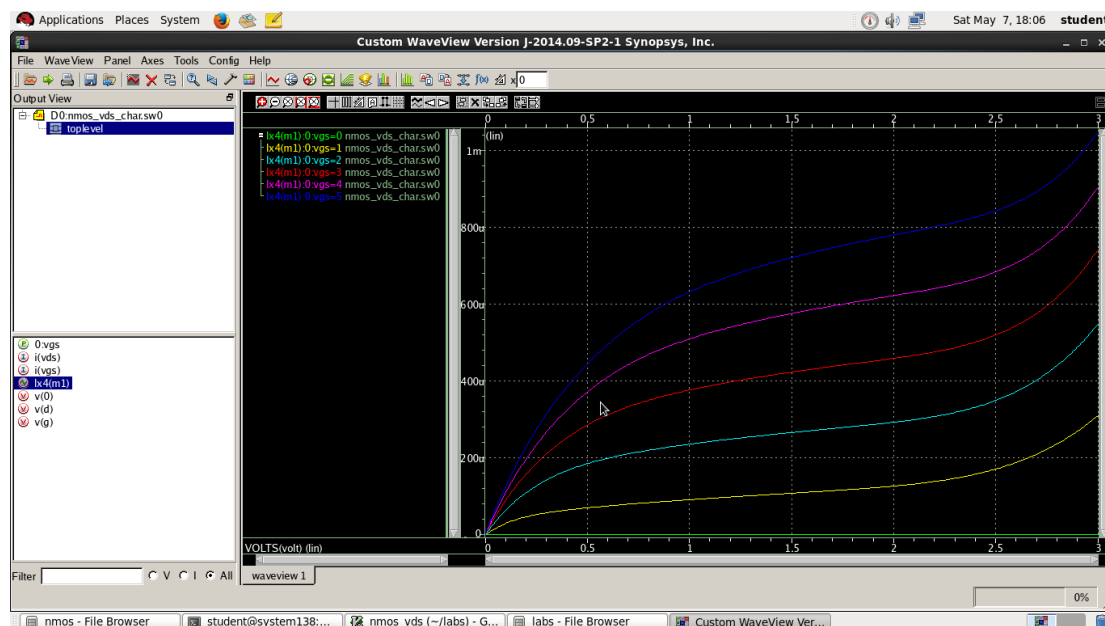
```
.plot DC lx4(M1)
```

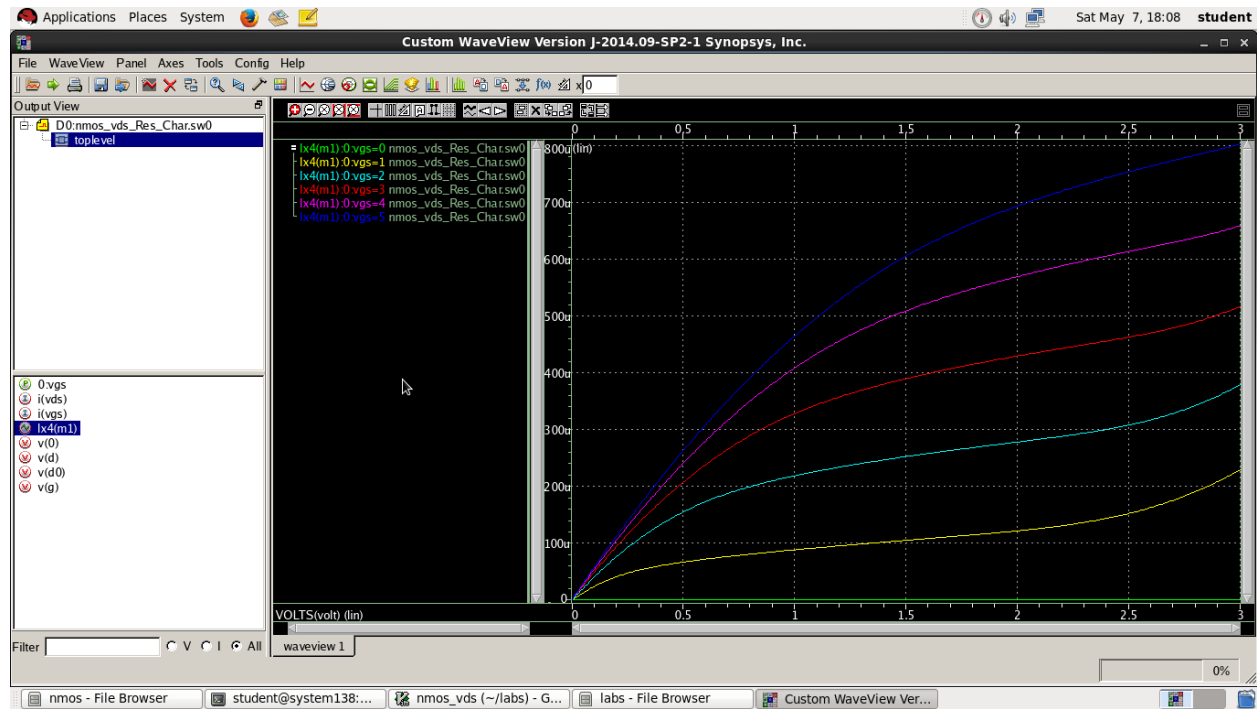
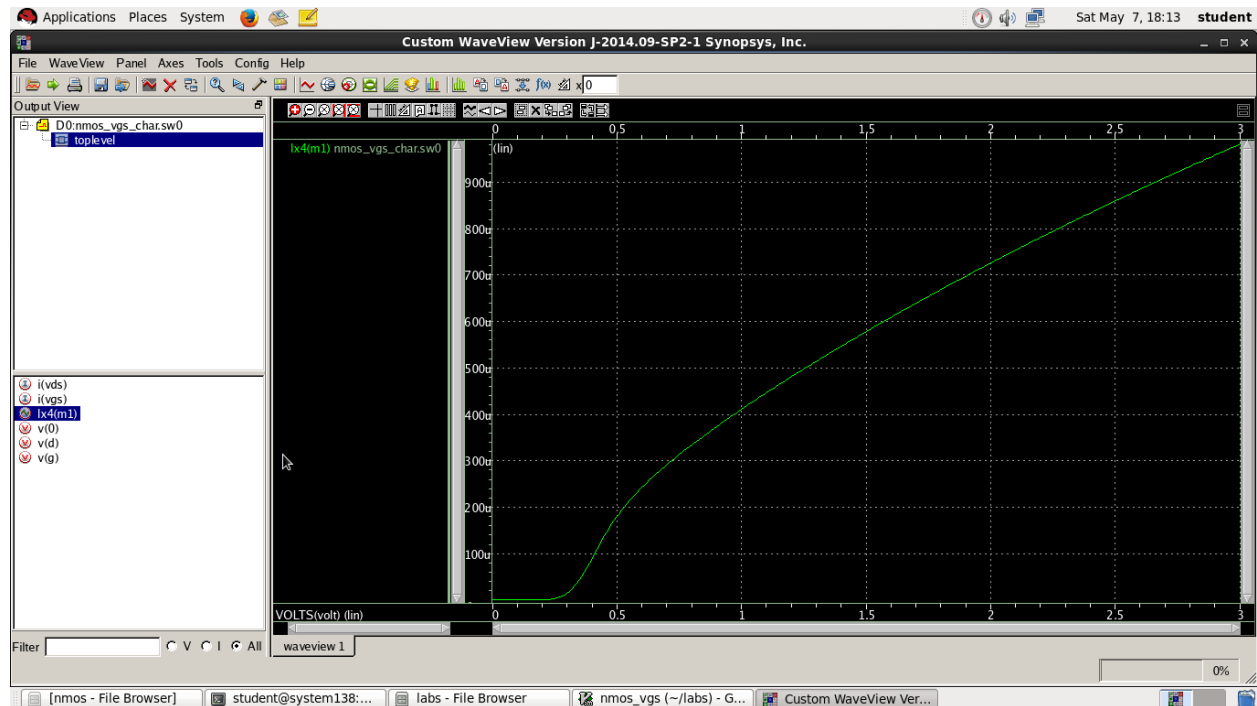
```
.option post
```

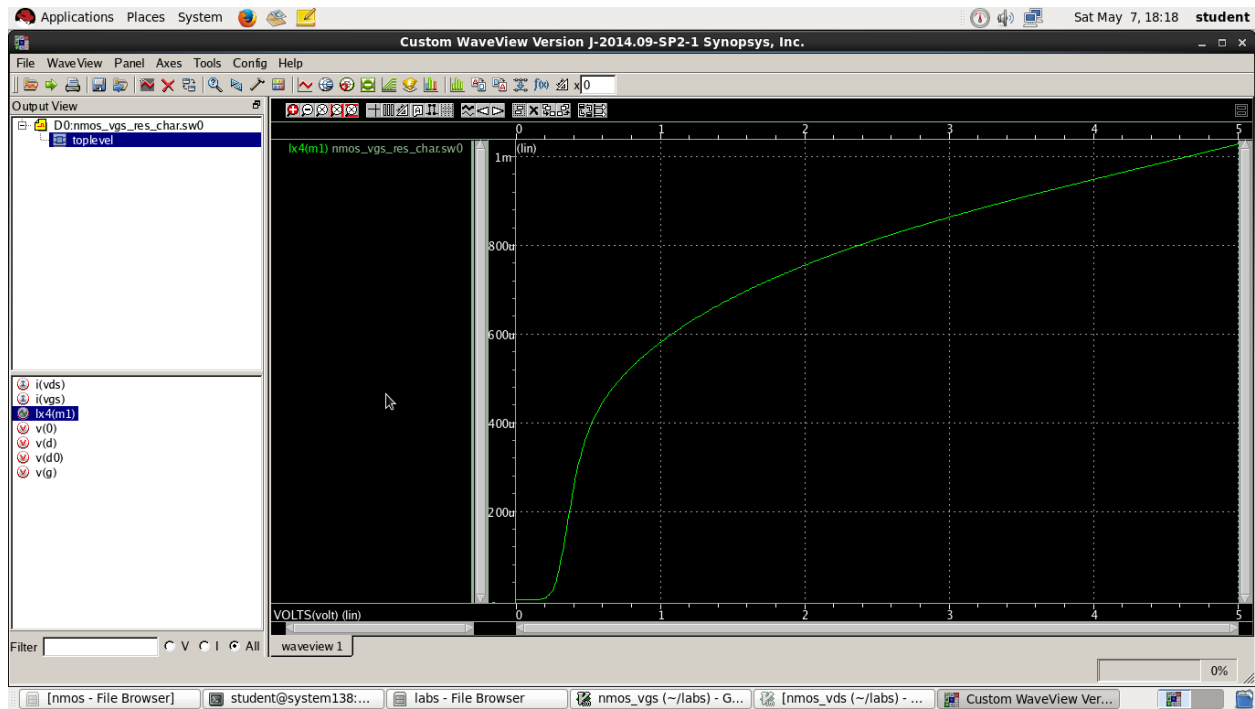
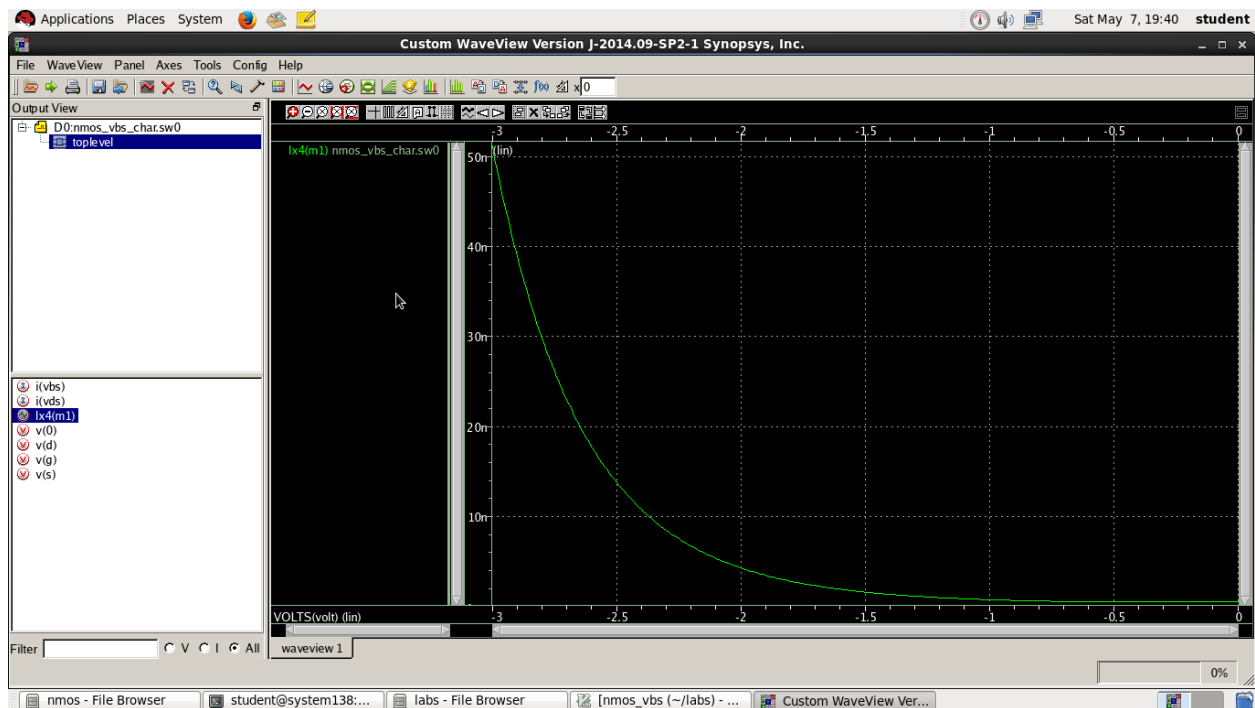
```
.end
```

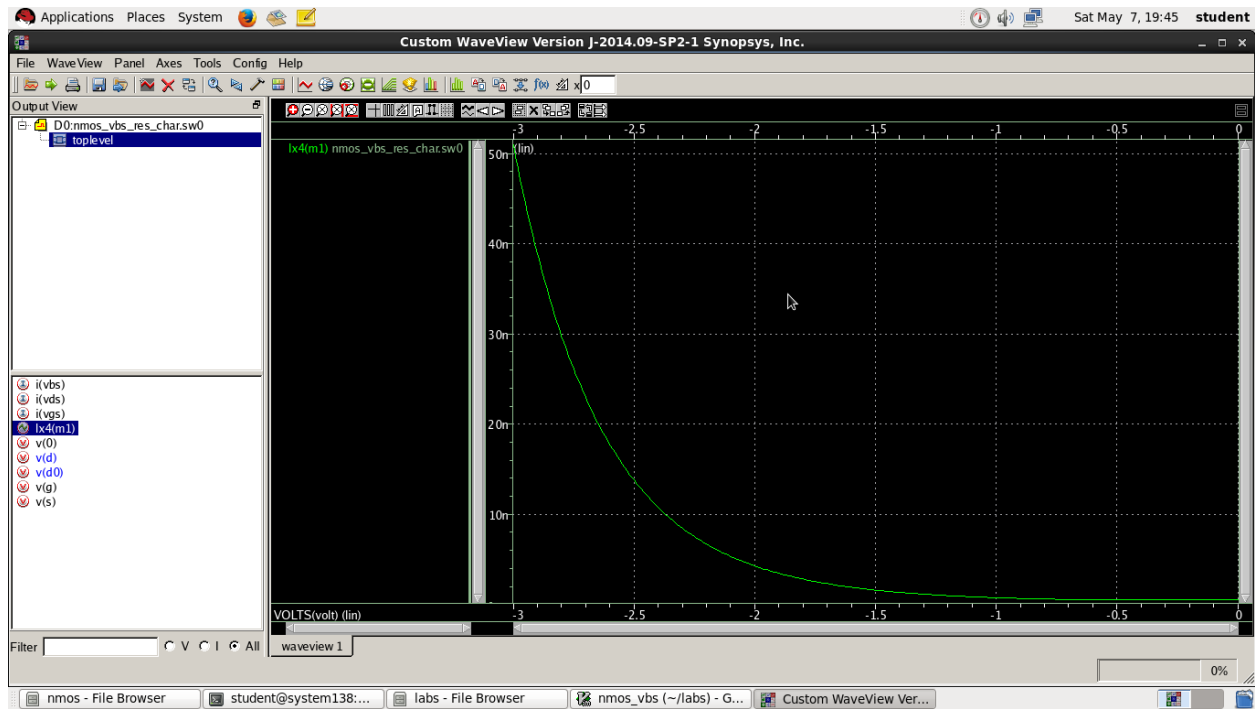
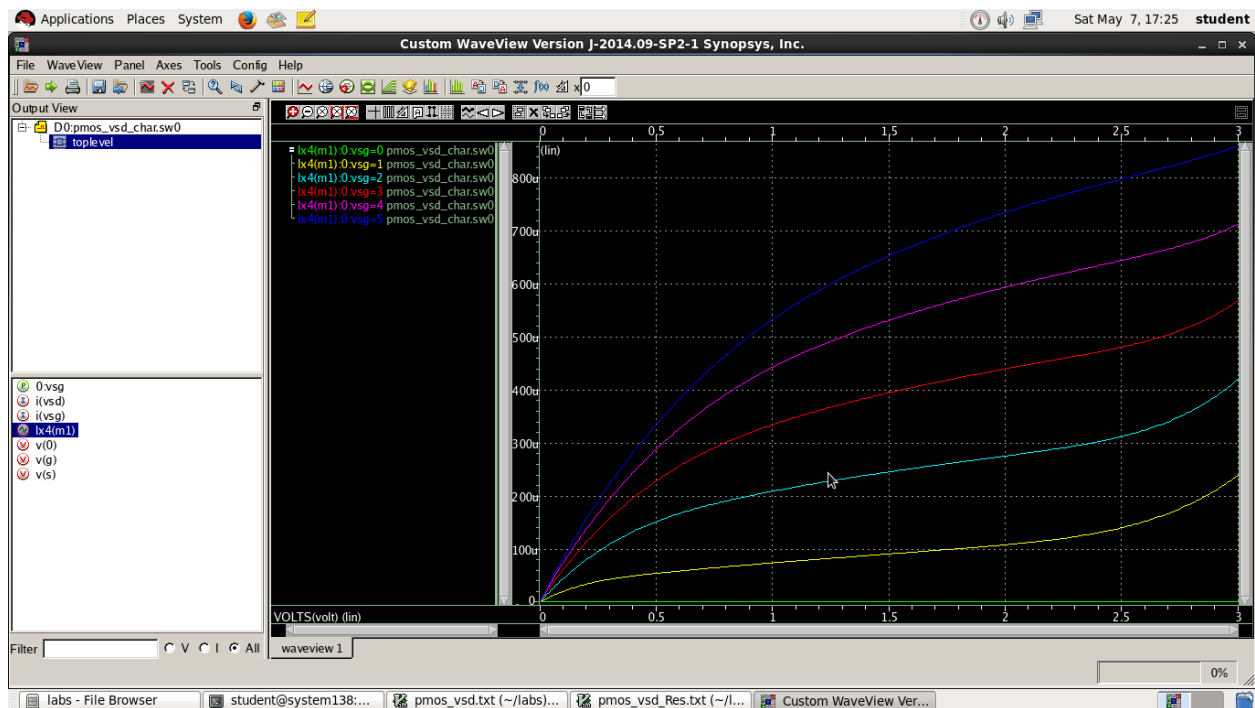
OUTPUT:

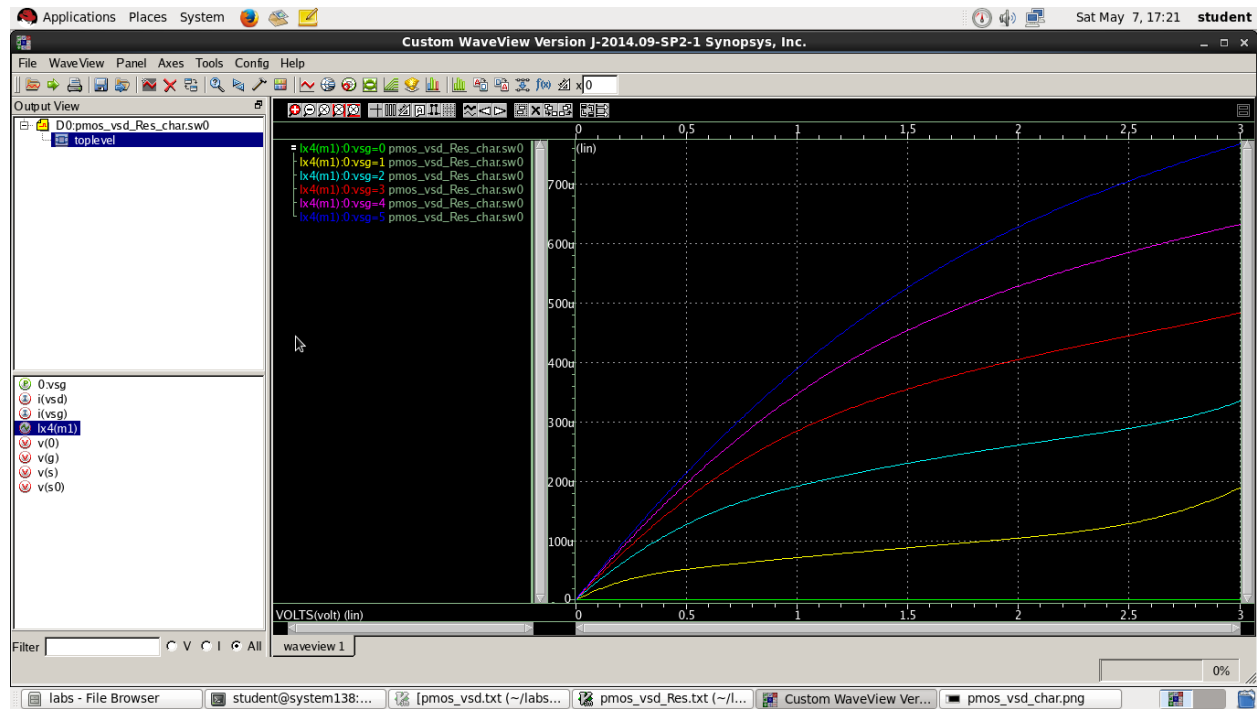
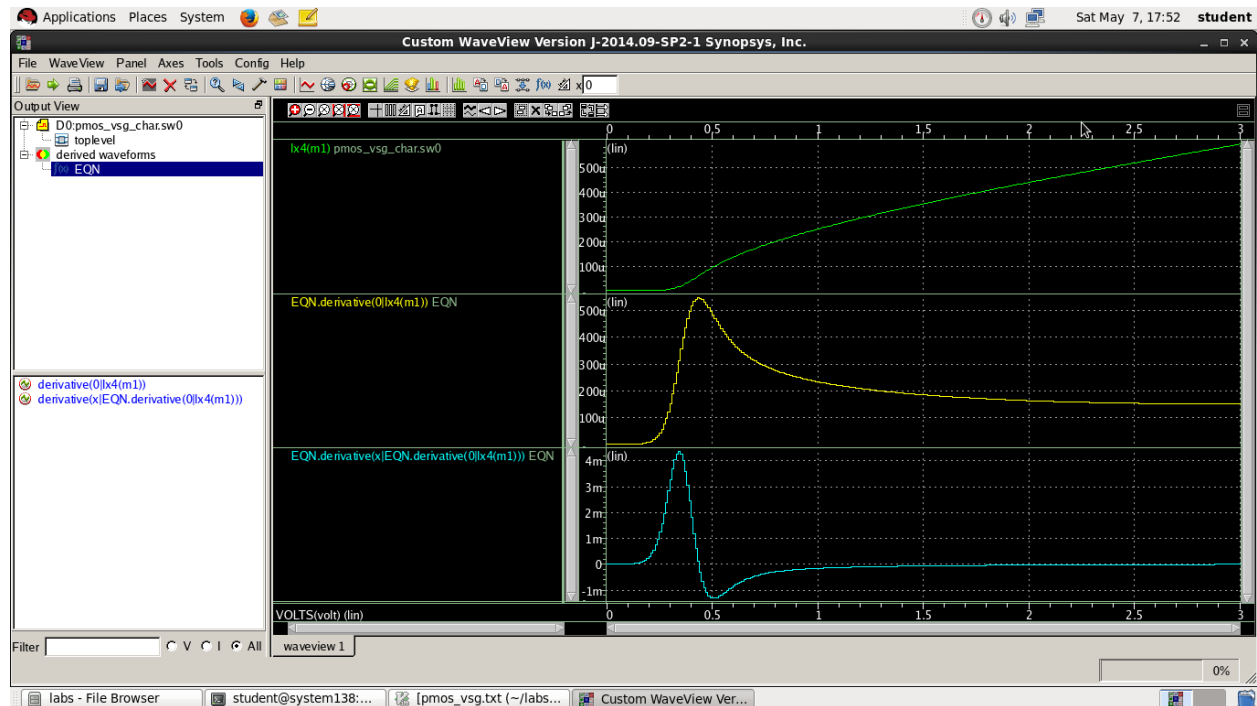
NMOS Vds:

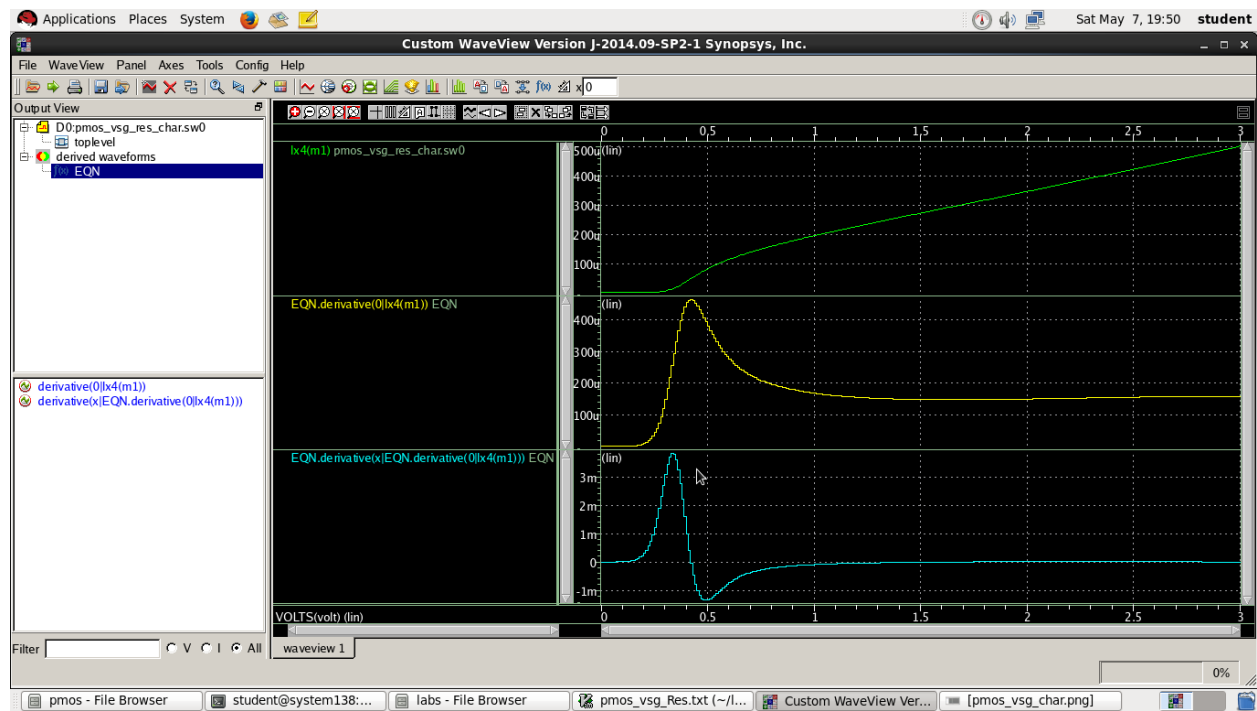
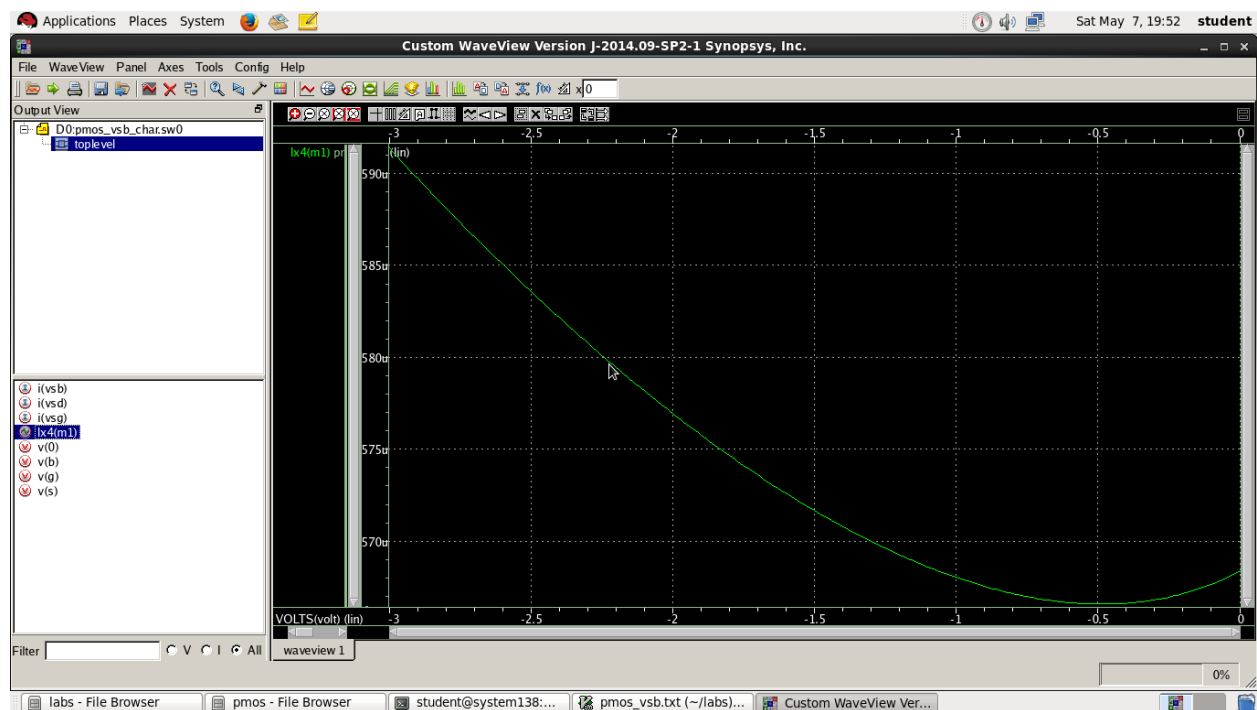


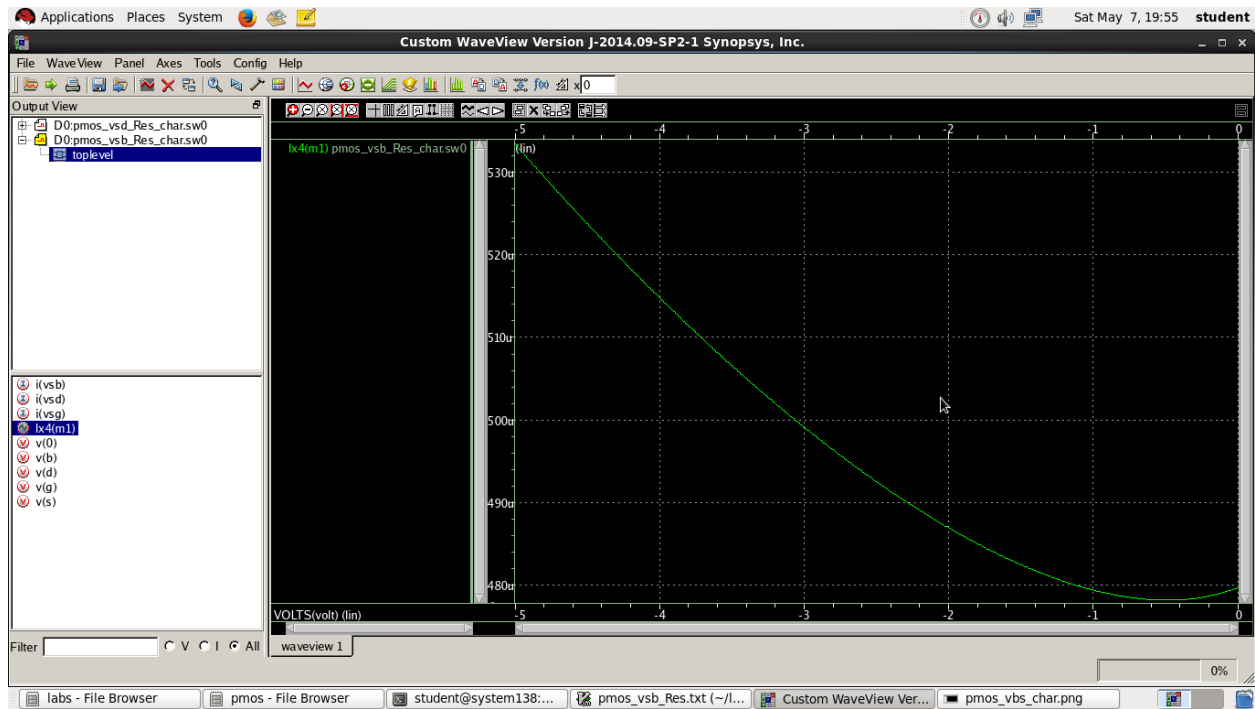
NMOS Vds with Resistance:**NMOS Vgs:**

NMOS V_{gs} with resistance:**NMOS V_{bs} :**

NMOS Vbs with resistance:**PMOS Vsd:**

PMOS Vsd with resistance:**PMOS Vsg:**

PMOS Vsg with resistance:**PMOS Vbs:**

PMOS Vbs with resistance:**INFERENCE:**

- Analyzed the characteristics of enhancement p- and n- type MOSFET
- Modeled the devices only by designing netlist for the operation
- Assigned node names for the MOSFETs and provided the input
- Manually written the netlist for the devices, so schematic is not required
- Since node names were assigned, connections can be easily monitored