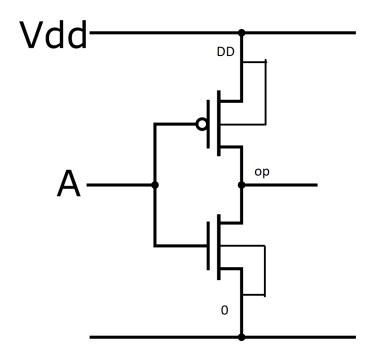
<expt. no.<="" th=""><th>1a -</th><th>MOSFET device and CMOS inverter characte</th><th>rization using</th><th>g HSPICE</th></expt.>	1a -	MOSFET device and CMOS inverter characte	rization using	g HSPICE
NAME:	S.	Chandra Moulee	Date:	07/05/2022
ROLL No).:	CB.EN.P2VLD21016	Marks:	out of 10

AIM:

To obtain MOSFET device and CMOS inverter characterization using HSPICE

BLOCK/CIRCUIT DIAGRAM:



CODE:

*CMOS Characteristics

.MODEL PCH PMOS LEVEL=54

.MODEL NCH NMOS LEVEL=54

MPA op A DD DD PCH L=L W=W

MNA op A 0 0 NCH L=L W=W

vdd DD 03

va A 0 3

.DATA d1

L W

90n 225n

100n 250n

120n 280n

.ENDDATA

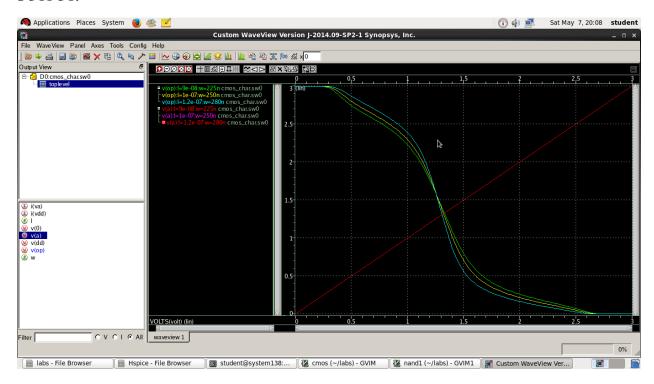
.DC va 0 3 0.01 SWEEP DATA=d1

.plot DC V(A) V(op)

.option post

.end

OUTPUT:



INFERENCE:

- Analyzed the CMOS inverter characteristics using Hspice tool
- Modeled the devices only by designing netlist for the operation with level 54 devices
- Assigned node names for the MOSFET devices and provided input and analyzed the output characteristics
- Manually written the netlist for the devices, so schematic is not required
- Since node names were assigned, connections can be easily monitored
- Analyzed the output characteristics of the CMOS inverter device with three different W and L values keeping the W/L ratio as 2.5 for all W, L values respectively