<Expt. No. 5 - Design and synthesis an 8-bit ALU in Basys 3 FPGA and perform logic and arithmetic operations	
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ROLL No.: CB.EN.P2VLD21016	**Marks :** **out of 10**

AIM:

To Design and synthesis an 8-bit ALU in Basys 3 FPGA and perform the following logic and arithmetic operations

1. Arithmetic Addition

   ALU_Out = A + B;

2. Logical Shift Left

   ALU_Out = A logical shifted left by 1;

3. Logical AND

   ALU_Out = A AND B;

4. Logical XOR

   ALU_Out = A XOR B;

5. Equal comparison

   ALU_Out = 1 A = B else 0;

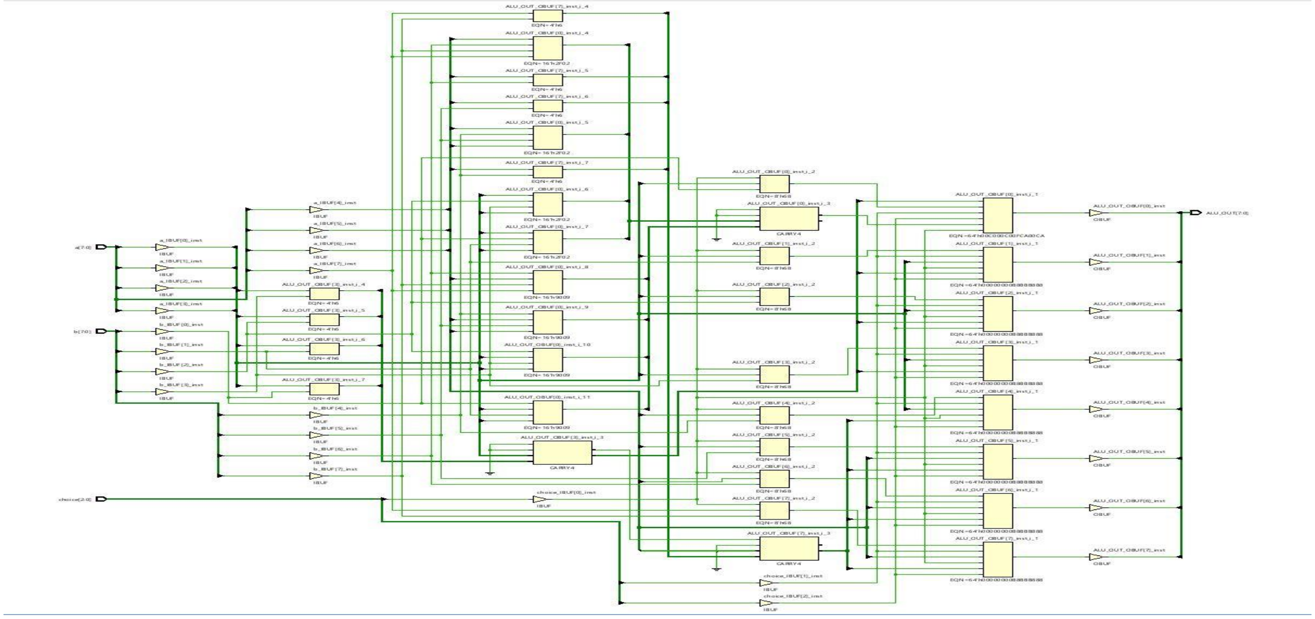
CODE:

```
module alu (a, b, ALU_OUT, choice);

input [2:0]choice;

input [7:0] a, b;

output reg [7:0] ALU_OUT;

parameter add=3'b000, ls=3'b001, and_8_bit=3'b010, exor=3'b011, comp=3'b100;


always@ (choice)

begin

case (choice)

add:    ALU_OUT = a+b; //Addition
```

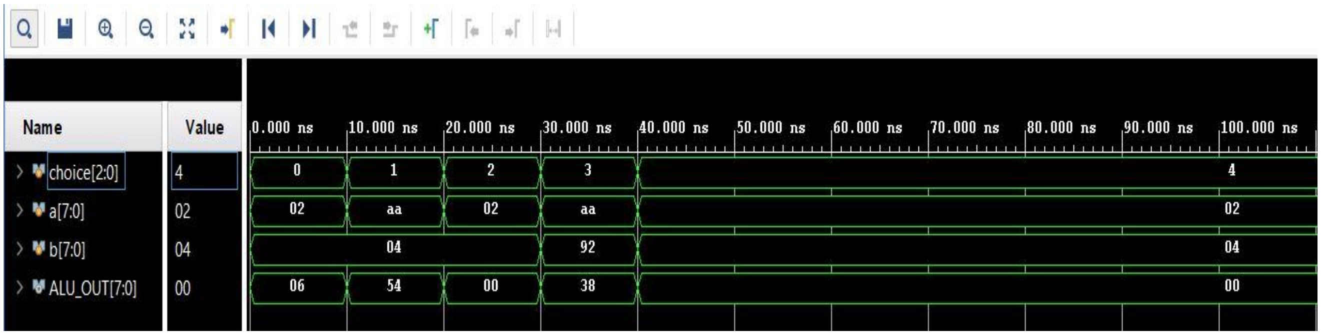
```
ls:       ALU_OUT = a<<1; //Left shift
and_8_bit: ALU_OUT = a & b; //AND operation
exor:      ALU_OUT = a ^ b; // EXOR operation
comp:              //Comparator
        begin
             if (a>b)
             ALU_OUT = 1'b1;
             else
             ALU_OUT=1'b0;
             end
default: ALU_OUT = 0;
endcase
end

endmodule

module tb_alu ();
reg [2:0]choice;
reg [7:0] a, b;
wire [7:0] ALU_OUT;

initial
begin

choice = 3'b000;
a=8'd2;
b=8'd4;
#10;

choice = 3'b001;
```

```
a=8'b10101010;
#10;

choice = 3'b010;
a=8'd2;
b=8'd4;
#10;

choice = 3'b011;
a=8'b10101010;
b=8'b10010010;
#10;

choice = 3'b100;
a=8'd2;
b=8'd4;
#10;

end

alu inst0(.a(a), .b(b), .ALU_OUT(ALU_OUT), .choice(choice));
endmodule
```

SCHEMATIC DIAGRAM:



OUTPUT:



Name	Value	0.000 ns	10.000 ns	20.000 ns	30.000 ns	40.000 ns	50.000 ns	60.000 ns	70.000 ns	80.000 ns	90.000 ns	100.000 ns
choice[2:0]	4	0	1	2	3							4
a[7:0]	02	02	aa	02	aa							02
b[7:0]	04		04		92							04
ALU_OUT[7:0]	00	06	54	00	38							00

ADD Operation:

a= 2d

b= 4d

ALU_OUT= 6d

Left shift Operation:

a=8'b10101010;

ALU_OUT = 54h (01010100)

AND Operation:

a=8'd2

b=8'd4

ALU_OUT = 0

Xor Operation:

a=8'b10101010

b=8'b10010010

ALU_OUT = 38

Comparison Operation:

a=8'd2

b=8'd4

ALU_OUT = 0

INFERENCE:

- Designed an 8 bit ALU logic operator for BASYS 3 board
- Operations are performed using two 8 bit input variables
- In this design ADD, Left shift, AND, XOR and Comparator operations were implemented
- Provided teh testbench for the design in Xilinx Vivado and obtained the outputs
- Schematic design is also obtained using Vivado