DETECTION AND CORRECTION OF TIMING VIOLATIONS IN SEQUENTIAL CIRCUITS

STA TERM WORK REPORT

Submitted by

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Abstract:

Sequential circuits work based on the clock signal, timing violations in the sequential circuits depend on the clock signal only. Static Timing analysis for any circuit depends on timing checks, design constraints and libraries. The design constraints are provided by the user and the library files are pre defined, so the timing check is the only parameter that can be changed in order to avoid any violation while designing itself. The timing chek depends on the timing path (critical path), arrival time, required time and min, max slack. Timing path refers to the path between the start point of the input port of the launch flip flop and the output port of the capture flip flop. Slack is the difference between the required and arrival time. Required time is the difference between the clock and setup time and arrival time is the difference between the clk-Q propagation time and combinational delay. Minimum slack is (Arrival time - Required time) and Maximum slack is (Required time - Arrival time). Slack of a sequential circuit depends on the clock signal, setup and hold times. The setup and hold times is based on the active edge of the clock signal, so the entire is indirectly based on the clock signal and its active edge. The setup and hold analysis depends on the paths such as register-register, input-register, register-output, input-output and other factors such as clock gating, recovery, removal time, data-data path, latch, slew, load (Fan-out, Capacitance) and clock timings (skew, pulse width). Even though the circuits are designed based on the timing analysis, it will not be the same when it is implemented in the hardware due to a factor called On-Chip variation (OCV). Usually OCV value will be around 20% i.e.., for a circuit of clock with 10ns, due to OCV, it might oscillate between 0/8 to 1.2 ns. The increase in the delay value due to OCV is called “Clock push-out” and the decrease in delay value is called “Clock pull-in”. Decrease in the clock signal signal timing will lead to the setup time violation. Synchronous sequential circuits need precise timing parameters and violations in these specifications causes the Chip to operate with reduced frequency or total failure of the chip. In order to avoid any timing violations in the sequential circuit, delay buffers and time borrowing principles are used, which are fixed and cannot be modified after implementing the circuit, so in this method a detector and corrector circuit is used for detecting the violations in the circuit and selecting clock signal depending upon the amount of the clock value required. The detector circuit has a detector circuit that takes the clock and data as the input. Both are provided to a one shot detector and provided to an NAND gate and a buffer which detects latency between the data and clock signal. The detector circuit produces two signals which are provided as the select lines to the multiplexer in the corrector circuit that selects the clock signal required depending upon the clock required. The multiplexer circuits are provided with clock signal with step increase in base clock signals

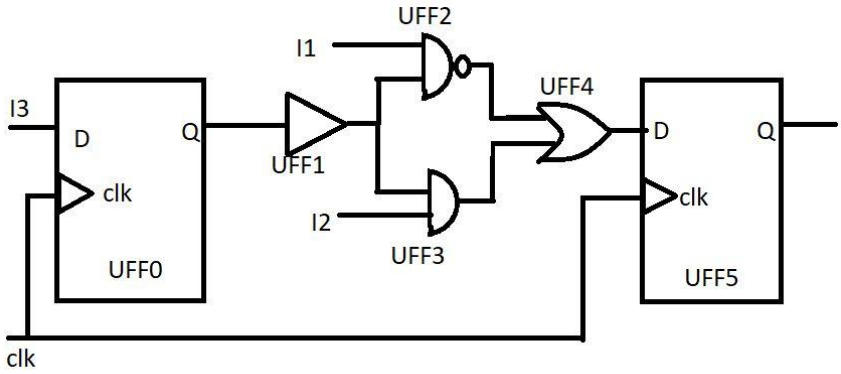
Objective:

To design a circuit that has a negative slack and do the following:

1. To detect the violation through the detector circuit
2. To modify the clock signal depending on the signal from the detector circuit and correct the clock signal using the corrector circuit

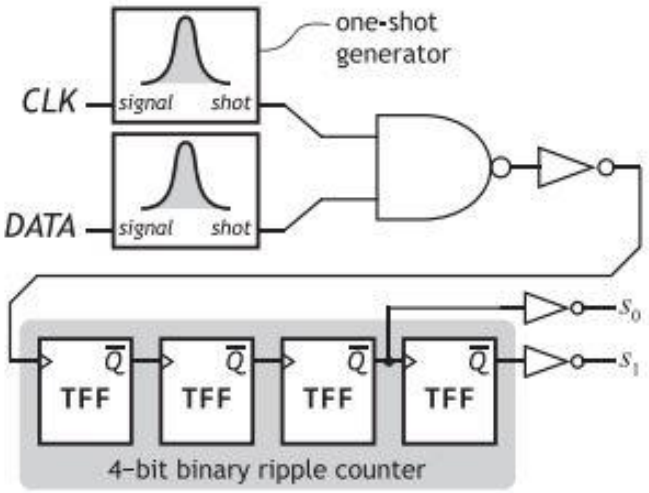
Methodology:

Circuit considered:



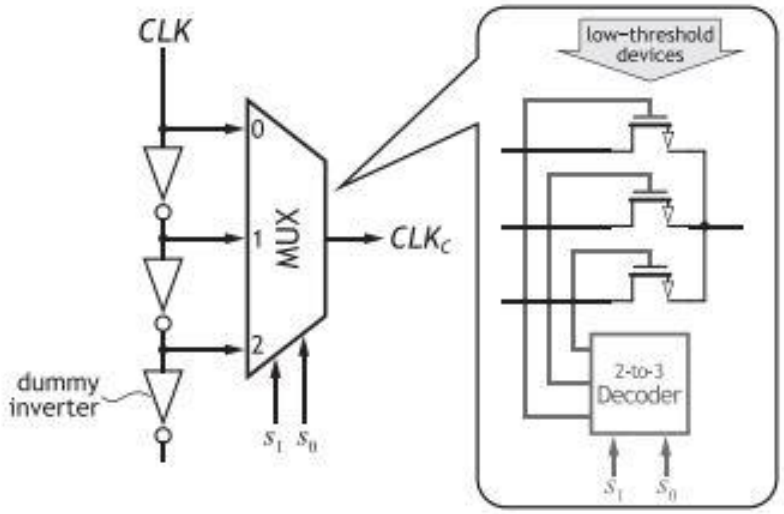
The circuit is provided with the clock of 1 ns period and duty cycle of 40%. The circuit has a launch and capture flip flop of naming UFF0 and UFF5 respectively. The combinational circuit has four gates such as UFF1, UFF2, UFF3 and UFF4. The circuit has three inputs, one provided to the launch flip flop and two for gates UFF2 and UFF3. The gates provide the combinational delay.

Detector circuit:



The detector circuit has two one shot generators which take inputs from the clock signal and the data the shots generated are provided to an NAND gate and an inverter. The output from the buffer is provided to a series of Toggle flip flops from the last two flip flops, two outputs S0 and S1 are obtained.

Corrector circuit:



The corrector circuit has three or four inputs depending upon the sequential circuit. If three different clocks are only required, then three buffer circuits are used. The multiplexer is made of a low threshold CMOS device exited by a 2X4 decoder in it. Based on the select line, the output clock is selected.

Working:

The one shot generator in the detector circuit detects the edge of the clock and data signal. When there is no time gap between the active edge of clock and data signal, output from the NAND gate will be 0 and the inverter produces active high signal, so the signal gets inverter again through the toggle flip flop and the value of S0 and S1 will be both 0, so the correction circuit will take the first input which the sam clock signal as the output. Similarly when there is time gap between the active edge of clock and data signal, then the NAND gate will be 1 and the inverter produces active low signal, so the signal gets inverter again through the toggle flip flop and the value of S0 and S1 will change accordingly, suppose if the time gap is low, then S0, S1 will be 0,1 and if it is high then S0, S1 will be 1,1 which will take the respective step increased clock signals and then the new signal will be set as master clock signal then buffers are provided from that clock. If the new clock signal doesn't have any time gap with the data signal, then the new clock signal will be at S0,S1 = 0,0

Results obtained:

Slack results for the circuits obtained with assumed clock signal,

Vivado result:

```
Max Delay Paths
--------------------------------------------------------------------------------
Slack (VIOLATED) :        -0.441ns  (required time - arrival time)
  Source:                 uff0/Q_reg/C
                            (rising edge-triggered cell FDRE clocked by clk  {rise@0.000ns fall@0.020ns period=0.100ns})
  Destination:            uff5/Q_reg/D
                            (rising edge-triggered cell FDRE clocked by clk  {rise@0.000ns fall@0.020ns period=0.100ns})
  Path Group:             clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            0.100ns  (clk rise@0.100ns - clk rise@0.000ns)
  Data Path Delay:        0.522ns  (logic 0.322ns (61.629%)  route 0.200ns (38.371%))
  Logic Levels:           1  (LUT3=1)
  Clock Path Skew:        -0.018ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.467ns = ( 4.567 - 0.100 )
    Source Clock Delay      (SCD):    4.762ns
    Clock Pessimism Removal (CPR):    0.277ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock clk rise edge)        0.000     0.000 r
    P23                                               0.000     0.000 r  clk (IN)
                         net (fo=0)                   0.000     0.000    clk
    P23                  IBUF (Prop_ibuf_I_O)         0.845     0.845 r  clk_IBUF_inst/O
                         net (fo=1, routed)           2.140     2.985    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.120     3.105 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)           1.657     4.762    uff0/clk_IBUF_BUFG
    SLICE_X1Y2           FDRE                                       r  uff0/Q_reg/C
  -------------------------------------------------------------------    -------------------
    SLICE_X1Y2           FDRE (Prop_fdre_C_Q)         0.269     5.031 r  uff0/Q_reg/Q
                         net (fo=1, routed)           0.200     5.232    uff0/Q
    SLICE_X0Y2           LUT3 (Prop_lut3_I1_O)        0.053     5.285 r  uff0/Q_i_1/O
                         net (fo=1, routed)           0.000     5.285    uff5/q4
    SLICE_X0Y2           FDRE                                       r  uff5/Q_reg/D
  -------------------------------------------------------------------    -------------------

                         (clock clk rise edge)        0.100     0.100 r
    P23                                               0.000     0.100 r  clk (IN)
                         net (fo=0)                   0.000     0.100    clk
    P23                  IBUF (Prop_ibuf_I_O)         0.769     0.869 r  clk_IBUF_inst/O
                         net (fo=1, routed)           2.040     2.909    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.113     3.022 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)           1.545     4.567    uff5/clk_IBUF_BUFG
    SLICE_X0Y2           FDRE                                       r  uff5/Q_reg/C
                         clock pessimism              0.277     4.844
                         clock uncertainty           -0.035     4.809
    SLICE_X0Y2           FDRE (Setup_fdre_C_D)        0.035     4.844    uff5/Q_reg
  -------------------------------------------------------------------
                         required time                          4.844
                         arrival time                          -5.285
  -------------------------------------------------------------------
                         slack                                 -0.441
```

DC_shell result:

```
Startpoint: uff0/Q_reg (rising edge-triggered flip-flop clocked by clk)
Endpoint: uff5/Q_reg (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
setup              ForQA                 saed90nm_max
dff_0              ForQA                 saed90nm_max
dff_1              ForQA                 saed90nm_max

Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (ideal)              0.00       0.00
uff0/Q_reg/CLK (DFFX1)                   0.00       0.00 r
uff0/Q_reg/QN (DFFX1)                    0.43       0.43 f
uff0/U5/ZN (INVX0)                       0.14       0.56 r
uff0/Q (dff_0)                           0.00       0.56 r
U25/Q (OR2X1)                            0.23       0.79 r
uff5/D (dff_1)                           0.00       0.79 r
uff5/U3/Q (AND2X1)                       0.23       1.02 r
uff5/Q_reg/D (DFFX1)                     0.05       1.06 r
data arrival time                                   1.06

clock clk (rise edge)                    1.00       1.00
clock network delay (ideal)              0.00       1.00
uff5/Q_reg/CLK (DFFX1)                   0.00       1.00 r
library setup time                      -0.28       0.72
data required time                                  0.72
-----------------------------------------------------------
data required time                                  0.72
data arrival time                                  -1.06
-----------------------------------------------------------
slack (VIOLATED)                                   -0.34
```

Slack report after detector and corrector circuit:

Vivado report:

```
Slack (MET) :             9.460ns  (required time - arrival time)
  Source:                 uff0/Q_reg/C
                            (rising edge-triggered cell FDRE clocked by clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            uff5/Q_reg/D
                            (rising edge-triggered cell FDRE clocked by clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (clk rise@10.000ns - clk rise@0.000ns)
  Data Path Delay:        0.540ns  (logic 0.404ns (74.805%)  route 0.136ns (25.195%))
  Logic Levels:           1  (LUT3=1)
  Clock Path Skew:        0.000ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.467ns = ( 14.467 - 10.000 )
    Source Clock Delay      (SCD):    4.762ns
    Clock Pessimism Removal (CPR):    0.295ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock clk rise edge)        0.000     0.000 r
    P23                                               0.000     0.000 r  clk (IN)
                         net (fo=0)                   0.000     0.000    clk
    P23                  IBUF (Prop_ibuf_I_O)         0.845     0.845 r  clk_IBUF_inst/O
                         net (fo=1, routed)           2.140     2.985    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.120     3.105 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)           1.657     4.762    uff0/clk_IBUF_BUFG
    SLICE_X0Y2           FDRE                                       r  uff0/Q_reg/C
  -------------------------------------------------------------------    -------------------
    SLICE_X0Y2           FDRE (Prop_fdre_C_Q)         0.246     5.008 r  uff0/Q_reg/Q
                         net (fo=1, routed)           0.136     5.144    uff0/Q
    SLICE_X0Y2           LUT3 (Prop_lut3_I1_O)        0.158     5.302 r  uff0/Q_i_1/O
                         net (fo=1, routed)           0.000     5.302    uff5/q4
    SLICE_X0Y2           FDRE                                       r  uff5/Q_reg/D
  -------------------------------------------------------------------    -------------------

                         (clock clk rise edge)       10.000    10.000 r
    P23                                              0.000    10.000 r  clk (IN)
                         net (fo=0)                  0.000    10.000    clk
    P23                  IBUF (Prop_ibuf_I_O)        0.769    10.769 r  clk_IBUF_inst/O
                         net (fo=1, routed)          2.040    12.809    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)        0.113    12.922 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)          1.545    14.467    uff5/clk_IBUF_BUFG
    SLICE_X0Y2           FDRE                                       r  uff5/Q_reg/C
                         clock pessimism             0.295    14.762
                         clock uncertainty          -0.035    14.727
    SLICE_X0Y2           FDRE (Setup_fdre_C_D)       0.035    14.762    uff5/Q_reg
  -------------------------------------------------------------------
                         required time                         14.762
                         arrival time                          -5.302
  -------------------------------------------------------------------
                         slack                                  9.460
```

DC_shell report:

```
| Timing Details
| --------------
--------------------------------------------------------------------------------------------------------


--------------------------------------------------------------------------------------------------------
From Clock:  clk
  To Clock:  clk

Setup :            0  Failing Endpoints,  Worst Slack        9.460ns,  Total Violation        0.000ns
Hold  :            0  Failing Endpoints,  Worst Slack        0.154ns,  Total Violation        0.000ns
PW    :            0  Failing Endpoints,  Worst Slack        4.600ns,  Total Violation        0.000ns
--------------------------------------------------------------------------------------------------------


Max Delay Paths
--------------------------------------------------------------------------------
Slack (MET) :             9.460ns  (required time - arrival time)
  Source:                 uff0/Q_reg/C
                            (rising edge-triggered cell FDRE clocked by clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            uff5/Q_reg/D
                            (rising edge-triggered cell FDRE clocked by clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (clk rise@10.000ns - clk rise@0.000ns)
  Data Path Delay:        0.540ns  (logic 0.404ns (74.805%)  route 0.136ns (25.195%))
  Logic Levels:           1  (LUT3=1)
  Clock Path Skew:        0.000ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.467ns = ( 14.467 - 10.000 )
    Source Clock Delay      (SCD):    4.762ns
    Clock Pessimism Removal (CPR):    0.295ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock clk rise edge)        0.000     0.000 r
    P23                                               0.000     0.000 r  clk (IN)
                         net (fo=0)                   0.000     0.000    clk
    P23                  IBUF (Prop_ibuf_I_O)         0.845     0.845 r  clk_IBUF_inst/O
                         net (fo=1, routed)           2.140     2.985    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.120     3.105 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)           1.657     4.762    uff0/clk_IBUF_BUFG
    SLICE_X0Y2           FDRE                                       r  uff0/Q_reg/C
  -------------------------------------------------------------------    -------------------
    SLICE_X0Y2           FDRE (Prop_fdre_C_Q)         0.246     5.008 r  uff0/Q_reg/Q
                         net (fo=1, routed)           0.136     5.144    uff0/Q
    SLICE_X0Y2           LUT3 (Prop_lut3_I1_O)        0.158     5.302 r  uff0/Q_i_1/O
                         net (fo=1, routed)           0.000     5.302    uff5/q4
    SLICE_X0Y2           FDRE                                       r  uff5/Q_reg/D
  -------------------------------------------------------------------    -------------------

                         (clock clk rise edge)       10.000    10.000 r
    P23                                              0.000    10.000 r  clk (IN)
                         net (fo=0)                  0.000    10.000    clk
    P23                  IBUF (Prop_ibuf_I_O)        0.769    10.769 r  clk_IBUF_inst/O
                         net (fo=1, routed)          2.040    12.809    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)        0.113    12.922 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)          1.545    14.467    uff5/clk_IBUF_BUFG
    SLICE_X0Y2           FDRE                                       r  uff5/Q_reg/C
                         clock pessimism             0.295    14.762
                         clock uncertainty          -0.035    14.727
    SLICE_X0Y2           FDRE (Setup_fdre_C_D)       0.035    14.762    uff5/Q_reg
  -------------------------------------------------------------------
                         required time                         14.762
                         arrival time                          -5.302
  -------------------------------------------------------------------
                         slack                                  9.460
```

Inference:

- Designed a circuit with launch and capture flip flop and combinational circuits in between using verilog code
- Generated clock with low period and duty cycle for getting the negative slack
- Implemented the detector and corrector circuit using two separate modules in the same file
- Detector circuit has a one shot generator for clock and data signal and the time difference between the signals is converted into two outputs
- Corrector circuit has a multiplexer with two select lines with system clock and buffered blocks from the clock
- Provided instantiation of the circuit to the detector and corrector circuit
- Generated timing report for the circuit before and after adding the detector, corrector modules
- Compared the timing report using Xilinx Vivado and Synopsys DC_shell

Conclusion:

Designed and implemented a detector and corrector circuit for a sequential circuit that has timing violation in it using