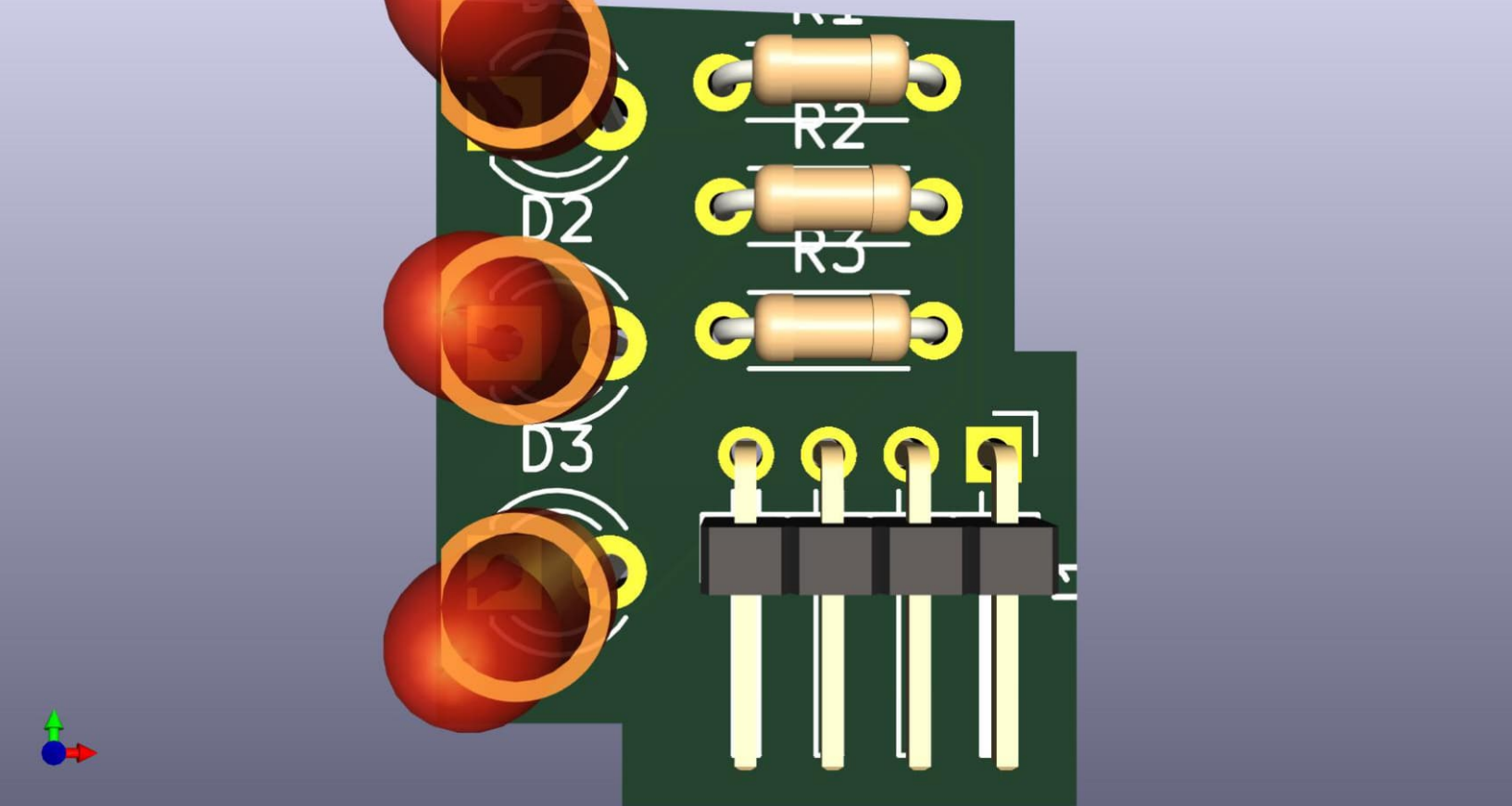
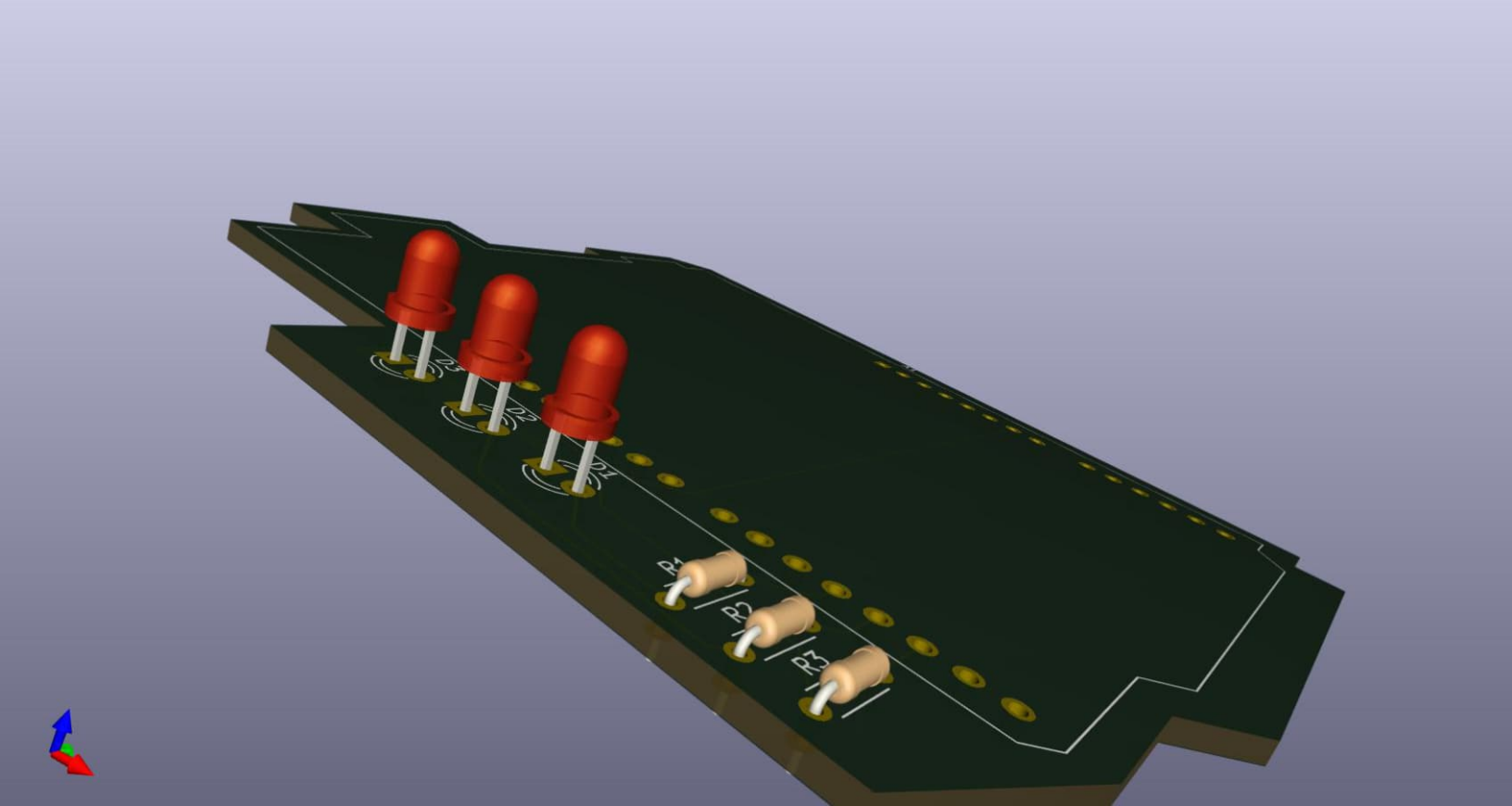

R2
D2
R3
D3


D1
D2
D3
R1
R2
R3

Refill all zones before performing DRC

Test for parity between PCB and schematic

Report all errors for each track

Violations (0) Unconnected Items (0) Schematic Parity (not run) Ignored Tests (4)

Show: All Errors 0 Warnings 0 Exclusions Save...

Delete Marker Delete All Markers Run DRC Close