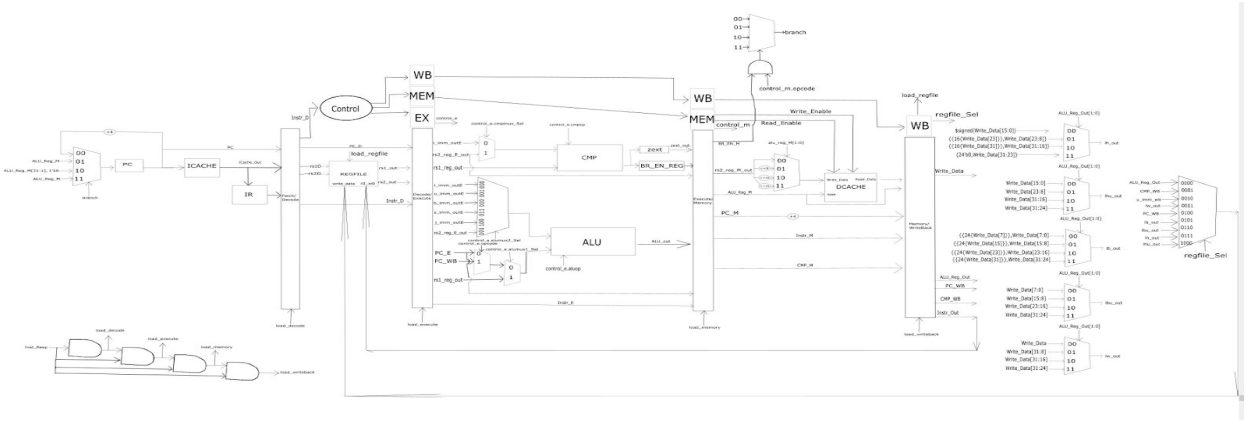
Progress Report:

For checkpoint 2, Shounak and Taras have begun planning how to implement our L1 cache designs which we created in checkpoint 1 with additional input and verification from Kevin. The arbiter implementation is being done by everyone as it is easier to understand the overall design of the cache with a good understanding of how the arbiter interacts with the caches. Meanwhile, we all have also begun to fix our MP2 cache designs since our implementations were not totally correct and based on the TA meeting, we were given a better idea on what needed to be fixed. We decided to work off of Kevin's original design as it was the one that was closest to working and Shounak and Taras were able to add their input and verification on the cache fixes. As a group, we also started working on a design to get our shadow memory working. Kevin and Taras also worked on the initial design for the datapath for data forwarding with insight and input from Shounak. Along with everything priorly stated, every member is collectively working on a report identifying the problems in the MP2 cache, and how to address them.

As for checkpoint 1, the paper design and datapath for the cpu was done by taras and Kevin, with Shounak's verification. The implementation of the design was completed by Kevin and Shounak, with input and debugging help from Taras. The paper designs for the L1 cache and arbiter design were done by Taras with input and verification from Kevin and Shounak.

This is an updated datapath with all the implementation post cp1. A higher resolution can be found on our github repository.



Roadmap:

For checkpoint 3, we will all collaborate and work together to implement hazard detection and the forwarding unit. In this scenario it makes more sense to collectively work as a group on arguably the hardest portion of the MP. Along with the hazard detection and forwarding unit, we will also implement the rest of the RVFI monitor signals to have a functional RVFI monitor. Taras will work on implementing the L2 Cache with overview from Kevin and Shounak, since Taras was the one who designed it. We will each come up with proposals for advanced features and collectively decide which one we will pursue with the approval of the TA.