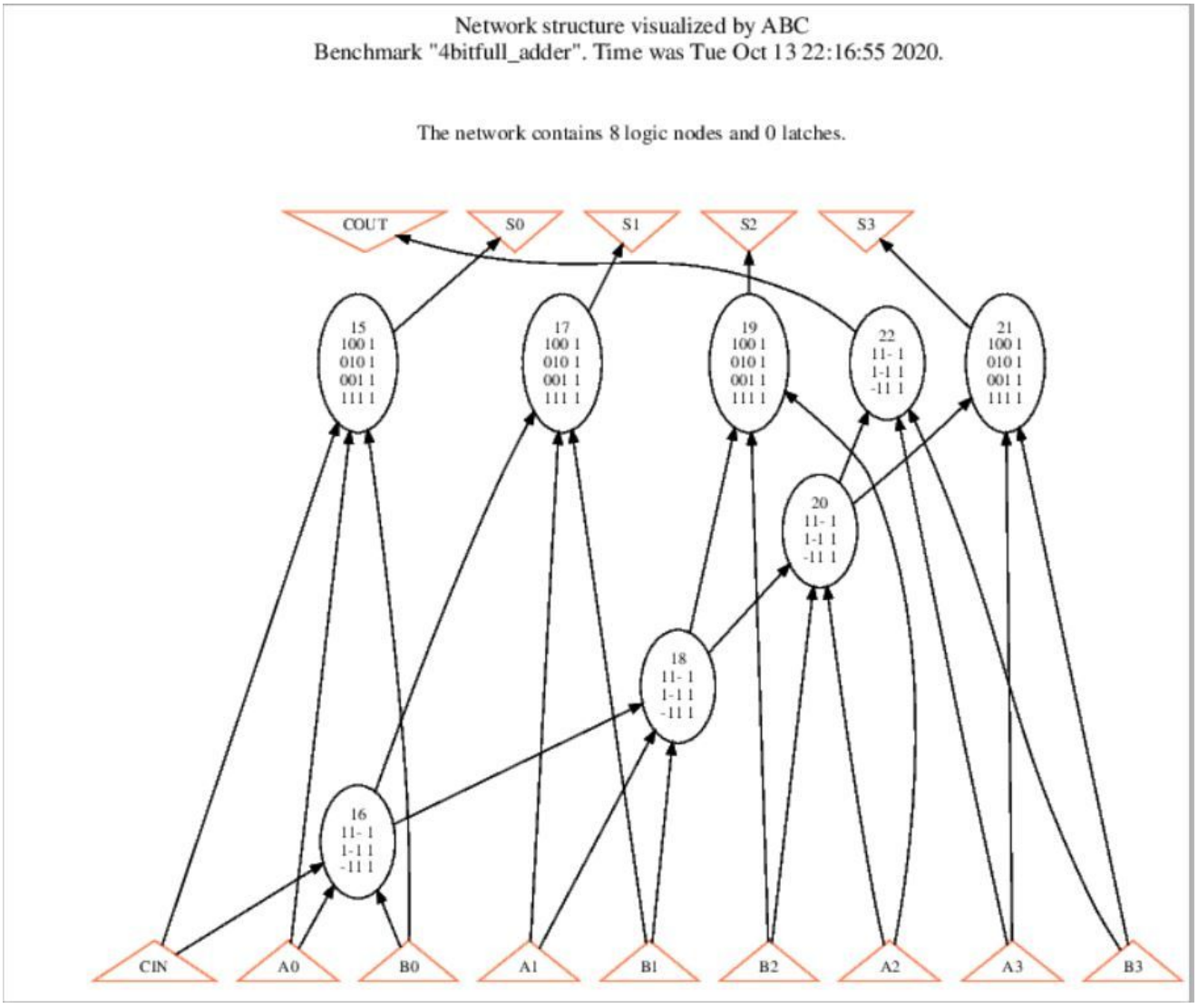
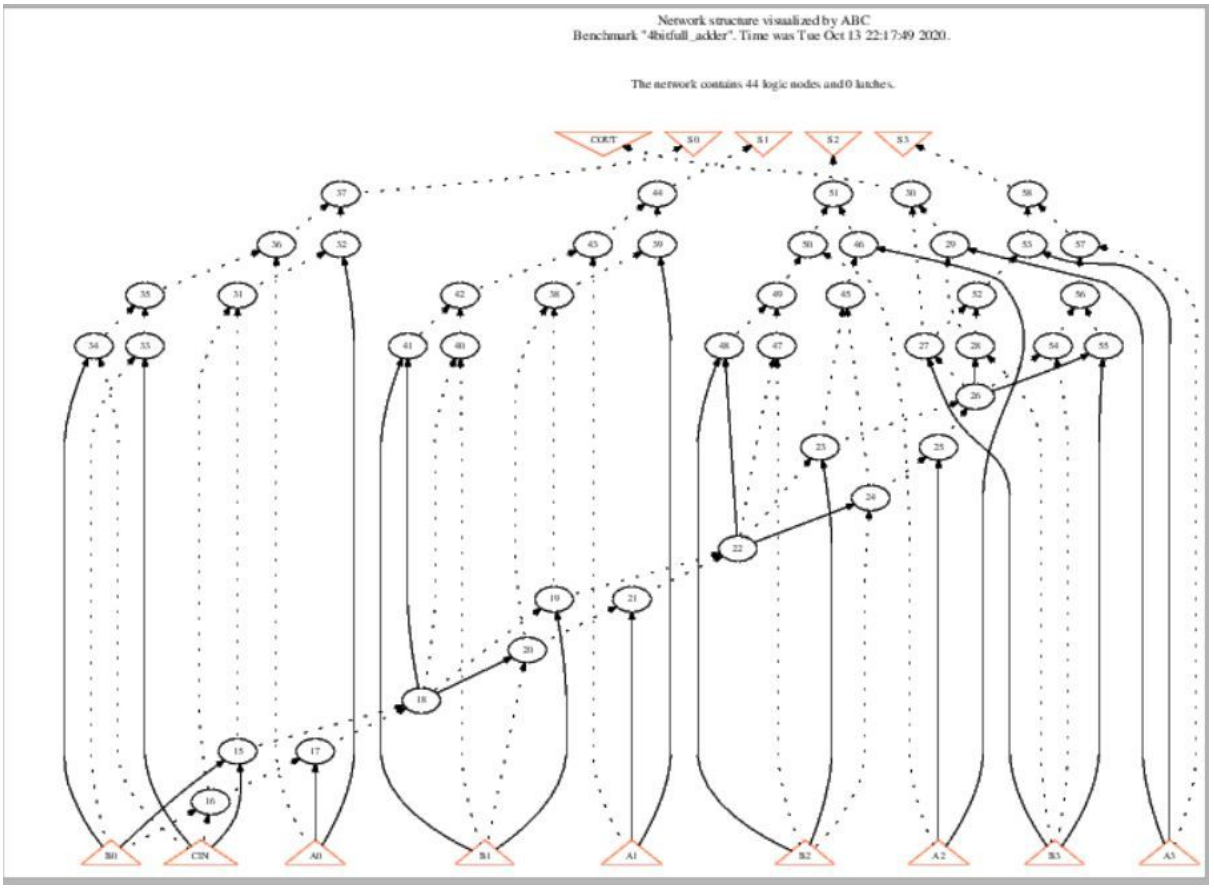
1. [Using ABC]

為了方便閱讀和不用放大，所以一頁只放一張圖片~

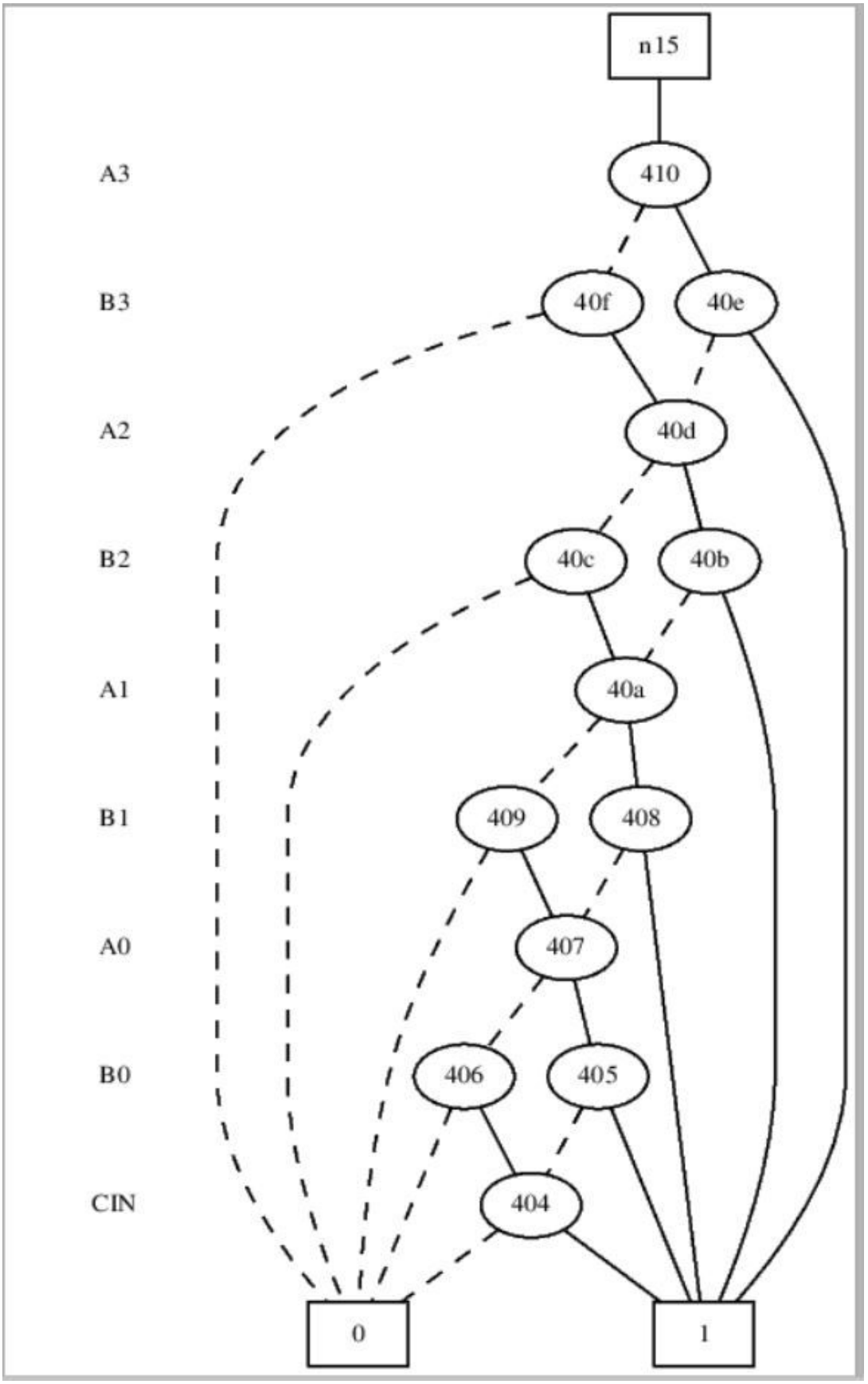
▼ 這張是直接show出來的圖片



下面這張是先strash再show出來的圖片



下面這張是先collapse再show_bdd出來的圖片



2. [ABC Boolean Function Representations]

(a) Compare the following differences with the four-bit adder example.

(1) logic network in AIG (by command `aig`) vs. structurally hashed AIG (by command `strash`)

```
UC Berkeley, ABC 1.01 (compiled Oct 13 2020 21:17:13)
abc 01> read lsv/pa1/4bitfull_adder.blif
Hierarchy reader flattened 4 instances of logic boxes and left 0 black boxes.
abc 02> print_stats
4bitfull_adder             : i/o =    9/    5  lat =    0  nd =     8  edge =     24  cube =    28  lev = 4
abc 02> aig
abc 02> print_stats
4bitfull_adder             : i/o =    9/    5  lat =    0  nd =     8  edge =     24  aig  =    52  lev = 4
```

aig 的功能是將原本的 logic network 裡面的 gates 都變成 and-inv 的形式

```
UC Berkeley, ABC 1.01 (compiled Oct 13 2020 21:17:13)
abc 01> read lsv/pa1/4bitfull_adder.blif
Hierarchy reader flattened 4 instances of logic boxes and left 0 black boxes.
abc 02> print_stats
4bitfull_adder             : i/o =    9/    5  lat =    0  nd =     8  edge =     24  cube =    28  lev = 4
abc 02> strash
abc 03> print_stats
4bitfull_adder             : i/o =    9/    5  lat =    0  and =     44  lev = 13
```

strash的功能則是直接用 AIG graph 代表整個 logic network

雖然兩者的功能都是把 logic network 化成 AIG，但 aig 應該只是把原本的SOP給拆開來(所以依然還是SOP的狀態，改變的只有node function)，但 strash 則是把原本的 logic network 轉換成由 POs 連到 PIs 的 AIG

(2) logic network in BDD (by command `bdd`) vs. collapsed BDD (by command `collapse`)

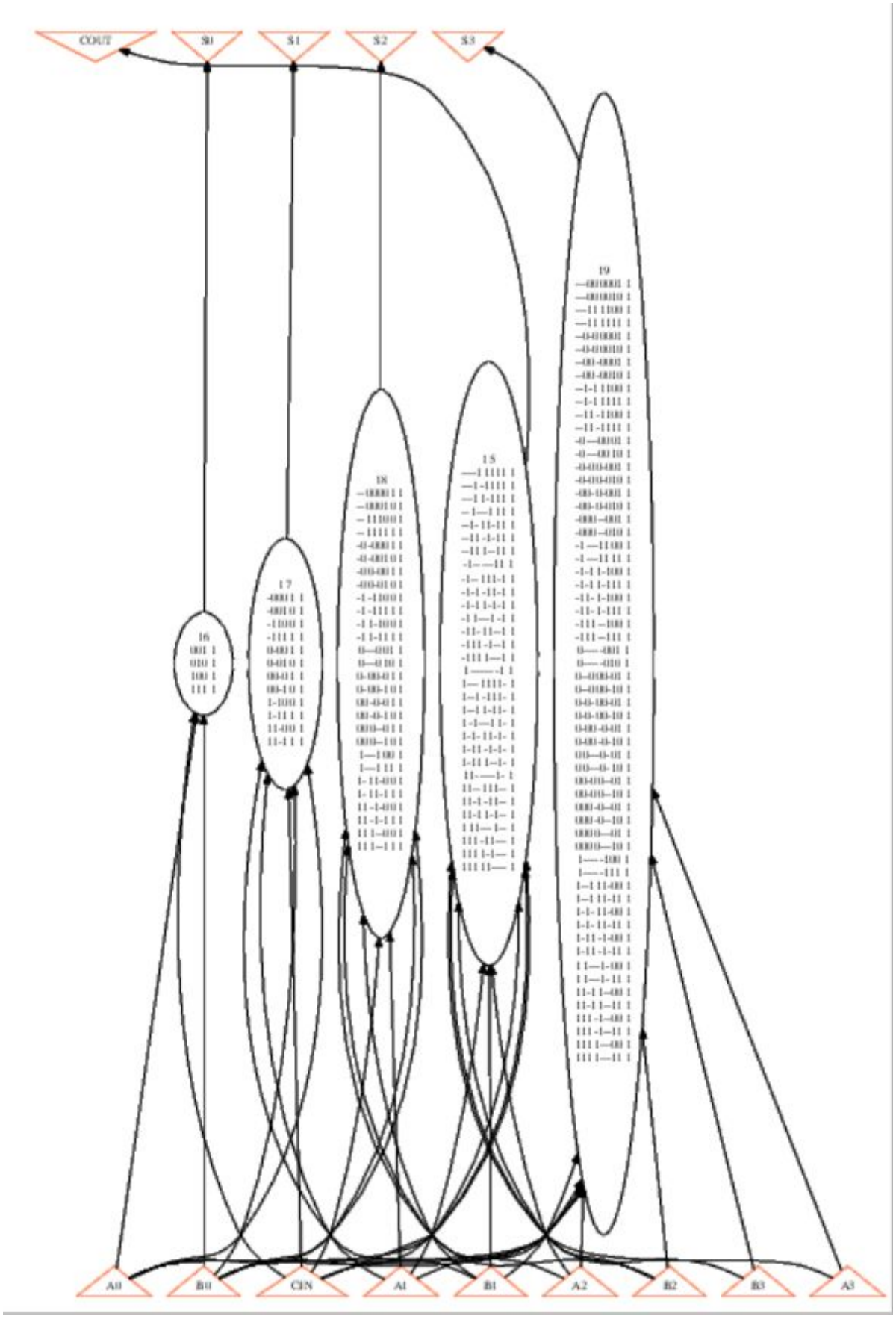
```
abc 02> print_stats
4bitfull_adder             : i/o =    9/    5  lat =    0  nd =     8  edge =     24  cube =    28  lev = 4
abc 02> bdd
abc 02> print_stats
4bitfull_adder             : i/o =    9/    5  lat =    0  nd =     8  edge =     24  bdd  =    28  lev = 4
```

bdd 的功能是將 logic network 用 BDD 的表示方式存起來

```
abc 02> print_stats
4bitfull_adder             : i/o =    9/    5  lat =    0  nd =     8  edge =     24  cube =    28  lev = 4
abc 02> collapse
abc 03> print_stats
4bitfull_adder             : i/o =    9/    5  lat =    0  nd =     5  edge =     33  bdd  =    43  lev = 1
```

collapse的功能是把全部POs和PIs的關係都拆開來做成BDD

經過bdd之後的 logic network 還是原本的 logic network 只是中間的 node function 都被用 BDD 表示了(所以原本gate level有多少應該就不會變)，但經過 collapse之後的 logic network就變成每個 POs 都直接對應到 PIs 了(會直接變成1個 level 如下頁圖)


COUT
S0
S1
S2
S3
I6
I7
I8
I5
I9
A0
B0
CIN
A1
B1
A2
B2
B3
A3

(b) Given a structurally hashed AIG, find a sequence of ABC command(s) to covert it to a logic network with node function expressed in sum-of-products (SOP).

>logic (就一個)