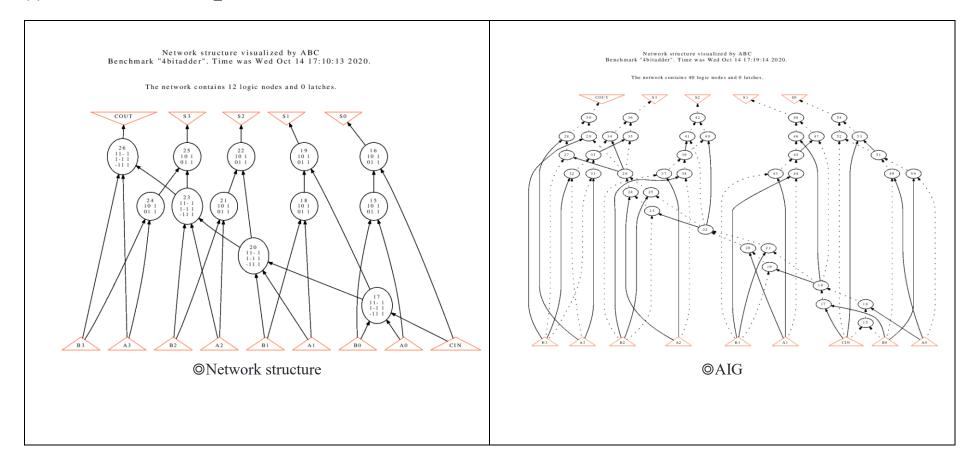
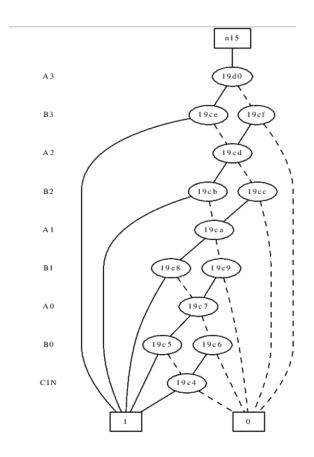
1. [Using ABC] (10%)

(a) Use **BLIF** manual to create a BLIF file representing a four-bit adder.

```
4bitadder.blif
1.model 4bitadder
2.inputs A3 A2 A1 A0 B3 B2 B1 B0 CIN
3 .outputs COUT S3 S2 S1 S0
4 .subckt fulladder a=A0 b=B0 cin=CIN
                                          s=S0 cout=CARRY1
5.subckt fulladder a=A1 b=B1 cin=CARRY1 s=S1 cout=CARRY2
6.subckt fulladder a=A2 b=B2 cin=CARRY2 s=S2 cout=CARRY3
7.subckt fulladder a=A3 b=B3 cin=CARRY3 s=S3 cout=COUT
8 .end
10 .model fulladder
11 .inputs a b cin
12 .outputs s cout
13 .names a b k
14 10 1
15 01 1
16 .names k cin s
17 10 1
18 01 1
19 .names a b cin cout
20 11- 1
21 1-1 1
22 -11 1
23 .end
```

(b) Results of show and show_bdd.:



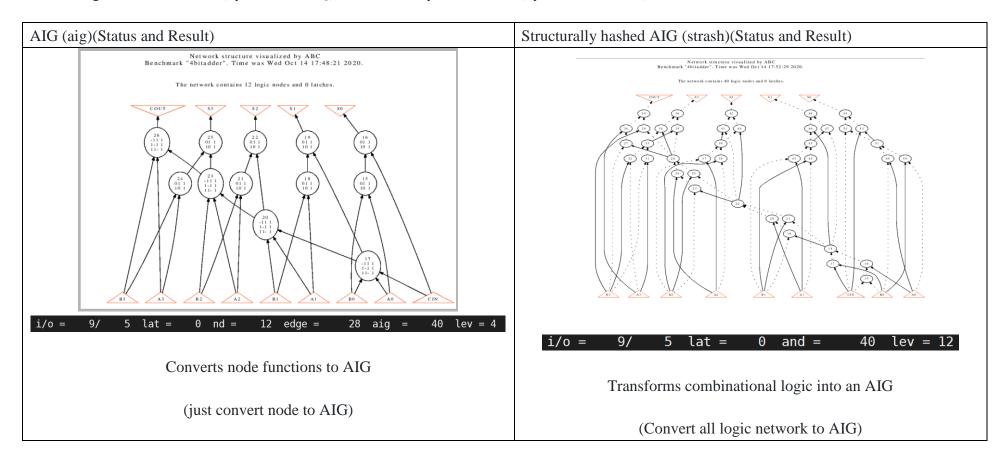


©BDD

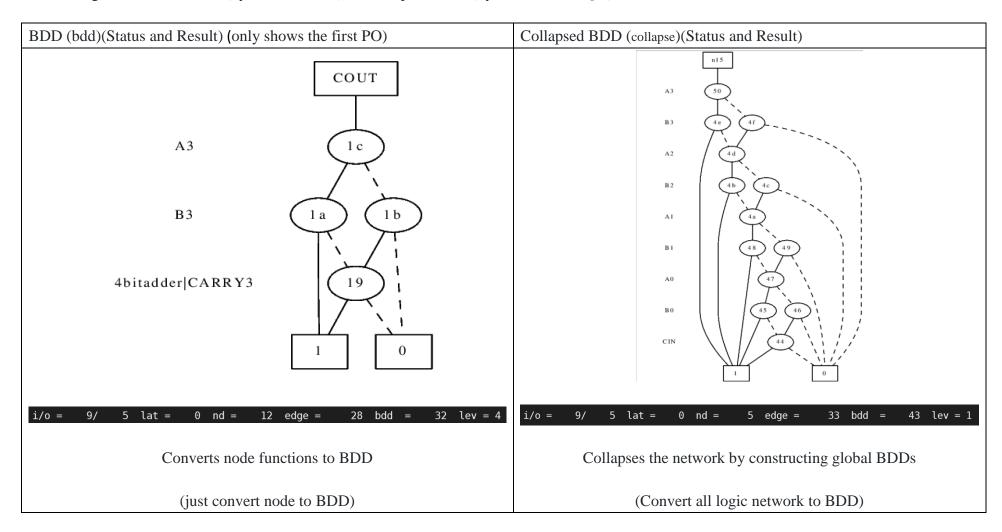
2. [ABC Boolean Function Representations] (10%)

In ABC there are different ways to represent Boolean functions.

- (a) Compare the following differences with the four-bit adder example.
 - 1. logic network in AIG (by command aig) vs. structurally hashed AIG (by command strash)



2. logic network in BDD (by command bdd) vs. collapsed BDD (by command collapse)



(b) Given a structurally hashed AIG, find a sequence of ABC command(s) to covert it to a logic network with node function expressed in sum-of-products (SOP).

Use command logic to transforms an AIG into a logic network with SOPs.

abc 08> read lsv/pa1/4bitadder.blif Hierarchy reader flattened 4 instances of logic boxes and left 0 black boxes. abc 09> strash abc 10> logic

> Network structure visualized by ABC Benchmark "4bitadder". Time was Wed Oct 14 19:05:25 2020.

> > The network contains 40 logic nodes and 0 latches.

