Logic Design and Verification PA1-2

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2 以本次作業的 four-bit adder (ADDER4.blif) 為例

2-(a)-1

`aig` 指令後的`print_stats`:

```
i/o =  9/  5  lat =  0  nd =  8  edge =  24  aig  =  52  lev = 4
```

`strash` 後的 `print_stats`:

```
i/o =  9/  5  lat =  0  and =  44  lev = 13
```

2-(a)-2

`bdd` 後的`print_stats`:

```
i/o =  9/  5  lat =  0  nd =  8  edge =  24  bdd  =  28  lev = 4
```

`collapse` 後的`print_stats`:

```
i/o =  9/  5  lat =  0  nd =  5  edge =  33  bdd  =  43  lev = 1
```

2-(b)

`logic` 指令可將 AIG 轉回 SOP 的形式。