R09943091 電子一 陳威旭

HW1 part2

- a.
 - 1.
 - 2.

b.

A sequence of ABC command: logic

Then type show, you can see the SOP with each node on the picture.

Before logic picture can see in part_1:

After logic:

Network structure visualized by ABC Benchmark "4bit_adder". Time was Wed Oct 14 23:50:54 2020.

The network contains 43 logic nodes and 0 latches.

