CS 250 Spring 2017 Homework 09
Due 11:58pm Wednesday, April 05, 2017
Submit your typewritten file in PDF format to Blackboard.

1. If a cache is big enough for the 90/10 Rule to apply, and the cache is 10 times faster than main memory, what does Amdahl's Law predict for the overall speedup from using this cache?
$$\frac{1}{(1-0.9)+\left(\frac{0.9}{10}\right)} = 5.3$$

2. How many direct-mapped cache organizations are possible given 32-bit byte addressing for programmers, word-addressed physical memory, 4-byte words, and a 17-bit tag?
Assuming an offset field of 1 bit.
14 bit Index field (32-17-1), 2^{14} possible cache organizations.

3. The i-cache (instruction cache) for a 32-bit RISC processor is direct-mapped with an offset field of 4 bits. Assume the cache is cold. Soon, the processor will fetch its first instruction at address 0x00400000.
    a. What is the best assumption about the size(s) of instructions for this processor? Why is it almost certain that the processor is designed this way?
    32 because RISC accepts fixed length instructions.

    b. How many 32-bit instructions can a block in this i-cache (instruction cache) hold?
    16

    c. Assume that the program loaded into memory starting at address 0x00400000 is pure straight line code. This means that this program is one, giant basic block of code, who knows how long, that fits within the available memory. Describe the hit and miss behavior of this i-cache (instruction cache) as the processor fetches the first four instructions of the program. State the type(s) of miss(es) that occur. Carefully consider how the address of the first instruction affects the number of hits and misses.

    The first instruction is a Compulsory miss because there is no data currently stored in the Cache. The next three instructions are a hit because there are all offsets on the same block.

    d. Now the program is loaded into memory starting at address 0x00400008. What is the hit/miss behavior and miss type(s) for the first four instructions? What happens afterwards?
    The behavior is the same as if loaded at 0x00400000. The block can contain 16 instructions so all four instructions can fit in the same block. There will be a Compulsory miss on the first instruction, but the other three will be hits.

    e. Expressed as a percentage, what is the overall hit rate of the straight line program? Remember, the program is many instructions long.
    6.25%

f. Now the program contains more than just straight line code. It has been re-written to have straight line code plus the occasional if-then-else statement. The program looks like this around an if-then-else statement (based Figure 9.2 in our textbook).

High level program	Assembly code			Basic Block
statement ;		instrs. for statement	; straight line (SL) instructions	1
if (cond.) {		instr. for condition	; 1 instruction evaluates condition	1
		branch to else	; EXIT the SL basic block	1
then_part		instrs. for then_part	; section of SL, a basic block	2
		…	; remaining then_part SL instrs.	2
} else {		branch to next_stmt	; EXIT the SL "then" basic block	2
else_part	else:	instrs. for else_part	; TARGET, else_part basic block	3
}		…	; remaining else_part SL instrs.	3
next_stmt ;	done:	instrs. for next_stmt	; TARGET, fall-through from else_part continues SL	3

Assume that the address of any given assembly instruction (machine instruction) in the assembly code is equally likely to correspond to any one of the 4 possible word offsets (w_offset) within an i-cache block. This means that the execution trace of the program can exit straight line code when executing any instruction word in a cache block.

Just for cache blocks containing a branch instruction, what is the average hit rate expressed as a percentage?

For simplicity in analyzing the situation for this question, assume (1) that any cache block contains at most one branch instruction (just one chance for the program execution trace to exit the block early) and (2) if a cache block contains a branch instruction, then it does not also contain a target instruction (a way back for the program execution trace to get back into the block after exiting because of the branch).

3%

g. In part (f), the inclusion of if-then-else in the original program, which was only straight line code, worsened the hit rate for the i-cache. Now imagine adding loops to the program of part (f). Will the $\mathbf{_{hit}}$ rate further worsen, stay the same, or improve? Using the program instruction execution trace concept, explain the reasoning behind your prediction of the effect of loops on hit rate.
Worsen because looping causes more misses.

h. The i-cache of this question has been designed with 4-word blocks. Think of i-cache operation in the event of a cache miss as an opportunity to perform instruction execution trace prediction. As compared to an i-cache design alternative where the block holds only one word, a 4-word-block design embodies its designer's vote for which type of execution trace prediction: no prediction, predict default_next, predict not default_next? Pick your answer and then explain why it is the correct choice. Default_next because no prediction would use 1-word blocks and not default_next would not benefit from a 4-word-block.

i. Cache misses can be categorized into three groups: compulsory miss, capacity miss, and conflict miss. In question part (g) program loops were introduced. Which miss type(s) can occur in the program with loops that are not possible for the program with only straight line code and if-then-else constructs?

   Conflict misses because the program is going back to a cache location that could have been overwritten.

4. A faster replacement algorithm for an associate cache improves which term or factor of the average memory access time equation?
   $(1 - r)C_m$ will be improved because the replacement algorithm is only used when a Miss occurs, so the Cost of a Miss will decrease if the replacement algorithm is faster.