CS 250 Spring 2017 Homework 11

Due 11:58pm Thursday, April 20, 2017

Submit your typewritten file in PDF format to Blackboard.

1. A serial interface operates at a throughput of 10 million bits per second and requires 100 microseconds to configure (prepare) a packet of bits to be transmitted regardless of the size of the packet.
   a. What is the effective throughput, expressed first in packets/second and then in bits/second, for this interface for an infinite series of identically-sized packets for sizes 1 bit, 100 bits, 10^4 bits, and 10^6 bits? Express answers rounded to 6 significant digits.

      1 bit = 10,000 packets/second, 10,000 bits/second
      100 bit = 10,000 packets/second, 1,000,000 bits/second
      10^4 bit = 1,000 packets/second, 10,000,000 bits/second
      10^6 bit = 10 packets/second, 10,000,000 bits/second

   b. What is being amortized?

      Creating packets

2. How many simultaneous transfers can occur over a crossbar witching fabric of N inputs and M outputs?

   N x M transfers

3. Assume that a RISC processor takes two microseconds to execute each instruction and an I/O device can wait at most 1 millisecond before its interrupt is serviced. What is the maximum number of instructions that can be executed with interrupts disabled?

   1 millisecond = 1000 microseconds / 2 microseconds = 500 operations – 1 operation to service the interrupt = 499 operations.

4. Suppose a user installs ten devices that all perform DMA into a single computer and attempts to operate the devices simultaneously. What components of the computer might become a bottleneck?

   The MMU will become a bottleneck because both the I/O devices and the CPU are accessing main memory at the same time.

5. A user invokes an app that writes a file. The app displays a progress bar that shows how much of the file has been written. Just as the progress bar reaches 50%, the power fails and the computer crashes. When the power is restored and the computer rebooted, the user discovers that less than 20% of the file was actually written. Why did the app report 50%?

The app had requested 50% of the file to be written but the I/O device hadn't completed the request yet.

6. A user invokes an app that writes a file. The app displays a progress bar that shows how much of the file has been written. The progress bar has been advancing quickly, but just as the progress bar reaches 99%, the progress bar seems to freeze, then after a delay the bar show 100%, then disappears, and the app GUI moves on to another phase of activity. What might explain why the progress bar seemed to freeze at 99% for a time before reporting 100%?

   The app had finished requesting the data to be written but the data hadn't actually been written yet.

7. Discuss the advantages of multiplexing with respect to buses. What are the two major disadvantages? Which of these two disadvantages is minimized, even rendered moot, by Moore's Law?
   Advantages would be supporting more busses and the ability to execute a fetch/store operation at the same time. Disadvantages would be the possibility of missing a transmission and the overhead cost of multiplexing the bus. The overhead cost would come down overtime by Moore's Law because the overhead can be made faster with better hardware.

8. What are the two types of bus error?
   Address conflict and Unassigned address.

9. Run a system info command on your computer, and use its output to find at least three different buses that your computer contains. For each bus, (1) describe in specific detail the physical hardware from which it would be constructed, (2) name the units within your computer that are connected to the bus (if any) and the external units (if any) typically connected to the bus, (3) classify the bus as serial or parallel, (4) state if the bus is proprietary or if is it standard and when was its standard specification released and what entity released the spec, and (5) state how the bus addresses are configured (manually per I/O device, by hardwiring on the bus, or automatically), and (6) state for automatically configured buses, state whether the bus is hot-pluggable or not. The web, especially Wikipedia, can be a helpful resource.

   USB
   1. The controller is usually implemented on the motherboard. Devices are connected to a four pin port (excluding Type-C and 3.1) which is usually a part of a hub.
   2. Mouse, Keyboard, Flash Drive
   3. Serial
   4. The USB 3.1 specification was released on July 31, 2013.
   5. Addresses are assigned by the OS on attachment.
   6. Hot-pluggable.

   SATA

1. Includes two cables, one for power and one for data. Data has 7 pins, where four implement the serial communication. These data cables are connected to the SATA controller from.
2. Hard Drive, Optical Drive
3. Serial
4. Revision 3.3 was released in February 2016
5. Addresses are assigned by the OS on attachment.
6. Hot-pluggable.

PCI-E.

1. PCI always connects to the motherboard, the CPU can only support so many PCI lanes. PCI-E ports are inset rectangular ports that a component is loaded into. The ports are x4, x8, x16 where x4 accepts smaller components than x16. Components can also connect to an external power bus for more power.
2. Graphics Card
3. Parallel
4. The 3.1 specification was released in November 2014
5. Addresses are assigned by the OS on attachment.
6. Hot-pluggable.