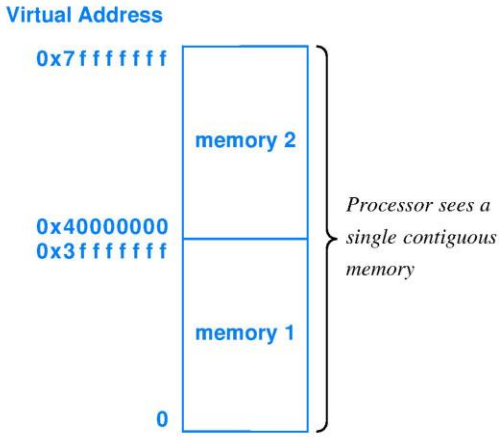
CS 250 Spring 2017 Homework 10
Due 11:58pm Wednesday, April 12, 2017
Submit your typewritten file in PDF format to Blackboard.

1. Consider the circuit for a 4 KB, 2-way set associative write-back cache using LRU replacement and having 16-byte blocks that is for a computer using 32-bit addresses that address 32-bit words in main memory.
    a. What are the sizes of the tag, index, and block offset fields in bits?
    Offset field is 2 bits, Index field is 8 bits, Tag field is 14 bits (Set field is 8 bits).

    b. How many blocks are there in the cache?
    250 blocks (4KB / 16B)

    c. How many bytes of overhead are there in the cache? What percentage of all memory bits in the cache are overhead bits?
    There are 16 overhead bits (2Bytes) per 16 stored bytes. 2Bytes * 256 (amount of possible blocks) = 512 Bytes of overhead. 512 / 4,000 = 12.8%.

2. Given the following virtual address space



and the C program

```
char c;
char *p;
p = (char *)1073741826;
c = *p;
```

Which memory module will be referenced, and where will the referenced byte be located with the module?
1073741826 = 0x40000002, so Module 2 will be referenced and the byte will be located at 0x00000002.

3. Assuming a page size of 8 Kbytes what is the page number in hexadecimal and offset in hexadecimal for addresses 0x00000FFF, 0x00001FFF, 0x00002002, and 0xFFFFDFFD? Pad as needed with leading zeros to obtain hexadecimal representations for your answers.

```
Pg #: 0x00000000      Offset: 0x00000fff
Pg #: 0x00000000      Offset: 0x00001fff
Pg #: 0x00000001      Offset: 0x00000002
Pg #: 0x0007ffff      Offset: 0x00001ffd
```

4. Assume a virtual memory with a 13-bit address space organized into 8 pages. Physical DRAM memory implements addresses 0x000 through 0xFFF.

Page number	Page frame
0	3
1	1
2	Not present in DRAM memory
3	Not present in DRAM memory
4	2
5	Not present in DRAM memory
6	0
7	Not present in DRAM memory

In the table below. for each listed virtual address, fill in the corresponding physical address or note if a page fault would occur.

Virtual address (13 bits shown in hex with leading zero padding)	Corresponding physical address or Page fault
0x0000	0x000
0x0E90	Page fault
0x03FF	Page fault
0x0400	0x7fc

5. In Question 4 we assumed that the given page table did not change as the CPU tried to access each of the 4 virtual addresses. An actual page table would dynamically update per its design as the CPU accessed successive virtual addresses.
So, let's assume that the CPU has accessed the four virtual addresses in the table of Question 4 in the order shown, that is, in the order of reading down the column of the table. Further, let's assume that any page faults that you identified in answering Question 4 are the only page faults that occurred when the CPU accessed these four addresses in order (depending on the replacement algorithm this need not be the case). Finally, let's assume that we do not know the page replacement algorithm used by this virtual memory system design nor do we know which accesses in Question 4 were loads and which were stores. Finally, a complete page table must at least have bits for each page to indicate Valid and Dirty (other bits may be needed to support access permissions and the page replacement algorithm, but let's not worry about access permission and we do not know the replacement algorithm, so we will ignore those bit(s) as well).

Fill in the empty page table below to show its contents after the fourth access. If there is more than one possibility for a translation entry, list all possibilities. Use the following definitions for the Valid and Dirty bits: 0 = characteristic not true, 1= characteristic is true, X = table entry is correct with either a 0 or 1 for this bit, and ? = "given the limited degree of knowledge about this virtual memory system design, the value of this bit must be only one of

0 or 1 but the actual value cannot be determined.”

Page	Starts at frame physical address	Present	Dirty
0	0x000	1	X
1	0x1ff	1	X
2	0x3fe	0	0
3	0x5fd	0	0
4	0x7fc	1	X
5	0x9fb	0	0
6	0xbfa	1	X
7	0xdf9	1	0