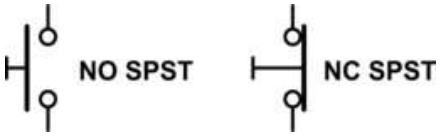
CS 250 Spring 2017 Homework 02
Due 11:58pm Wednesday, January 25, 2017
Submit your typewritten file in PDF format to Blackboard.

1. Write out the POS expression for 2-input XNOR.

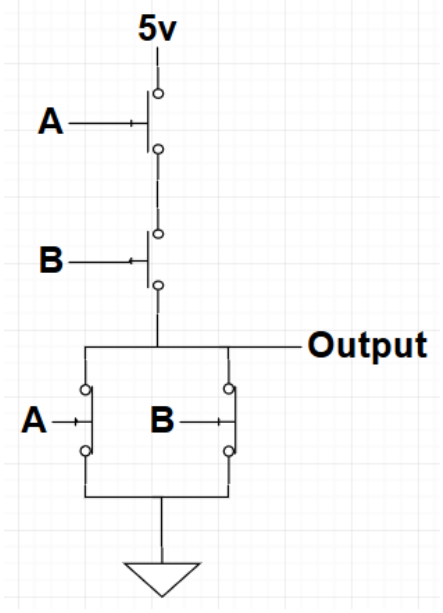
A	B	A XNOR B
0	0	1
0	1	0
1	0	0
1	1	1

$= \overline{AB} + AB$

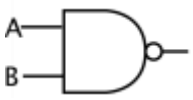
2. The normally-open (NO) SPST push button switch (same type as in the lab kit) transitions from high resistance to low resistance when pushed. The normally-closed (NC) SPST push button switch reverses this behavior. The schematic symbols for these two switches are shown here.

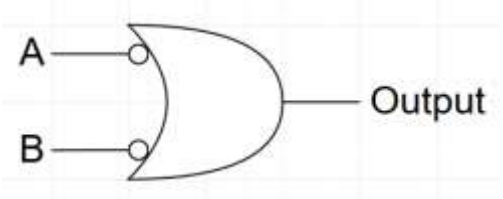


Using these two switch types, wire, and connections to +5 V and ground, draw a schematic to implement (AB)' and clearly label your inputs and output.



3. Examine the gate shown below, then draw an equivalent single gate that does not contain a NAND gate nor an AND gate.





4. The most important logic gate parameter for the prevention of error is the
    a. width of the voltage band representing logic 1
    b. width of the voltage band representing logic 0
    c. power supply voltage
    d. gap between the highest logic 1 voltage and the lowest logic 0 voltage
    e. gap between the lowest logic 1 voltage and the highest logic 0 voltage

    E

5. A revised version of the Lab01 take home problem has been assigned. You are to rebuild the XNOR gate using only 2-input NAND gates, with one difference. Because you are practicing to qualify to compete in the Olympic Games, you must operate the circuit using the tip of an epée while in a fencing pose as shown at the web link and standing far enough away from your breadboard that by stretching you can only just reach the circuit with the tip of the epée.
    See https://en.wikipedia.org/wiki/Épée - /media/File:Fencing_epee_valid_surfaces.svg to become familiar with an epée.
    Can you re-build the XNOR circuit using fewer than 5 two-input NAND gates as was done originally in lab? If yes, describe why and how.

    No, in order to implement an XNOR circuit in NAND logic you have to have at least 5 NAND gates. This is because it takes four NAND gates to implement XOR in NAND logic, adding another NAND gate is required which brings the total up to five.