CS 250 Spring 2017 - Lab 02
Due in lab Jan. 31 through Feb. 03, 2017
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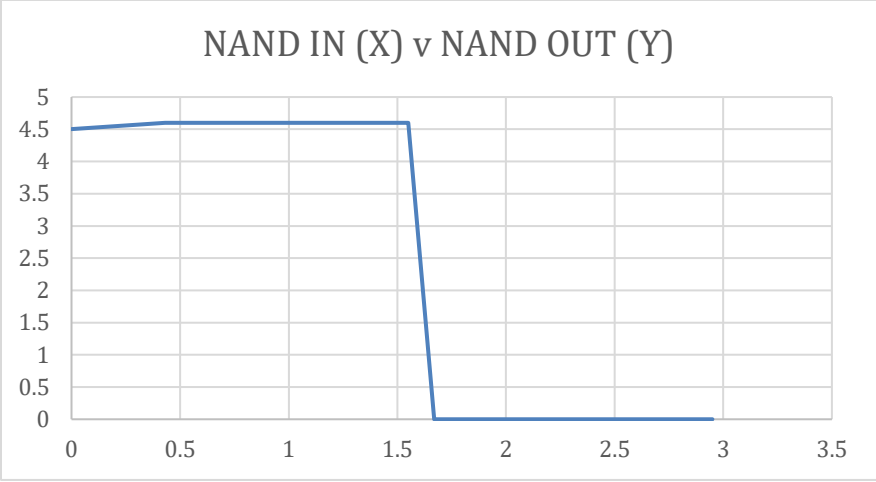
In-Lab Experiments, Part 1

1. [5 points] As you turn the potentiometer knob to move terminal 2 from terminal 1 (connected to the 470 ohm resistor) towards terminal 3 (connected to ground), the Analog Input voltage linearly changes from 5 volts to 0 volts. Carefully observe Red LED1 and Red LED2. Describe the behavior of the two LEDs with respect to the action of the potentiometer.

   When you start out, with the pot all the way clockwise the NAND output is high so LED2 is turned on. LED1 is completely off. As you turn the pot counter-clockwise, you'll get to a point (about midway through the pot rotation) where LED2, from NAND, turns off. At this point LED1 has a slight glow. As you continue rotating counter-clockwise, LED1 gets brighter and brighter until you run out of rotations.

2. [15 points] Plot your data point pairs (NAND1 input voltage from potentiometer, NAND1 output voltage). Comment on the shape of the function NAND1 output voltage = f(NAND1 input voltage from potentiometer) displayed in your plot. Does f show digital behavior?

NAND IN	NAND Out
0	4.5
0.43	4.6
1.13	4.6
1.55	4.6
1.67	0
1.78	0
1.94	0
2.21	0
2.9	0
2.95	0



3. [10 points] NAND1 produces a high quality (more digital) output signal despite the many poor quality logic 0 and logic 1 voltages and voltages within the gap between the valid logic levels that the potentiometer voltage provides to NAND1. Why is the behavior of NAND1 to a poor quality input so important to computer circuits comprised of billions of transistors?

   If a NAND gate didn't produce a high quality output, then the other gates depending on that signal would be compromised. This would produce a large amount of errors and make the circuits unreliable.

In-Lab Experiments, Part 2

4. [10 points] Fill in the following table with your observations from Part 2 experiments.

Clock source	Typical number of bounces observed from LEDs A, B, C, D (74163 output)
Clock 1 (potentiometer)	Oscillates between 4 leds on and 1 one led one when rotating.
Clock 2 (SPST switch)	2-3, holding the button for longer periods generates bounces
Clock 3 (SPDT switch)	Too many to count, would cycle all the way through the count
Clock 4 or 5 (SR Q or Q')	0, no visible bounces

Take Home Questions

5. [10 points] Why is skipping consecutive numbers in the output of the 74163 counter an indication of switch bounce?

   A bounce would cause numbers to be skipped because it acts like very fast clock signals.

6. [10 points] If the 74163 advances the count by 1 for a single Clock 3 input this means that the switch did not bounce that time. True or False? Explain your answer.

   False, the bounce could have been small enough to not toggle between HIGH and LOW.

7. [10 points] What is the mathematical expression for the number of bounces observed by the 74163 chip circuitry as contrasted with the number of bounces that your eyes are capable or observing by examining the 74163 output using LEDs A, B, C, and D?

8. [10 points] How does the memory capability of the SR latch (NAND2 and NAND3) transform the bouncing SPDT switch input into a bounce-free output?

   The SR latch requires that the opposite of S be applied to R in order to change state, so if S is the same logic value as R, in the case of a bounce, there is no change applied.

9. [20 points, 5 points each of the four parts] Design a logic circuit to compute the function F(A,B,C) = 1 when at least two of the A, B, and C inputs are logic value 1. Show the following for F(A,B,C): (1) truth table, (2) K-Map, (3) minimized Boolean expressions in both SOP and POS form, (4) draw schematics for both the SOP and POS expressions using NAND and NOR gates, respectively.

A	B	C	F(A,B,C)
0	0	0	0
0	0	1	0
0	1	0	0
0	**1**	**1**	**1**
1	0	0	0
1	**0**	**1**	**1**
1	**1**	**0**	**1**
1	**1**	**1**	**1**

1

AB C	00	01	11	10
0	0	0	**1**	0
1	0	**1**	**1**	**1**

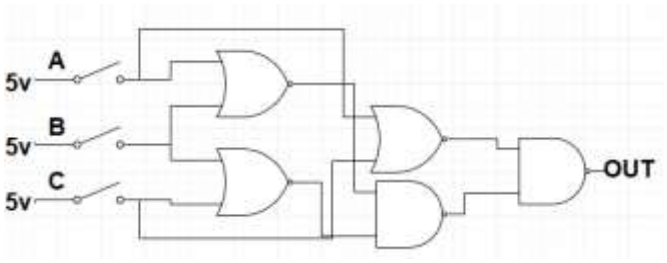
2

3

SOP: $BC + CA + AB$

POS: $(B + C) \cdot (C + A) \cdot (A + B)$

POS



SOP