Communication Circuits Design – 2018-19, semester II

Lab 4 - Week 12

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Phase locked loop

The objective of this lab is to become familiar with Phase Locked loop (PLL). PLL has a built-in phase detector and a voltage control oscillator (VCO). PLL takes in a unknown frequency signal to which it locks and then outputs this signal from its VCO. Due to the advancement of semiconductor technology, PLL is available in integrated circuit (IC) form. For this lab CD4046B IC will be used.

Theory recap.

PLL is very useful circuit block widely used in radio frequency (RF) and wireless communication. The key operation of a PLL is to detect phase difference (frequency difference) between two signals. The phase difference is then feed into a low pass filter which converts the phase difference to voltage difference. Finally, the voltage is fed to VCO input to generate frequency with same phase of the other signal. As a result, phase (frequency) of the both signals are locked. The basic block diagram of a PLL is shown in Figure 1. We will explore VCO part of the PLL (CD4046B) to generate different frequency.

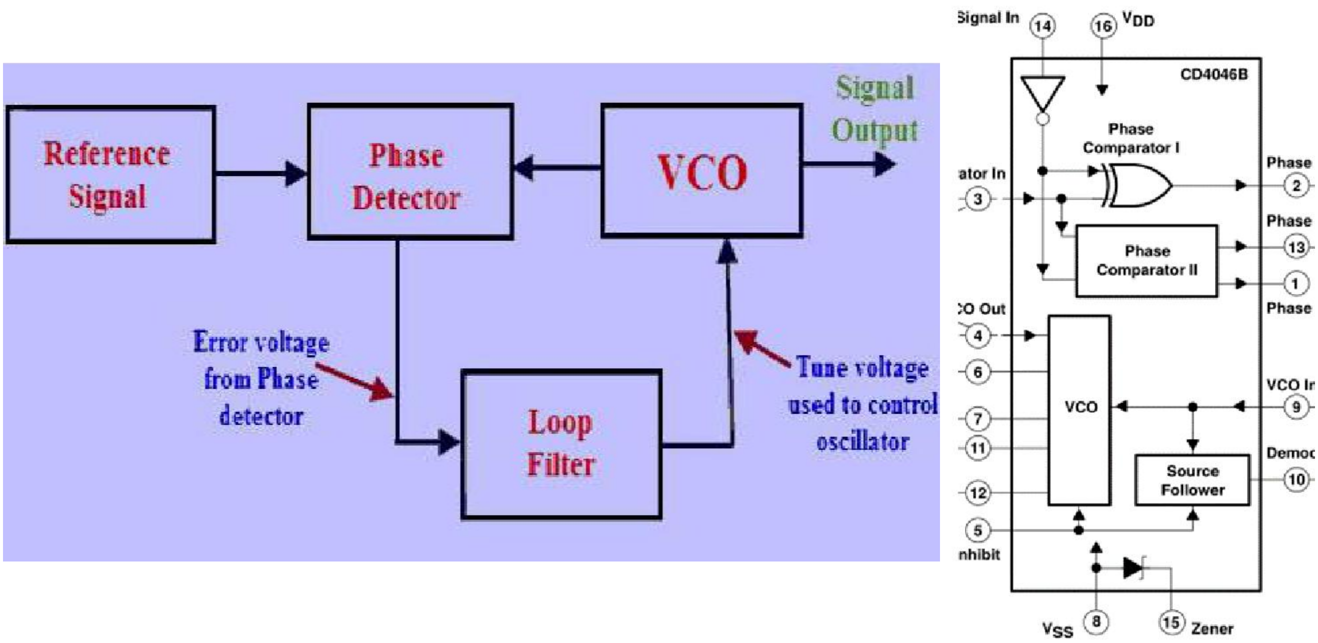


Figure 1 Basic block diagram of Phase Locked Loop [1,2]

Pinout of the CD4046B

CD4046B is a 16 pins IC. To use the CD4046's VCO, we will be using few of its 16 pins. The pinout of the CD4046B is shown on figure 2. The VCO of the IC CD4046B requires one capacitor C1 and one resistor R1. C1 and R1 determines the frequency range of the VCO. Equation below can be used to calculate the frequency of the VCO.

$$f = \frac{1}{C1 \times R1} \quad (1)$$

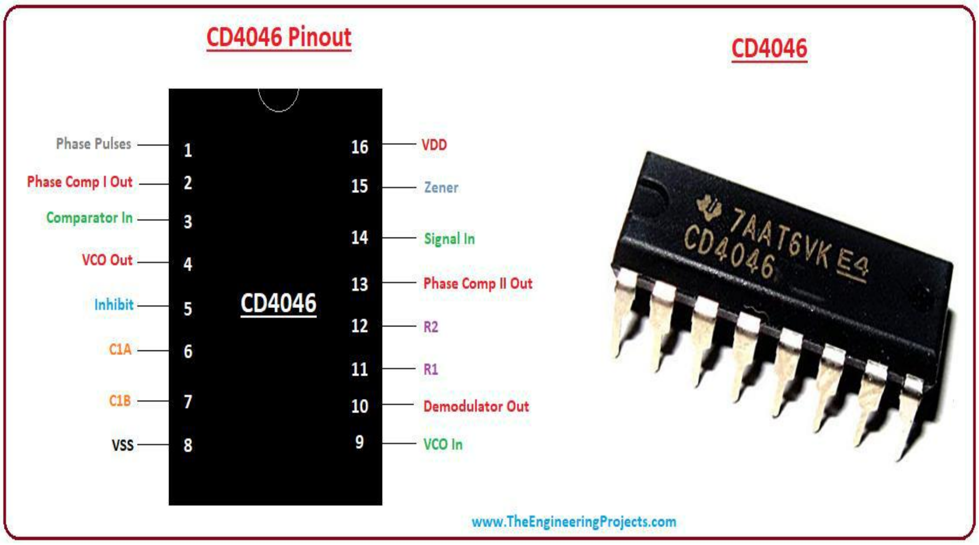


Figure 2: Figure 2 Pinout of CD4046B

Components required

- Capacitor ceramic C1 = 10nF ×1
- Resistor R1 = 100k ×1
- Resistor R2 = 2.2k ×1
- Potentiometer R3 = 10k ×1

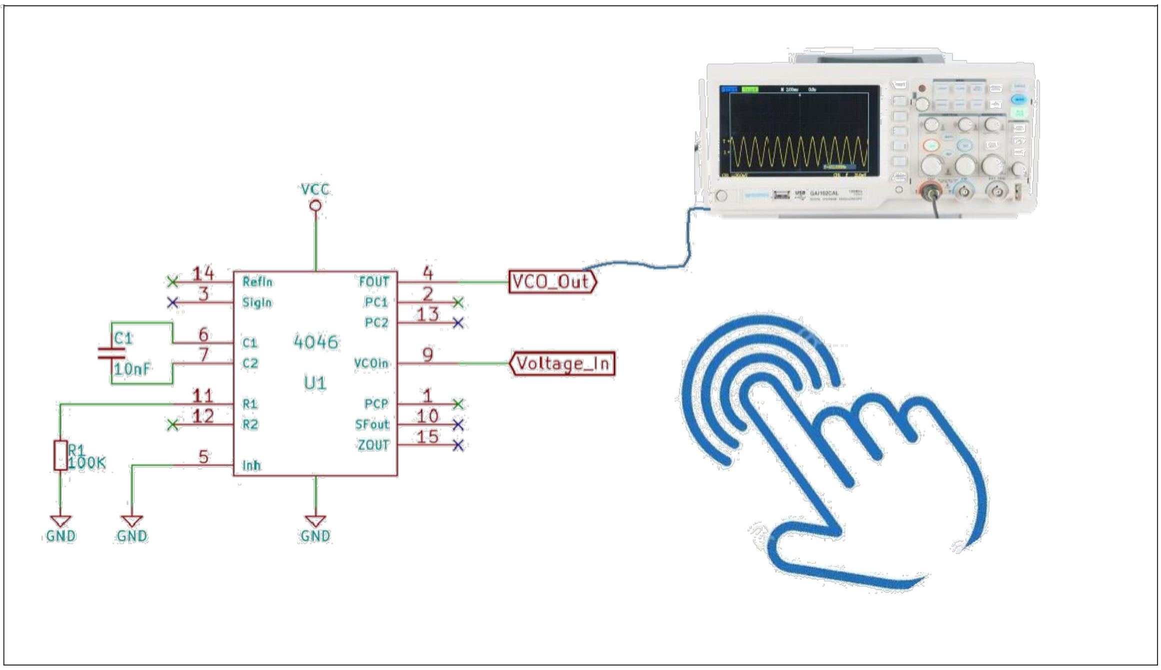
Practical procedure.

1. Using equation 1 calculate the f value by multiplying C1 and R1, write it down
2. Use DC power supply, set it to 5V. Connect +5 to pin 16 (V_{DD})and 0V to pin 8 (V_{SS}). Do not turn the DC supply ON.
3. VCO has an inhibit pin, pin 5 which allows to electronically turn on or off the output voltage power supply. Connect pin 5 to ground.
4. Connect capacitor C1 (10nF) between pin 6 and 7
5. Connect resistor R1 (100k) pin 11 to GND
6. Now turn ON the DC power supply
7. Connect pin4, the output of the VCO to an oscilloscope and observe the frequency and write it down.
8. Now touch pin 9, the input of the VCO, explain what change you can observe on the oscilloscope?

1. $f = \frac{1}{R_1 C_1} = \frac{1}{10\text{nF}\times 100\text{k}\Omega} = 1000Hz$

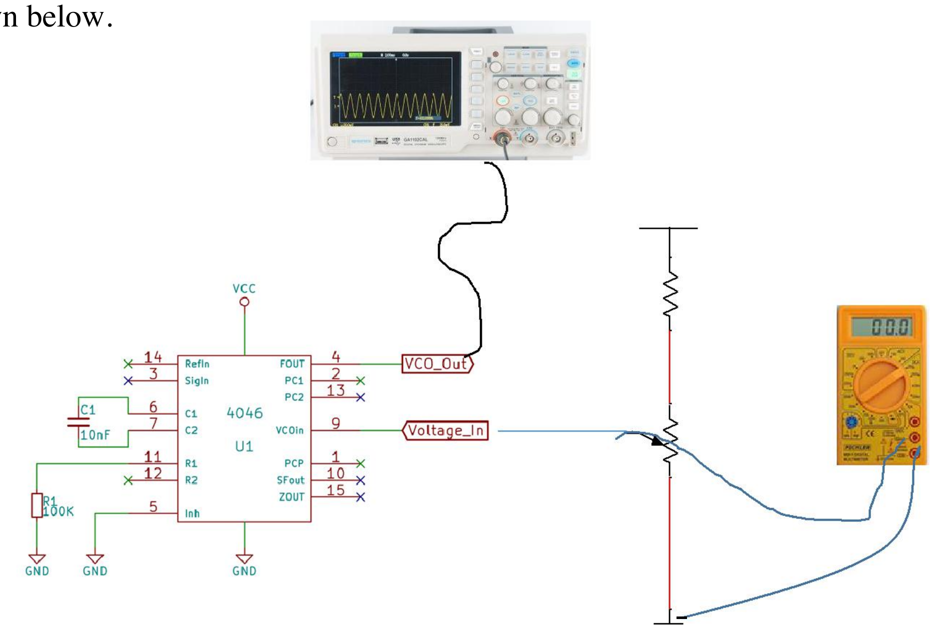
7. The frequency range is from 537Hz to 621Hz

8. After we connect our hand to pin9, the frequency would fluctuate theoretically as our finger is as a resistance, which is not stable according to the wetness of the finger and how large the force we use to connect the pin with our hand. **The result from the experiment shows that the fluctuate do not change a lot (range is from 529Hz to 623Hz) because the connection between our hand and pin is stable and the resistance of my finger is very high, which is close to the air. So, there would be no significant changes.**



Now we will put some variable voltage in pin 9 as shown below:

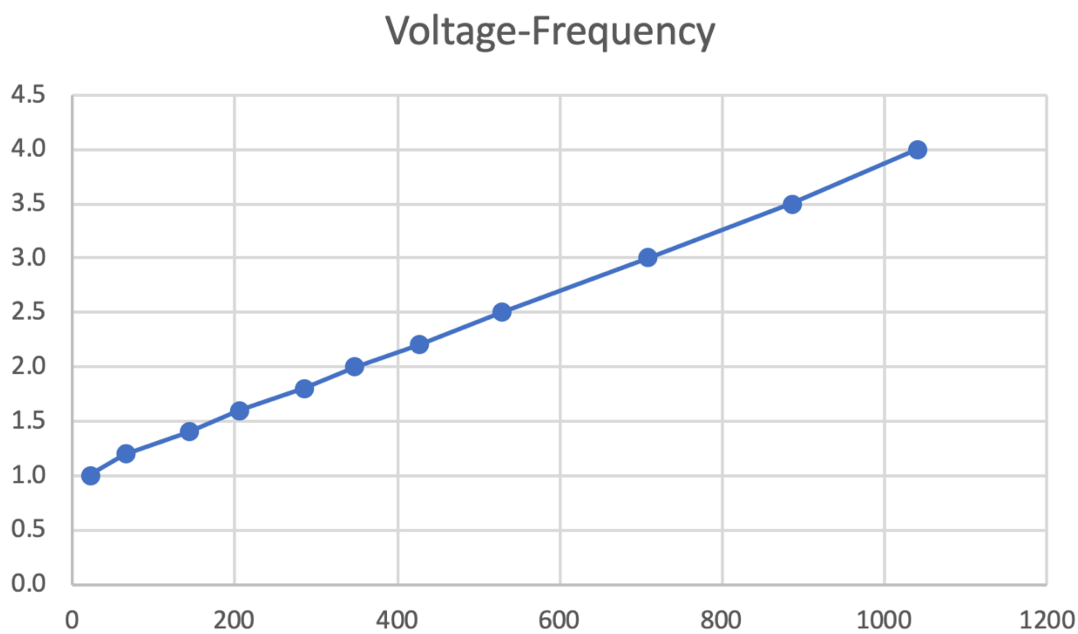
9. Use R2 and R3 in series, connect the middle pin of the potentiometer to pin 9 as shown below.



10. Change the potentiometer slowly and observe the voltage on the voltmeter and frequency change on the oscilloscope and write it down table below.

Voltage (V)	Frequency
1.0	21.3Hz
1.2	64.4Hz
1.4	142.7 Hz
1.6	205.8 Hz
1.8	285.1 Hz
2.0	346.6 Hz
2.2	425.5 Hz
2.5	527.4 Hz
3.0	707.9 Hz
3.5	885.5 Hz
4.0	1040 Hz

11. Draw a graph of voltage vs frequency from your observation from task 10 table. Discuss the maximum frequency range of the VCO. Does it match with calculated frequency from equation 1? Does the frequency changes linearly with the voltage change?



from the line chart, we can find that the approximate linear trendline of it is:

$$V = 0.0029f + 0.9865$$

The maximum frequency range of voltage is 0-4V. So the maximum frequency range is up to 1000 Hz.

Form the result it is close but a little different from the theoretical result as the it is only 40Hz higher than the theoretical one. The difference is trivial.

From the graph, we can see the obvious argument in its favor is that it is learner, or at least close to leaner approximately. The frequency is 1040Hz when the voltage is 4V, which is close to the theoretical result.