Problem Set 6

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1a)

Op	Cycles
or	4
and	4
sub	4
sw	4
lw	5
add	4
bne	3
Total	28

1b)

For a single-cycle datapath, each instruction must use all 5 stages. This makes the total time 11ns. The clock rate is then $\frac{1}{11e-9} = 90.0MHz$.

1c)

In a 5-stage pipeline, each instruction will use all 5 stages and each stage will be the length of the longest stage. This means the clock cycle is $5ns = 200Mhz$.

1d)

Assuming full forwarding, the only command to cause a delay will be the LW, which will cause a delay of 2 cycles. Thus, the total number of cycles will be 13.

2a)

In a pipelined architecture, the clock cycle time is the same as the longest stage. For this example, this would be the MEM stage, which is 600ps.

2b)

In a single-cycle datapath, the clock cycle time is the sum of all 5 stages = 1500ps.

2c)

In a pipelined processor, the latency of an r-type instruction is $600 \times 5 = 3000ps$ since even an r-type needs to go through all 5 stages. In a single-cycle processor, the latency of an r-type instruction is the same as the clock cycle time, 1500ps, since each instruction executes in 1 cycle.

3)

$\frac{1}{\frac{70 \times 1e6}{n_{stages}}} = 4e-9$ thus $n_{stages} = 3.57$. This means 4 stages will be needed, as fractional stages are impossible.

4a)

With no forwarding, and each instruction being dependent on the previous, two bubbles will need to be inserted after each instruction to ensure correct operations. This is because each instruction cannot execute until the previous has finished the WB stage.

Figure 1: Cycle table for problem 4a.

CYCLE	IF	ID	EX	MEM	WB
1	or				
2	bubble	or			
3	bubble	bubble	or		
4	or	bubble	bubble	or	
5	bubble	or	bubble	bubble	or
6	bubble	bubble	or	bubble	bubble
7	or	bubble	bubble	or	bubble
8		or	bubble	bubble	or
9			or	bubble	bubble
10				or	bubble
11					or
12					
13					
14					

4b)

With full forwarding, all data hazards for sequential r-type instructions are alleviated.

Figure 2: Cycle table for problem 4b.

CYCLE	IF	ID	EX	MEM	WB
1	or				
2	or	or			
3	or	or	or		
4		or	or	or	
5			or	or	or
6				or	or
7					or
8					
9					
10					
11					
12					
13					
14					

4c)

$\frac{11}{7} = 1.57$

5)

With full forwarding, LW and the branch assumption can cause bubbles. In this example, the branch will be assumed not taken. However, upon execution the comparison will be found to be equal and the branch will need to be taken.

Figure 3: Cycle table for problem 5.

CYCLE	IF	ID	EX	MEM	WB
1	or				
2	addi	or			
3	sll	addi	or		
4	beq	sll	addi	or	
5	lw	beq	sll	addi	or
6	bubble	lw	beq	sll	addi
7	sw	bubble	lw	beq	sll
8	addi	bubble	bubble	bubble	beq
9		addi	bubble	bubble	bubble
10			addi	bubble	bubble
11				addi	bubble
12					addi
13					
14					

6)

With full forwarding, the only instruction that will result in a delay is the LW instruction. A LW followed by an instruction that requires the loaded word will need to be delayed by one cycle.

Figure 4: Cycle table for problem 6.

CYCLE	IF	ID	EX	MEM	WB
1	addi				
2	addi	addi			
3	sll	addi	addi		
4	add	sll	addi	addi	
5	lw	add	sll	addi	addi
6	bubble	lw	add	sll	addi
7	sw	bubble	lw	add	sll
8	add	sw	bubble	lw	add
9		add	sw	bubble	lw
10			add	sw	bubble
11				add	sw
12					add
13					
14					