

Problem Set 10

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1a)

- A: $time = 5s + \frac{3145728 \text{ bytes} \times s^{-1}}{5120s} = 619.4s$
- B: $time = 4s + \frac{3145728 \text{ bytes} \times s^{-1}}{3072s} = 1028s$

1b)

$$5 + \frac{N}{5120} = 4 + \frac{N}{3072} \quad (1)$$

$$\frac{N}{5120} = -1 + \frac{N}{3072} \quad (2)$$

$$N = -5120 + \frac{5N}{3} \quad (3)$$

$$\frac{-2N}{3} = -5120 \quad (4)$$

$$N = 7680 \text{ bytes} \quad (5)$$

2a)

With a device generating 150 requests per second, and each request requiring 12,000 cycles to handle, the total number of cycles per second spent handling interrupts and processing requests will be:

$$150 \frac{\text{requests}}{\text{second}} \times 12,000 \text{ cycles} = 1,800,000 \frac{\text{cycles}}{\text{second}}.$$

2b)

For just a polling scenario, the CPU will use 500 cycles once every .5ms.

$$\frac{1 \text{ poll}}{5e^{-4} \text{ seconds}} \times 500 \text{ cycles} = 1,000,000 \frac{\text{cycles}}{\text{second}}$$

2c)

$$\frac{1_{poll}}{N_{seconds}} \times (500 + 12000) \text{ cycles} = 1800000, \text{ thus } N = .0069\text{s or } 6.9\text{ms.}$$

3a)

Memory-mapping implements I/O by allowing peripheral device access through the same address bus as normal memory. This has the benefit of not needing special I/O commands; rather the same load instruction can be used to access system memory or an external device, at the cost of decreasing the amount of addresses reserved for memory. Consequently, CPUs are allowed to remain simpler, cheaper, smaller, and faster without the overhead of the extra logic.

3b)

DMA is an improvement over CPU programmed I/O because it requires fewer active CPU cycles to complete memory access. CPU Programmed I/O requires the CPU to be active during the entire read or write sequence. With DMA, a device is allowed to directly access memory and bypass the need for the CPU to act as middleman. In this scheme the CPU is only need at the beginning and end of an access, the rest of the time it is free to perform other functions.