

# Problem Set 8

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Justin Ely

605.411 Foundations of Computer Architecture

31 October, 2016

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## 1a)

To select chip b, the chip selector bit will be 0, so cell 74 stays as 74, and  $0xD132 = 53554$ .

```
li $t1, 74
li $t2, 53554
```

## 1b)

To select chip a, the chip selector bit will be 1, so cell 43 becomes 2147483691, and  $0xB133 = 45363$ .

```
li $t1, 2147483691
li $t2 45363
```

## 2a)

The time for each read will be  $5ns + 25ns = 30ns$ . The amount of data transferred per read will be 64 bits = 8 bytes. Thus the bandwidth will be  $\frac{8bytes}{30e-9seconds} = 2.667e8 \frac{bytes}{second}$  or .266 Gigbytes per second.

## 2b)

LW retrieves 1 word, which is 32 bits or 4 bytes. Thus, LW would need only 1 read which would take a minimum of 30ns. The LW, in practice, would take more time depending on the architecture of the pipeline and the time required for the other 4 stages.

**3)**

- a) 1
- b) 1
- c) 0
- d) 0

**4a)**

**Presuming you mean problem 3 instead of problem 1:**

This is best characterized by a latch as the output changes in response to the input, not in response to a clock.

**4b)**

This is best characterized by S-R, as the output state can be set or reset based on which input is triggered, and remembers that state when the inputs are turned off.

**5Ia)**

$15e9 = \frac{4 \times N}{10e-9} = 37.5$ . Thus, 38 memory banks would be required to provide 15 billion bytes per second.

**5Ib)**

22 bits are required to address the bytes on a given chip, and 4 bits are required to select the chip, so the total number of bits is 26.

**5IIa)**

Longest stage = 20ns, so clock rate =  $\frac{1}{20e-9} = .05GHz$ .

**5IIb)**

Width = word size = 32 bits = 4 bytes. Depth =  $\frac{2^{30}}{4} = 268435456 = 2^{28}$  bytes.

### 5IIc)

This pipeline would need 1 new instruction every 20 ns, for a bandwidth of  $\frac{4}{20e-9} = 2e8 \frac{\text{bytes}}{\text{second}}$ . However, DDRAM transfers twice the data with each read, so the bandwidth could be halved to  $1e8 \frac{\text{bytes}}{\text{second}}$ .

### 5IIId)

$128e6 \frac{\text{bytes}}{\text{second}} = \frac{\text{width}}{\text{cycletime}} = \frac{4 \frac{\text{bytes}}{\text{cycle}}}{\text{cycletime}}$ . Thus the cycle time is  $3.125e-8$  seconds/cycle.

### 6)

| CMD             | Big-Endian | Little-Endian |
|-----------------|------------|---------------|
| lw \$t0,0(\$t1) | 0x89875543 | 0x43558789    |
| lh \$t0,0(\$t1) | 0x00008987 | 0x87890000    |
| lb \$t0,3(\$t1) | 0x00000043 | 0x43000000    |
| lh \$t0,2(\$t1) | 0x00005543 | 0x43550000    |