Problem Set 3

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605.411 Foundations of Computer Architecture

20 September, 2016

1)

For this, and following solutions, (n) represents column n in the table. This is used to reduce errors in typing when doing arithmetic with derived columns.

1	2	3	4	5	6	7
a	b	(ab)'	A'(3)	B'(3)	((4)(5))'	((6)(6))'
0	0	1	1	1	0	1
1	0	1	0	1	1	0
0	1	1	1	0	1	0
1	1	0	1	1	0	1

The result (column 7) has the same truth table as a XNOR gate.

2)

ROW	A	B	C	Y	Maxterm	Minterm
0	0	0	0	1		A'B'C'
1	0	0	1	0	A + B + C'	
2	0	1	0	1		A'BC'
3	0	1	1	1		A'BC
4	1	0	0	0	A' + B + C	
5	1	0	1	0	A' + B + C'	
6	1	1	0	1		ABC'
7	1	1	1	0	A' + B' + C'	

3a)

1	2	3	4	5	6	7
a	b	c	ab	bc	ac	(4) + (5) + (6)
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	1
1	0	0	0	0	0	0
1	0	1	0	0	1	1
1	1	0	1	0	0	1
1	1	1	1	1	1	1

3b)

AB + BC + AC

4)

1	2	3	4	5	6
a	b	ab	a'b'	(3) + (4)	(5)'
0	0	0	1	1	0
1	0	0	0	0	1
0	1	0	0	0	1
1	1	1	0	1	0

This logic circuit can be replaced with a single XOR gate.

5)

From the circuit diagram shown:

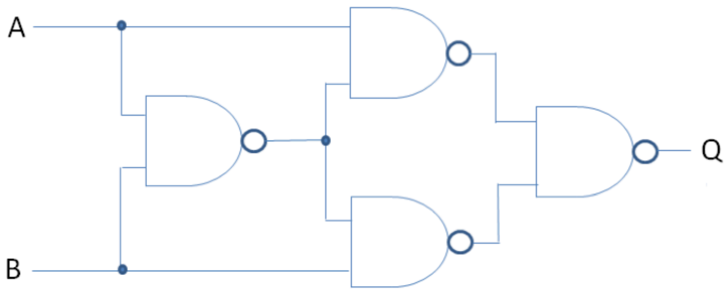
1. $o_3 = S`I_2$
2. $o_2 = SI_3 + S`I_1$
3. $o_1 = I_2S + S`I_0$
4. $o_0 = I_1S$

Thus, by setting $S = 1$, and $I_3, I_2, I_1, I_0 = 1011$, the circuit comes out as: $o_3, o_2, o_1, o_0 = 0101$.

6)

From problem 1, column 6 is the same output as an XOR gate, and has been constructed with only NAND gates. Thus, the circuit would look like that shown in the figure below.

Figure 1: Circuit diagram for an XOR gate using only NAND gates.



7)

1	2	3	4	5	6	7	8	9
A	B	A‘B	AB‘	A‘B + AB’	C	(5)‘C	C’(5)	R
0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	1	0	1
0	1	1	0	1	0	0	1	1
0	1	1	0	1	1	0	0	0
1	0	0	1	1	0	0	1	1
1	0	0	1	1	1	0	0	0
1	1	0	0	0	0	0	0	0
1	1	0	0	0	1	1	0	1

8a)

A	B	C	Z	Minterm
0	0	0	1	A’B’C’
0	0	1	0	A’B’C
0	1	0	0	A’BC’
0	1	1	1	A’BC
1	0	0	1	AB’C’
1	0	1	0	AB’C
1	1	0	0	ABC’
1	1	1	1	ABC

The function Z is then built of the minterms on rows where Z=1: $Z = A'B'C' + A'BC + AB'C' + ABC$.

8b)

$$
\begin{aligned}
Z &= A'B'C' + A'BC + AB'C' + ABC && (1)\\
Z &= B'C'(A' + A) + BC(A' + A) && (2)\\
Z &= B'C' + BC && (3)
\end{aligned}
$$