Problem Set 3

Justin Ely

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1)

1	2	3	4	5	6	7
a	b	(ab)'	A'(3)	B'(3)	((4)(5))'	((6)(6))'
0	0	1	1	1	0	1
1	0	1	0	1	1	0
0	1	1	1	0	1	0
1	1	0	1	1	0	1

The result (last column) has the same truth table as a XNOR gate.

2)

3a)

1	2	3	4	5	6	7
a	b	c	ab	bc	ac	(4) + (5) + (6)
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	1
1	0	0	0	0	0	0
1	0	1	0	0	1	1
1	1	0	1	0	0	1
1	1	1	1	1	1	1

3b)

AB + BC + AC

4)

1	2	3	4	5	6
a	b	ab	a'b'	(3) + (4)	(5)'
0	0	0	1	1	0
1	0	0	0	0	1
0	1	0	0	0	1
1	1	1	0	1	0

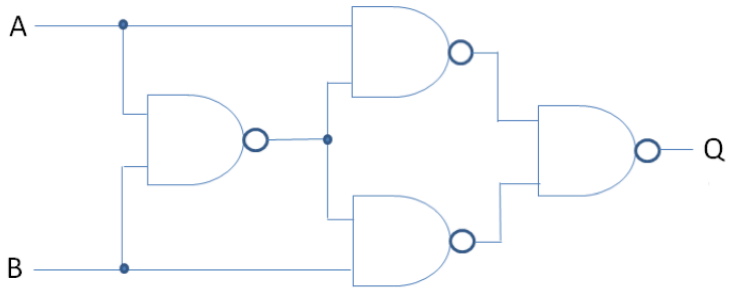
This logic circuit can be replaced with a single XOR gate.

5)

6)

From problem 1, column 6 is the same output as an XOR gate, and has been constructed with only NAND gates. Thus, the circuit would look like that shown in the figure below.

Figure 1: Circuit diagram for an XOR gate using only NAND gates.



7)

8)