Changseob **Lee**

Spice Developer · Modeling Expert

1-1, Samsungjeonja-ro, Hwaseong, Rep. of KOREA

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Research Interests

Decision Making, Adaptable Optimization, Device Circuit Modeling, Digital Integrated Circuit Design

Work Experience

Samsung Electronics. Co., Ltd.

Hwaseong, S.Korea

SPICE Group, Samsung Foundry

Feb. 2018 - Present

Project Experience

FDSOI(Fully Depleted Silicon-On-Insulator) SPICE Modeling

Samsung Foundry

LN18FDSOI, LN28FDSOI SPICE Developer

Oct. 2019 - Present

- Analyzed pre &post simulation on circuit designer's view de-embedding metal and contact access
- Described characteristics of silicon (I-V, C-V) depending on temperature dependency
- Implemented fixed corner and statistical model based on Monte Carlo method

MBCFET(Multi-Bridge-Channel FET) SPICE Modeling

Samsung Foundry

3GAE process SPICE Developer

Oct. 2018 - Oct.2019

- Developed device behavior and process design kit structure establishing initial library structure for advanced process
- Implemented characteristics of threshold voltage, saturation & linear current based on silicon measurement

FinFET SPICE Modeling

Samsung Foundry

7nm Process SPICE Developer

Oct. 2018 - Dec. 2019

- Analyzed FinFET layout structure based on process assumption and design rule manual
- Implemented characteristics of devices according to several threshold voltages

Tool development (Silicon Data Filtering & Modeling)

Samsung Foundry

Tool Developer

Mar. 2020 - Oct.2021

- Integrated silicon handling method of SPICE team, device team and Fab team analyzing codes (HSPICE, Python, Tcl, Perl)
- Reduced turn around time by 90% integrating scripts and methodologies of specialized teams
- Awarded Samsung Foundry Work Smart Fair 2021.Q2, which is given to individuals who enhanced dramatic work efficiency

Samsung Unified Infra Structure Development

Samsung Foundry

Tool Developer

Mar. 2019 - Mar.2020

- Standardized the structure of the SPICE model library by specifying differences in process objectives.
- Encapsulation of HSPICE, Python, Verilog-A and Perl improving inter-departmental compatibility.
- Awarded Design Platform team project, which is given to a promising group that designs innovative architecture

PMIC, CMOS Image Sensor, Pannel and Mobile DDI SPICE Modeling

Samsung Foundry

BCD1370, BCD1340HP, APM906M, BCD90GP, LF6, LF6S, LL1313GP, LL1318GPS, LL13A13P SPICE Developer

Oct. 2018 - Present

- Developed schottky diode, zener diode, iso-bjt, resistor, and varactor considering improved design rule manual
- Reformed model equation, library structure, and TEG structure to describe scaled physics' behavior
- Described device model with my own equation based on newly updated design rule of BEOL

MOS Varactor Model Equation Development

Samsung Foundry

The 2nd Author

Oct.2020

- Implemented applied logistic regression model on varactor devices improving conventional verilog-A model
- Increased hspice simulation performance by 3x, reduced memory usage by 20%
- Published Samsung Foundry Symposium, where influential research of the year is published

Publications

Samsung Foundry Symposium

- [Published] Jooyoung Song, **Changseob Lee**, "Samsung Foundry MOS Varactor Model Equation Development", 2021
- [In Prepartion] **Changseob Lee**, Jooyoung Song, Sungjae Lee, "Application of the Ridge Regression in MOSFET modeling and Parameter Extraction", 2022

Education

SKKU(SungKyunKwan University) *Suwon, S.Korea*

B.S. in Semiconductor Systems Engineering *Mar. 2012 - Feb. 2018*

- Relevant Courses: Analog IC Design, Digital IC Design, Semiconductor Integration Engineering, Physical Electronics, Display Device and Process, Electromagnetism, Probability Random Process, Honor Calculus

Scholarships & Awards

2021.Jun **Individual Award**, Samsung Foundry Work Smart Fair 2021.Q2 *Samsung Foundry*

2020.Mar **Project Award**, Developed Samsung Unified Modeling Infra Structure *Samsung Foundry*

2012-2017 **Samsung Semiconductor Scholarship**, Full Tuition (6 Semesters) *B.S in SKKU*

2012-2017 **Samsung Electronics Scholarship**, Additional Full Tuition fee (7 Semesters) *B.S in SKKU*

Hosted Seminars

HSPICE Optimizer Algorithm *Samsung Foundry*

to Samsung Foundry *Sep.2022*

- Lectured how to apply theoretical algorithms to CMOS extraction mathematically
- Introduced Levenberg-Marquardt algorithm, Combination of Steepest Decent method and the Gauss-Newton method

Ridge Regression, Linear Algebra *Samsung Foundry*

to Samsung Foundry *Apr.2022*

- Analyzed geometric, statistical interpretation of Ridge Regression and how to apply in SPICE Model
- Lectured how pre-consider numerical conditions that circuit designers will face

De-embedding Methodology *Samsung Foundry*

to ST Micronics, France *Aug.2022-Oct.2022*

- Mathematically described silicon trend, which is caused by uncertainty of circuit designers
- Introduced how to completely de-embed metal, contact access effect in SOI process

SPICE Modeling Methodology *Samsung Foundry*

to SSIR(Samgsung Semiconductor India Research), India *Jun.2019*

- Introduced model equations, library structure, and usage of internal SPICE modeling tools
- Clarified equation's limitation and risky points of auto-optimization

Photo Diode Model Implement Methodology *Samsung Foundry*

to Samsung Foundry *Jun.2019*

- Built model equation, model &Silicon correlation Verification, and Netlist Library
- Initially introduced how to apply luminance properties to conventional model computation

Field Training in Samsung Electronics

2022.Sep **Digital Integrated Circuit Design (40hr)**, Memory, Multiplier&Shifter, Adder, Desgin methodology, Timing

2021.Oct **Regression Analysis (36hr)**, Model Validation and Diagnostics, Ridge&LASSO Regression, Projection

2021.Sep **Mathematical Statistics (24 hr)**, Method of Estimation, Confidence Interval, Normal Distribution

2021.Nov **Structured Big Data Analysis (32hr)**, Ensemble Algorithms,Linear Regression

2020.Jun **Python (32 hr)**, scikit-learn (K-Nearest Neighbor, Decision Tree, PCA, mRMR, DTW)

2019.Mar **Machine Learning (32 hr)**, Dimension Reduction Algorithm, Support Vector Machine

2019.Jun **FinFET Layout (32hr)**, Layout drawing, LVS & DRC verification

2018.Aug **Process Design Kit (12hr)**, Connection of SPICE, PEX, CDS, DRC, LVS Teams

2018.Jun **Analog Integrated Circuit Design (32hr)**, OP-Amplifier Circuits, Output Stages and Power Amplifiers

2018.Jun **Device/Process (64hr)**, Advanced transistor, Future Devices

Skills

Programming Python, Perl, Git, Verilog-A, C/C++, Matlab, LINUX, Excel VBA, Tcl

Tools HSPICE, Spectre, BSIMProPlus, IC-CAP, Cadence tools, Spotfire