ECE 441
Single Bus Step Cycle Practice Questions

MOVE.L $7000,$B100

0	0	Size	DESTINATION	SOURCE
0	0	1 0	0 0 1 1 1 1	1 1 1 0 0 0

23F8 7000 0000B100

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	$FC2$	$FC1$	$FC0$
1	A000	23F8	1	0	0	0	1	1	0
2	A002	7000	1	0	0	0	1	1	0
3	A004	0000	1	0	0	0	1	1	0
4	A006	B100	1	0	0	0	1	1	0
5	7000	U	1	0	0	0	1	0	1
6	7002	U	1	0	0	0	1	0	1
7	B100	U	0	0	0	0	1	0	1
8	B102	U	0	0	0	0	1	0	1

LEA +5(A3),A2

0	1	0	0	Register	1 1 1	Effective Address
0	1	0	0	0 1 0	1 1 1	1 0 1 0 1 1

45EB 0005

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	$FC2$	$FC1$	$FC0$
1	A000	45EB	1	0	0	0	1	1	0
2	A002	0005	1	0	0	0	1	1	0

MOVE.L (A1),(A2)

0	0	Size	DESTINATION	SOURCE
0	0	1 0	0 1 0 0 1 0	0 1 0 0 0 1

2491

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	$FC2$	$FC1$	$FC0$
1	A000	2491	1	0	0	0	1	1	0
2	A100	U	1	0	0	0	1	0	1
3	A102	U	1	0	0	0	1	0	1
4	A200	U	0	0	0	0	1	0	1
5	A202	U	0	0	0	0	1	0	1

CLR.L $A000

0	1	0	0	0 0 1 0	Size	Effective Address
0	1	0	0	0 0 1 0	1 0	1 1 1 0 0 1

42B9 0000A000

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	$FC2$	$FC1$	$FC0$
1	A000	42B9	1	0	0	0	1	1	0
2	A002	0000	1	0	0	0	1	1	0
3	A004	A000	1	0	0	0	1	1	0
4	A000	42B9	1	0	0	0	1	0	1
5	A002	0000	1	0	0	0	1	0	1
6	A002	0000	0	0	0	0	1	0	1
7	A000	0000	0	0	0	0	1	0	1

ROR (A2)+

1	1	1	0	0	1	1	dr	1	1	Effective Address
1	1	1	0	0	1	1	0	1	1	0 1 0

E6DA

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	$FC2$	$FC1$	$FC0$
1	A000	E6DA	1	0	0	0	1	1	0
2	A200	U	1	0	0	0	1	0	1
3	A200	U	0	0	0	0	1	0	1

PEA -15(A2) A2 → A200 -15 → FFF1

0	1	0	0	1	0	0	0	0	1	Effective Address
0	1	0	0	1	0	0	0	0	1	1 0 1 0 1 0

486A FFF1

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	$FC2$	$FC1$	$FC0$
1	A000	486A	1	0	0	0	1	1	0
2	A002	FFF1	1	0	0	0	1	1	0
3	A6FE	A1F1	0	0	0	0	1	0	1
4	A6FC	0000	0	0	0	0	1	0	1

Calculates an effective address <ea> and pushes it onto the stack pointed to by address register A7 (the stack pointer, SP).

DISPLACEMENT : 1000 0000 XXXX XXXX (X: DISPLACEMENT INTEGER) => 1000 0010 (8002)

ADDI.L #$2,2(A2,A0)

A000
A200
\+ 2
4202

0	0	0	0	0	1	1	0	Size	Effective Address
0	0	0	0	0	1	1	0	1 0	1 1 0 0 1 0

06B2 00000002 8002

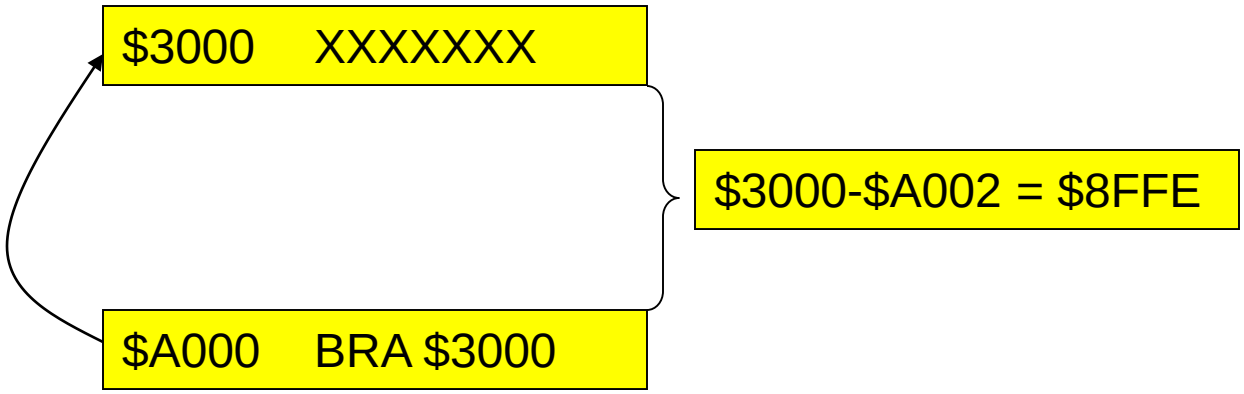
Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	$FC2$	$FC1$	$FC0$
1	A000	06B2	1	0	0	0	1	1	0
2	A002	0000	1	0	0	0	1	1	0
3	A004	0002	1	0	0	0	1	1	0
4	A006	8002	1	0	0	0	1	1	0
5	4202	U	1	0	0	0	1	0	1
6	4204	U	1	0	0	0	1	0	1
7	4204	U	0	0	0	0	1	0	1
8	4202	U	0	0	0	0	1	0	1

BRA $3000

0	1	1	0	0	0	0	0	8 BIT DISPLACEMENT
0	1	1	0	0	0	0	0	0000 0000

6000 8FFE

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	$FC2$	$FC1$	$FC0$
1	A000	6000	1	0	0	0	1	1	0
2	A002	8FFE	1	0	0	0	1	1	0



MOVEM.L (A3)+,A0/D0

0	1	0	0	1	dr	0	0	1	Sz	Effective Address
Register List Mask										
0	1	0	0	1	1	0	0	1	1	0 1 1 0 1 1
Register List Mask										

4CDB 0101

A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	**(A)+**
D0	D1	D2	D3	D4	D5	D6	D7	A0	A1	A2	A3	A4	A5	A6	A7	**-(A)**

Bus Cycle #	Address	Data	$R/\overline{W}$	$\overline{UDS}$	$\overline{LDS}$	$\overline{AS}$	$FC2$	$FC1$	$FC0$
1	A000	4CDB	1	0	0	0	1	1	0
2	A002	0101	1	0	0	0	1	1	0
3	A300	U	1	0	0	0	1	0	1
4	A302	U	1	0	0	0	1	0	1
5	A304	U	1	0	0	0	1	0	1
6	A306	U	1	0	0	0	1	0	1