Hardware Session

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Topics Overview

1. Inside a FPGA

2. Standard memory on FPGA

3. Simulation, Implementation and Debugging skill on Vivado (Ex.1 using topic 2)

4. Serial and parallel communication

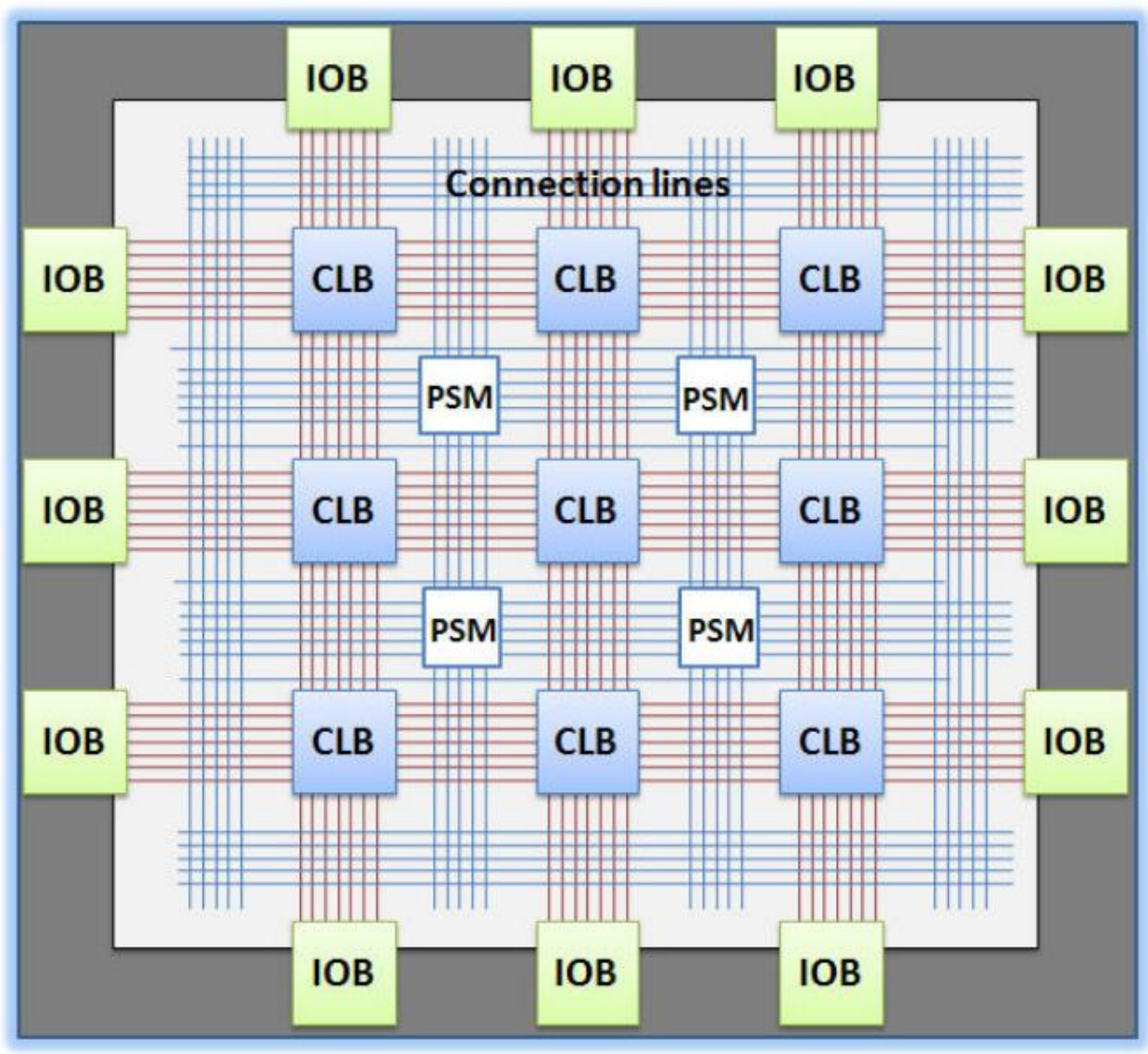
5. Image Capture and Pre-processing (EX.2)

6. How to design FPGA on Zynq

7. Schematic design for FPGA (Optional)

1. Inside a FPGA

Inside a FPGA – Reduced and simplified



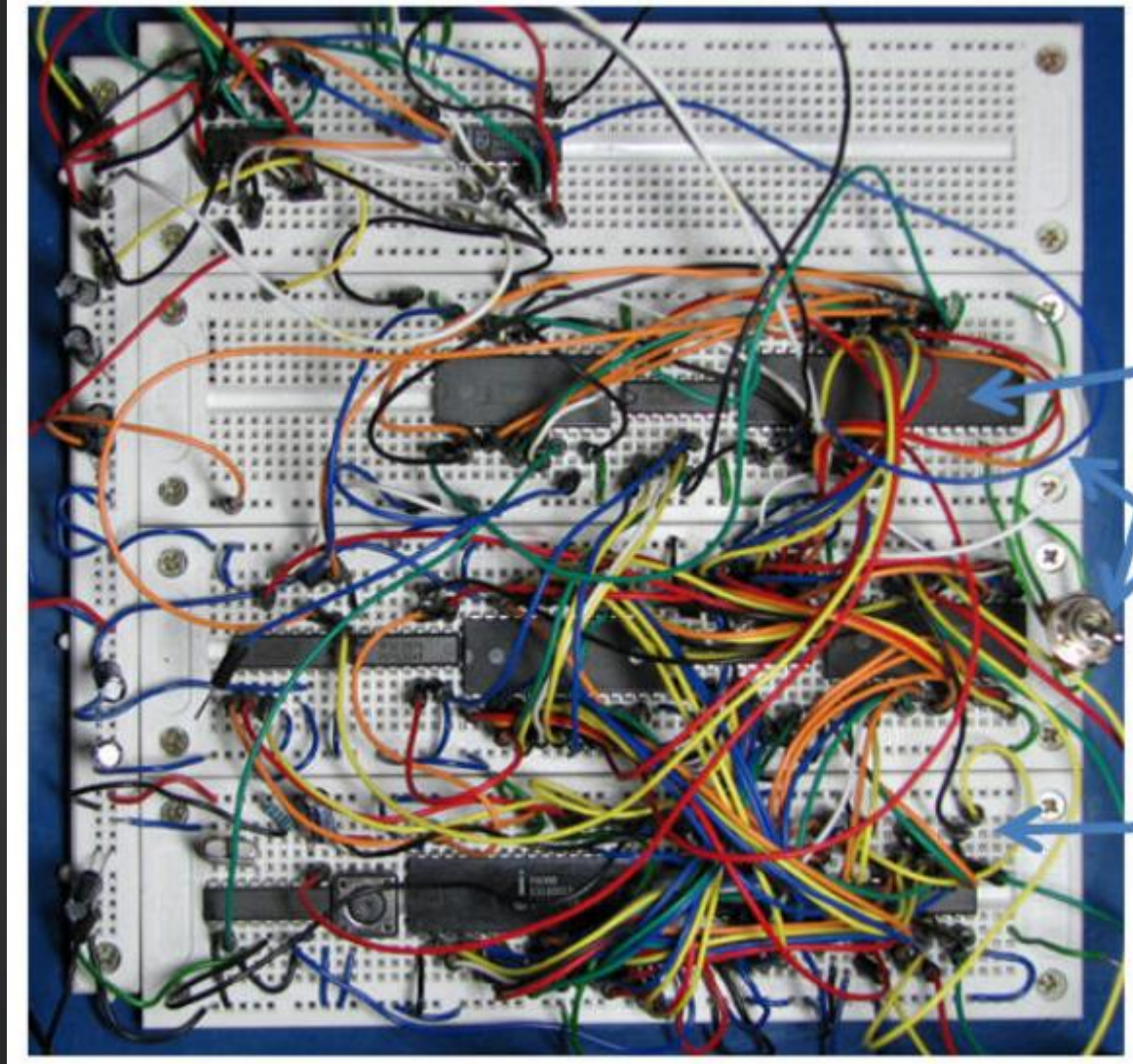
IOB
Input Output Block

CLB
Configurable
Logic Block

PSM
Programable
Switch Matrix

Connection lines
Single, Long
Double, Direct

Old "Alternative" to the FPGA



IOB

"IOB"
Input Block

CLB

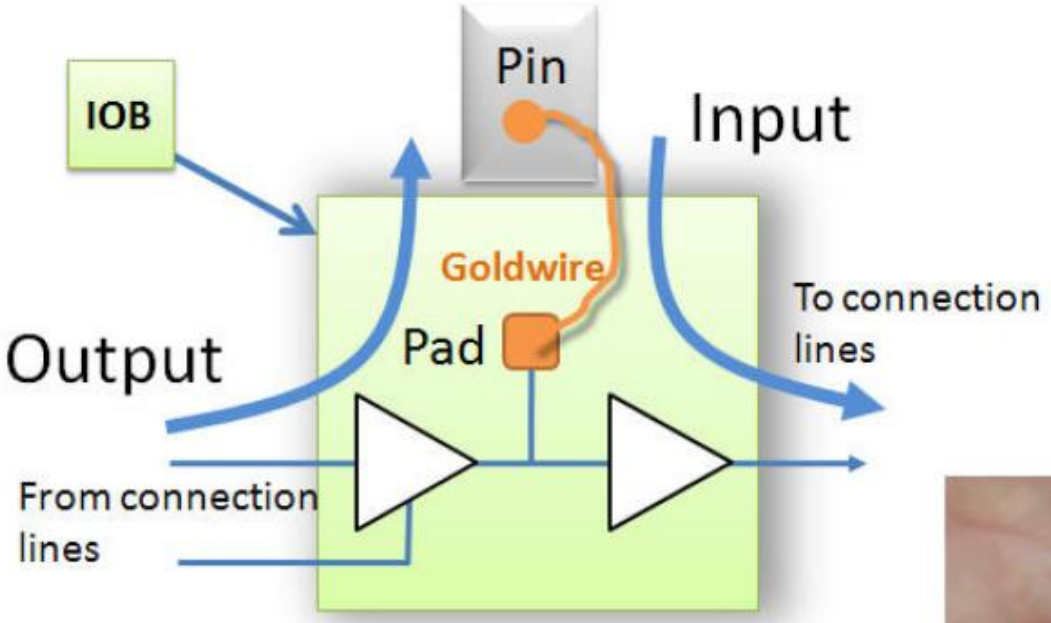
"CLB"
Non Configurable
Logic Block

PSM

"PSM"
Programable
Switch Matrix

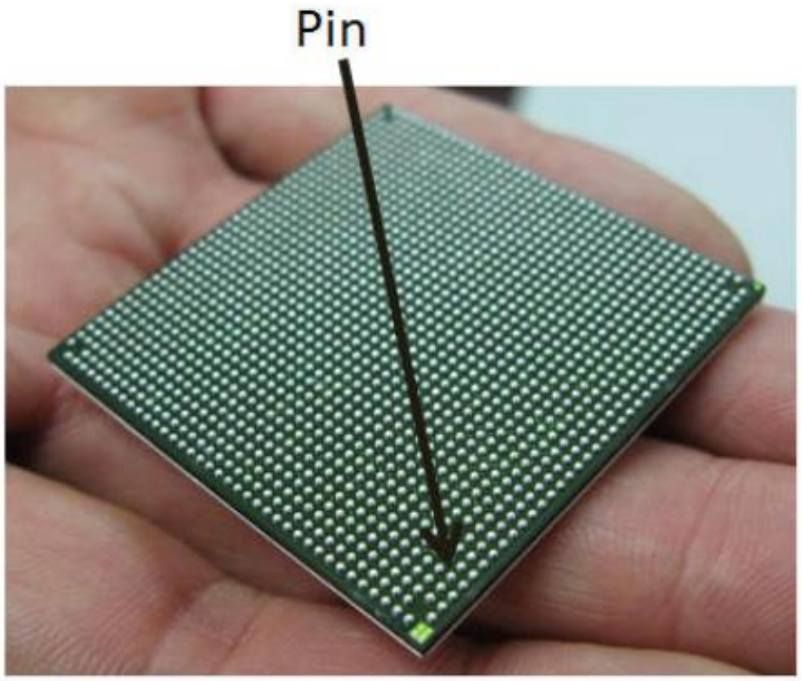
Connection lines
Single, Long
Double, Direct

I/O-Block - simplified

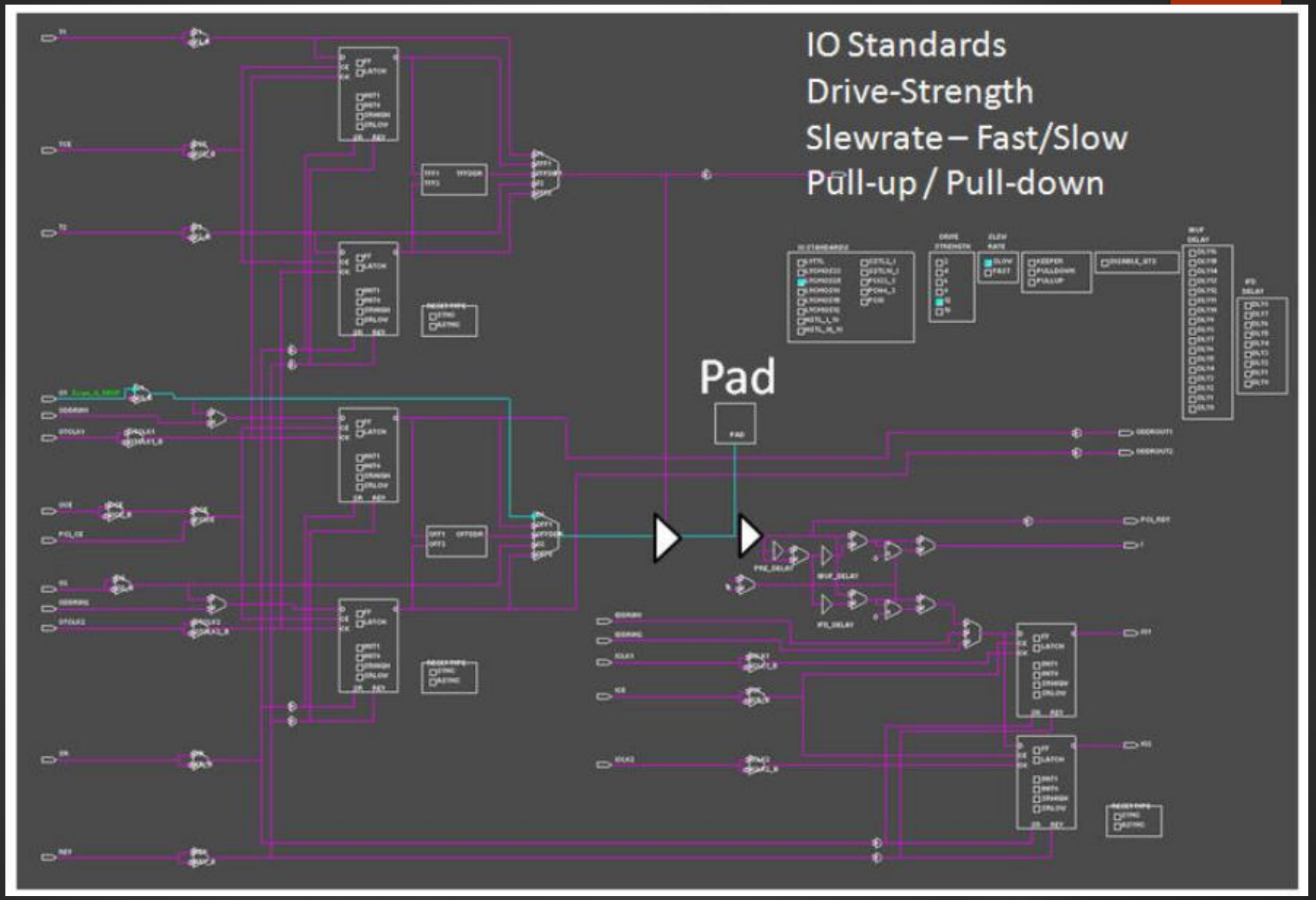


FPGAs comes in different housings
The most compact called PBGA.

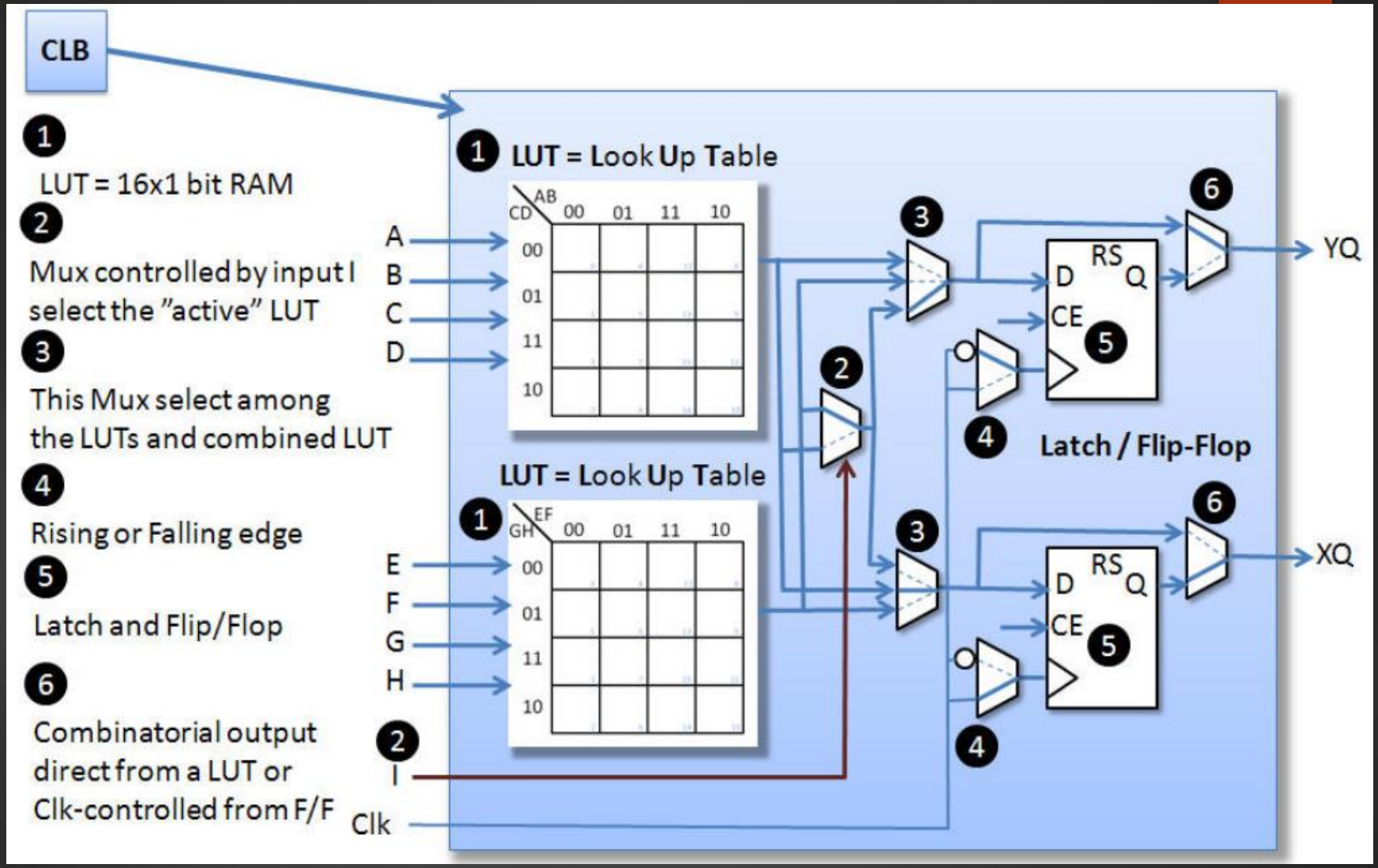
PBGA = Pin Ball Grid Array



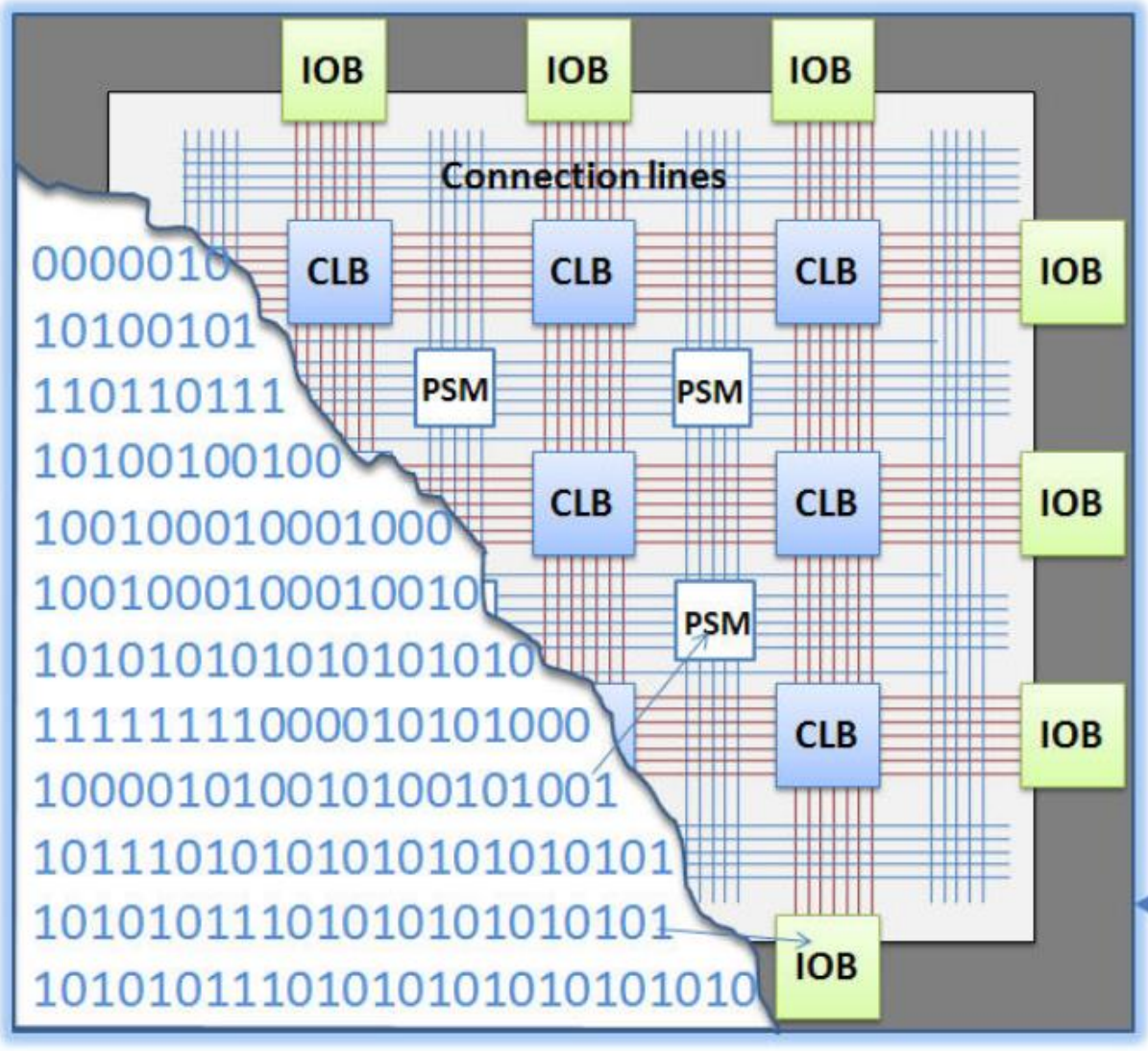
Real world I/O-Block



Configurable Logic Block - simplified



What's behind a FPGA



Most FPGAs based at Static RAM technology.

Each time the FPGA powered up must it recieve a configuration in form of 0 and 1 bits (Several millions)

It takes 16 bit to initialize a LUT but most of the bits will be used by the connection lines and PSMs

Serial Flash memory with configuration

Inside a FPGA – 100k gate - 36% used