EE3024 – Digital Signal Processing

Project – Advanced Light Intensity Indicator (ALII)

Group 18

230675D – S. V. C. H. Vithanage

230691X – N. M. S. U. Weerakoon

230700D – W. T. D. Weliwaththa

230705X – B. G. U. A. P. Wickramasinghe

230732C – W. A. K. S. Wimalasiri

Feature 01: Power Line Noise Removal (Analog Filtering Stage)

Introduction

- Unwanted electrical noise must be eliminated from the environment before the Light Dependant Resistor (LDR) output signal is sent to the Analog-to-Digital Converter (ADC) stage. 50 Hz to 100 Hz power line interference affects the LDR voltage in indoor lighting conditions and is primarily caused by:
    - AC mains supply
    - LED and CFL lamp flickering
    - Switching noise from nearby electronic devices
    - Long connecting wires acting as antennas

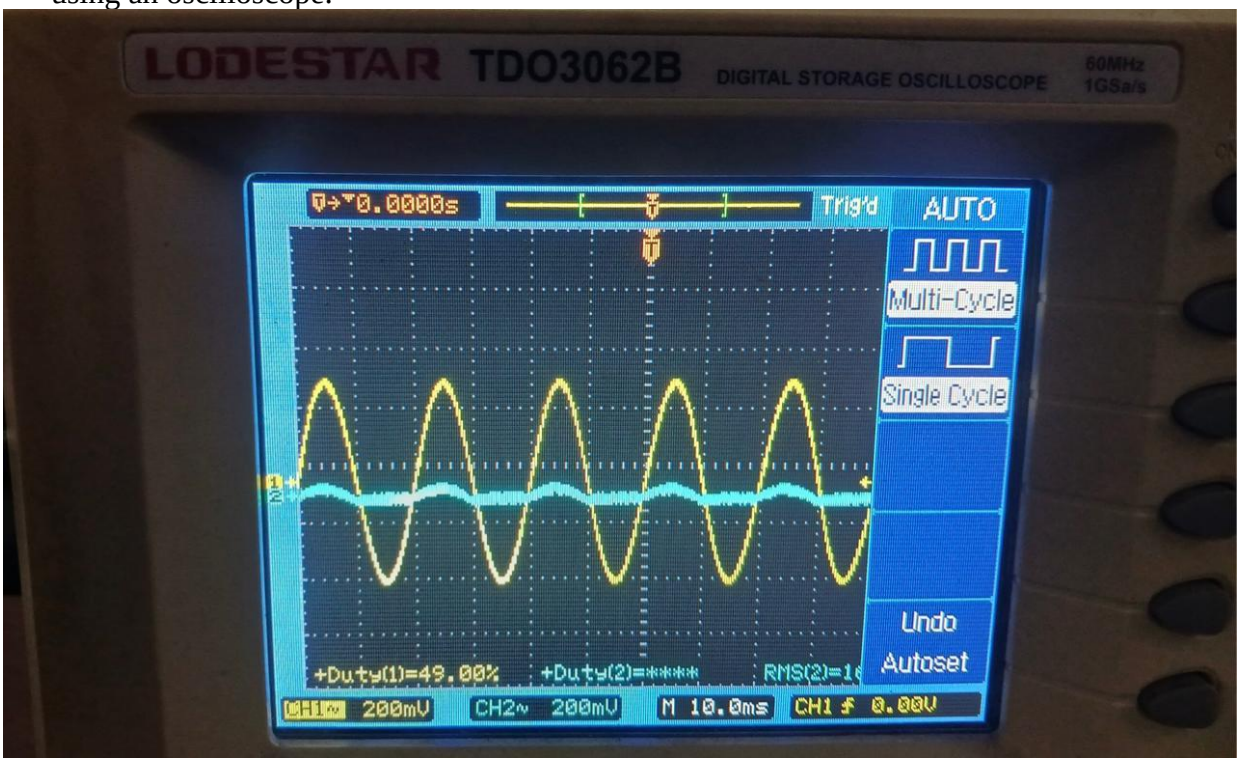
If this unwanted noise is not eliminated, it can cause:

- Unstable switching of comparators
- Flickering in the seven-segment display
- False triggering in the stabilizer stage
- Inaccurate averaging in the averaging stage

Therefore, the LDR voltage divider and the ADC input are separated by an analog low-pass filtering stage, as clearly shown in our Falstad circuit.

Experimental Verification of 50 Hz noise

- The presence of 50 Hz power line interference at the LDR output was experimentally verified using an oscilloscope.



Role of Low-Pass Filter

- The ambient light changes very slowly and contains only low-frequency signals below 10 Hz, while most noise is present at higher frequencies (50–100 Hz). Therefore, a low-pass filter is used to allow the slow light changes to pass and block the fast unwanted noise. As a result, the ADC receives a clean and stable voltage for accurate digital output.

Choice of Active Sallen-Key Filter

- Our group has implemented a 2^{nd} order Sallen-Key active low-pass filter using;
    - An operational amplifier
    - Two resistors
    - Two capacitors

Active Filter Instead of a Passive RC Filter

- Due to the high output impedance of the passive RC filter, the cut-off frequency changes as the filter is loaded by the ADC.
- The Sallen-Key active filter avoids this by providing;
    - High input impedance
    - Low output impedance
    - Stable cut-off frequency
    - Proper isolation between the sensor and ADC

Cut-Off Frequency Selection

- The cut-off frequency is set to 10 Hz to match the slow LDR response and gradual light changes

Mathematical Design for Filter

- **Calculation:**

Required attenuation to remove 50 Hz noise = $20\log_{10}(0.1) = |-20\ dB| = 20\ dB$

For a Butterworth filter:

$A = 10\log_{10}[1+ (\omega / \omega_c)^{2n}]$

$10^2 = 1+(50/10)^{2n}$

$100 = 1 + 5^{2n}$

$99 = 5^{2n}$

$n = 0.5\log_5(99)= 1.43$

Since order must be an integer:

$n = 2$

Normalized Transfer function for 2^{nd} order Butterworth filter:

$H(s) = 1/(s^2 +\sqrt{2}s +1)$

Denormalized Transfer function:

$H(s) = 1/(s^2/\omega_C^2 + \sqrt{2}s/\omega_C +1)$

From the denormalized Butterworth design:

$C_2 \geq 2C_1$

Selected values:

$C_1 = 1\mu F$

$C_2 = 2\mu F$

Required resistor sum:

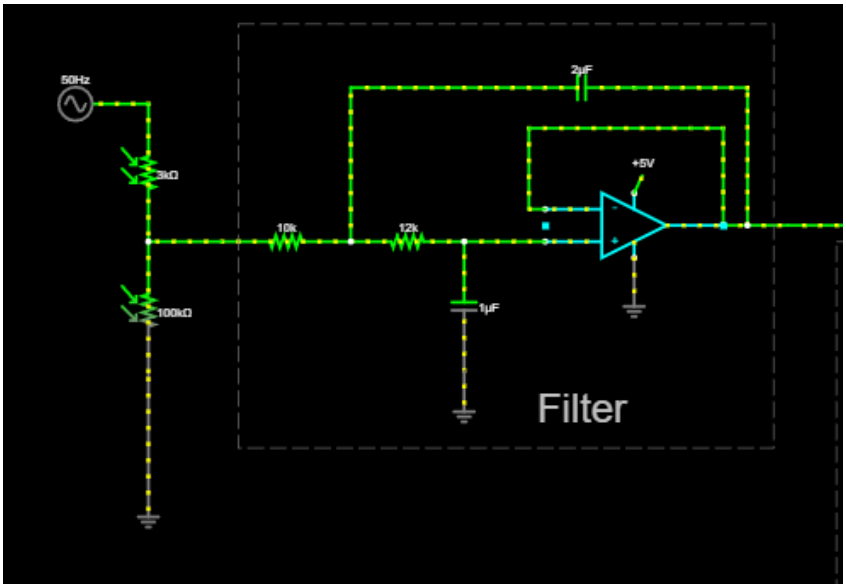
$R_1 + R_2 = 22k\Omega$

Chosen standard resistor values:

$R_1 = 10k\Omega$

$R_2 = 12k\Omega$

Falstad Simulation



Assumptions made

- The operational amplifier is powered using a stable single supply.
- The op-amp is assumed to be ideal.
- Component tolerance (±5%) have a negligible effect on system performance
- Power supply noise remains within acceptable laboratory limits

Feature 02: LDR Sensing and ADC with Seven Segment Display (0-7)

Introduction

- This feature senses ambient light using an LDR, convert it into digital form with an ADC and displays the light level from 0(very low light level) to 7(very bright light level) on seven-segment display in real time.

LDR Sensing and Voltage Generation

- A Light Dependent Resistor (LDR) – Light Sensing Element
- LDR is connected with a fixed resistor as a voltage divider.
- Output voltage change with light level due to,
    - More light → LDR resistance decreases
    - Less light → LDR resistance increases
- The changing voltage represents the **ambient light intensity**

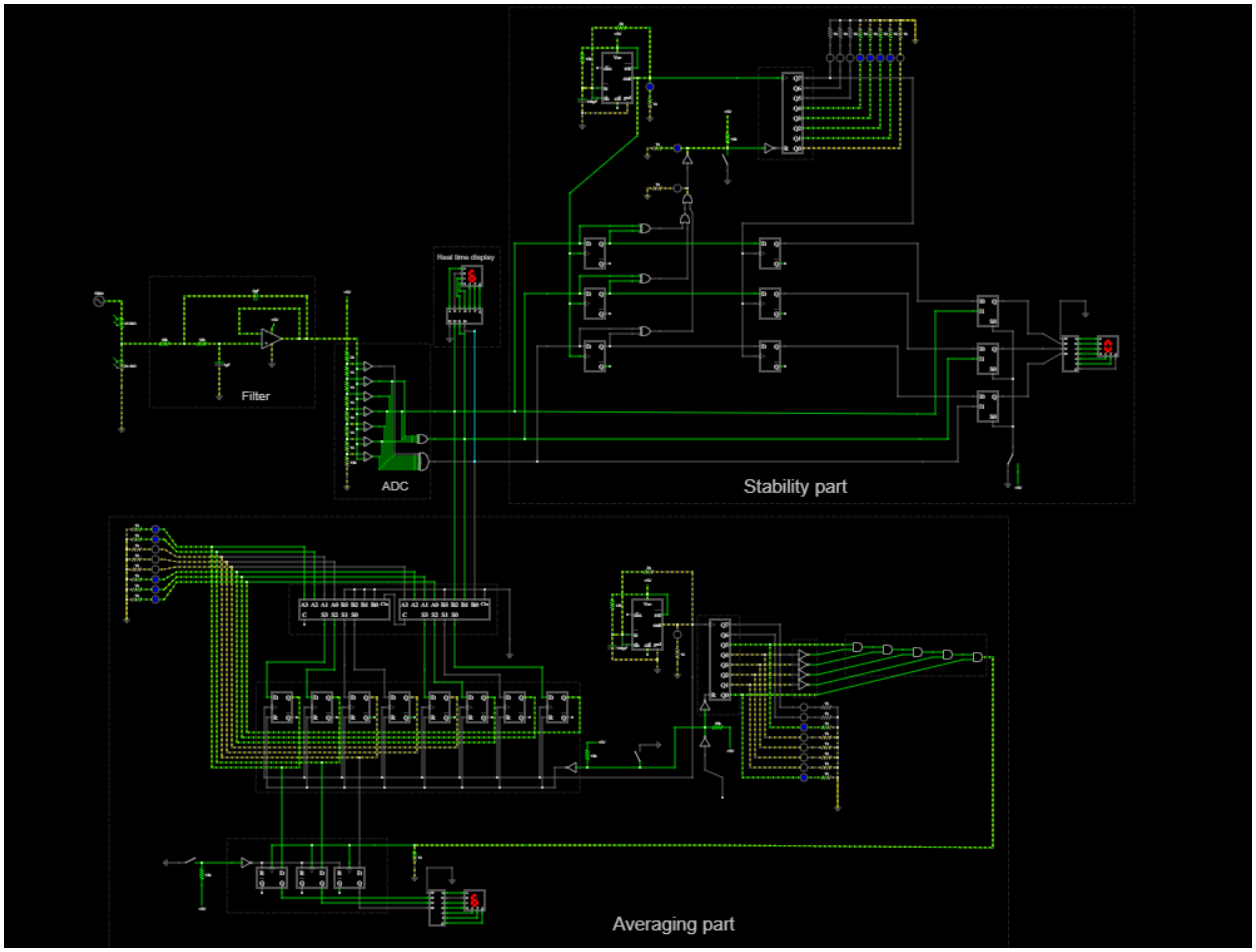
Analog to Digital Conversion and Display of Light Intensity

- The output of LDR is an analog voltage, while seven-segment display works using digital signals. Therefore, Analog to Digital Converter required.
- In this design, a **3-bit flash ADC** is used.
- Flash ADC structure:
  Number of output levels of an ADC = 2^n
  For n = 3;
  Number of output levels = 2^3 =8
  The ADC provides 8 digital levels from 0 to 7.

  Number of resistors = 2^3=8
  Number of comparators = $2^3 - 1$ =7
- **Why pull-Up resistors are used**:
    - The output of comparators can swing into negative voltage because they typically operate with both +5 V and −5 V. However, negative voltage can harm or result in malfunctioning digital components like flip-flops, encoders, and decoders, which can only operate at 0–5 V. The comparators are powered only by a +5 V supply with pull-up resistors at the output in order to prevent this. The pull-up resistor pulls the output HIGH when off, and the LM339's open-collector output pulls it LOW. This generates a clean, safe digital output between 0 and 5 V that can be used with any logic circuit.
    - Also, a pull-up resistor with a single +5V supply is used to constrain the output within 0 - +5V because comparators operating with ±V supplies can produce negative output voltages that are incompatible with single supply digital components(0 - +5V).This ensures safe, clean digital signaling and shields the downstream logic from malfunction or damage.
- The flash ADC produces 8 individual digital outputs for different light levels. The digital section is made simple and effective by using an **8-to-3 encoder** to covert these 8 lines into a 3-bit binary output (0 to 7).

- The ADC output can fluctuate quickly due to noise, shadows and slight changes in light. A stability circuit with flip-flops and logic gates keeps the output constant to prevent flickering on the display.
- Minor fluctuations can continue even after stabilization. By processing several samples, the averaging circuit smoothes the digital output, providing a more precise and reliable light level.
- The seven-segment decoder and display receives the steady 3-bit output, which clearly displays values from 0 to 7.

Falstad Simulation



Assumptions made

- All components are considered ideal.
- All digital components are 0V – 5V compatible.
- The system runs on a stable +5V supply.
- The sequential logic uses a stable and correctly timed clock signal.
- The 8 ADC reference resistors are perfectly matched.
- All memory elements (Flip-Flops) are properly cleared at power-up.

Feature 3: Stabilizer Circuit (Sudden Variation Suppression)

Introduction

- The stabilizer circuit is a digital control stage placed after the 3-bit ADC and before the averaging circuit. Its main function is to reduce sudden and temporary changes in the light level caused by noise, shadows and fast environmental variations. It ensures that the displayed light value changes only when the light level remains stable for a certain period of time. The stabilization time can be adjusted from 30 seconds to 300 seconds using a variable resistor and a switch is provided to enable or disable the stabilizer when required.

Need for Sudden Variation Suppression.

- Sudden fluctuations in light intensity could be caused by:
    - Human movement near the sensor.
    - Switching ON/OFF of nearby lamps.
    - Temporary shadows.
    - Small electrical disturbances.
- As a result, the stabilizer circuit must:
    - Prevent flickering on the seven-segment display.
    - Avoid rapid jumping between values.
    - Eliminate false triggering of digital circuits.
    - Provide a steady and reliable output.

Working Principle of the Stabilizer Circuit

I. Sampling and Comparison

- The previous 3-bit ADC output is stored in a single set of D flip-flops. XOR gates are used to compare the current ADC value with this stored value; if a bit has changed, each XOR output becomes high. A single CHANGE_DETECTED signal, which indicates instability whenever any bit changes, is produced by combining the three XOR outputs via an OR gate.

II. Counter Control and Stability Detection

- When CHANGE_DETECTED = 1, the counter is instantly reset. The counter keeps counting incoming clock pulses if no change is detected (CHANGE_DETECTED = 0). The input is considered stable once the counter has completed 64 uninterrupted pulses. This corresponds with the simulation's binary counter and reset wiring.

III. Output Latching

- A latch-enable pulse is produced when the counter reaches the stable count. The stable 3-bit value is stored by another set of D flip-flops that are triggered by this pulse. Until a new stable value is found, the output stays unchanged.

Stabilization Time Control (30 s – 300 s Adjustable)

- **Calculation**

A variable resistor adjusts the clock frequency (f) to control the stabilization time based on the fixed number of pulses (N=64)

$$Required\ Frequency(f) = \frac{\mathrm{N}}{\mathrm{T}}$$

$$f = \frac{1}{0.693 \times 2 \times \mathrm{Rvar} \times \mathrm{C}}$$

Given values:
N= 64 pulses and C = 100µF

For Minimum Stability Time (T=30 s),

$f = \frac{64}{30} \approx 2.13$ Hz

Substituting into the clock equation,

$$2.13 = \frac{1}{0.693 \times 2 \times \mathrm{Rvar} \times 100 \times 10^{-6}}$$

$\mathrm{Rvar} \approx 3.38\ \mathrm{k\Omega}$

For Maximum Stability Time (T=300 s),

$f = \frac{64}{300} \approx 0.21$

Substituting into the clock equation,

$$0.21 = \frac{1}{0.693 \times 2 \times \mathrm{Rvar} \times 100 \times 10^{-6}}$$

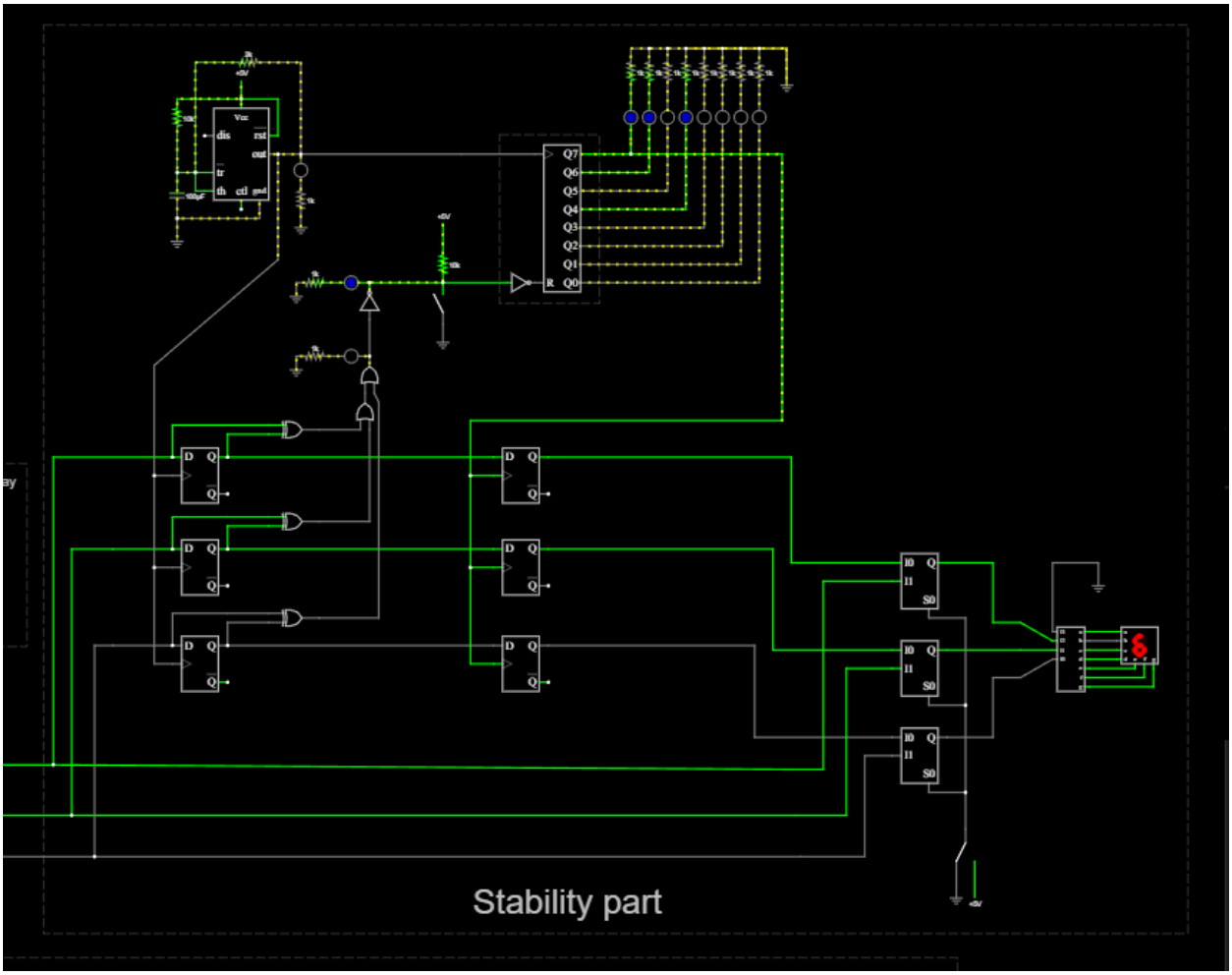
$\mathrm{Rvar} \approx 33.82\ \mathrm{k\Omega}$

- The required resistance range is approximately 3.3kΩ to 34 kΩ.
- So as to smoothly change the stabilization time from 30 to 300 seconds , a ….. variable resistor is chosen.

Enable / Disable Switch Operation

- In the simulation, the switch is connected after the output latch. When the switch is ON, the stabilizer output from the latch is used. When the switch is OFF, the raw ADC output bypasses the stabilizer and goes directly to the next stage.
- This allows selection between:
    - Fast response mode
    - Stable display mode

Falstad Simulation



Assumptions Made

- All flip-flops and logic gates work ideally.
- The input from the ADC is assumed to be filtered and stable (Feature 01).
- Clock frequency remains constant.
- The enable/ disable switch operates correctly.
- Power supply voltage remains constant.

Feature 4: Average Light Intensity Measurement and Display (300 s – 900 s Adjustable)

Introduction

- The system shows the average light intensity over a chosen time period in addition to the stabilized real-time light intensity. By eliminating transient variations, this feature provides a more accurate representation of the lighting condition. A variable resistor allows the averaging time to be changed from 300 to 900 seconds, and a push button reset allows the averaging process to be restarted as needed.

Need for Average Light Intensity Indication

- Instant light intensity values may vary due to:
    - Temporary shadows
    - Human movement near sensor
    - Short-term light fluctuations
    - Environment disturbances
- Therefore, the average light intensity display:
    - Represent long-term lighting conditions
    - Removes short term fluctuations
    - Helps in accurate energy management
    - Provides accurate indication of ambient lighting

Working Principle of the Averaging Circuit

I. Sampling and Accumulation

- Clock pulses are used for sampling the stabilized digital output.**33** stabilized samples are collected in the given design. Using an **adder circuit**, each sample is added to a running total.

II. Storage

- The accumulated sum is stored in a bank of **D flip-flops**.

III. Division (Averaging)

- The averaged 3-bit value is produced by combinational logic after all 33 samples have been collected. This final digital average is fed into a different display and seven-segment decoder.

- Thus, the display shows the **mean light intensity** over the selected time period.

Average Time Control (300 s – 900 s Adjustable)

- **Calculation**

  Based on the fixed number of samples (N=33) per cycle, a variable resistor adjusts the clock signal's frequency(f) to control the averaging time.

$$Required\ Frequency(f) = \frac{Number\ of\ Samples(N)}{\text{Time Period(T)}}$$

$$f = \frac{1}{0.693 \times 2 \times \text{Rvar} \times C}$$

Given values:
N= 33 samples and C = 100µF

For Minimum Averaging Time (=300 s),

$Required\ frequency(f) = \frac{33}{300}$ = 0.11 Hz

Substituting into the clock equation,

$$0.11 = \frac{1}{0.693 \times 2 \times \text{Rvar} \times 100 \times 10^{-6}}$$

$$Rvar = \frac{1}{0.11 \times 0.693 \times 2 \times 100 \times 10^{-6}}$$

Rvar ≈ 65.59 kΩ

For Maximum Averaging Time (= 900s),

$Required\ frequency(f) = \frac{33}{900} \approx 0.0366$ Hz

Substituting into the clock equation,

$$0.0366 = \frac{1}{0.693 \times 2 \times \text{Rvar} \times 100 \times 10^{-6}}$$

$$Rvar = \frac{1}{0.0366 \times 0.693 \times 2 \times 100 \times 10^{-6}}$$

Rvar ≈ 196.77 kΩ

- The required resistance range is approximately 65 kΩ to 200 kΩ.
- So, a ….. variable resistor is selected to adjust the averaging time from 300 s to 900 s.

Push Button Reset Operation

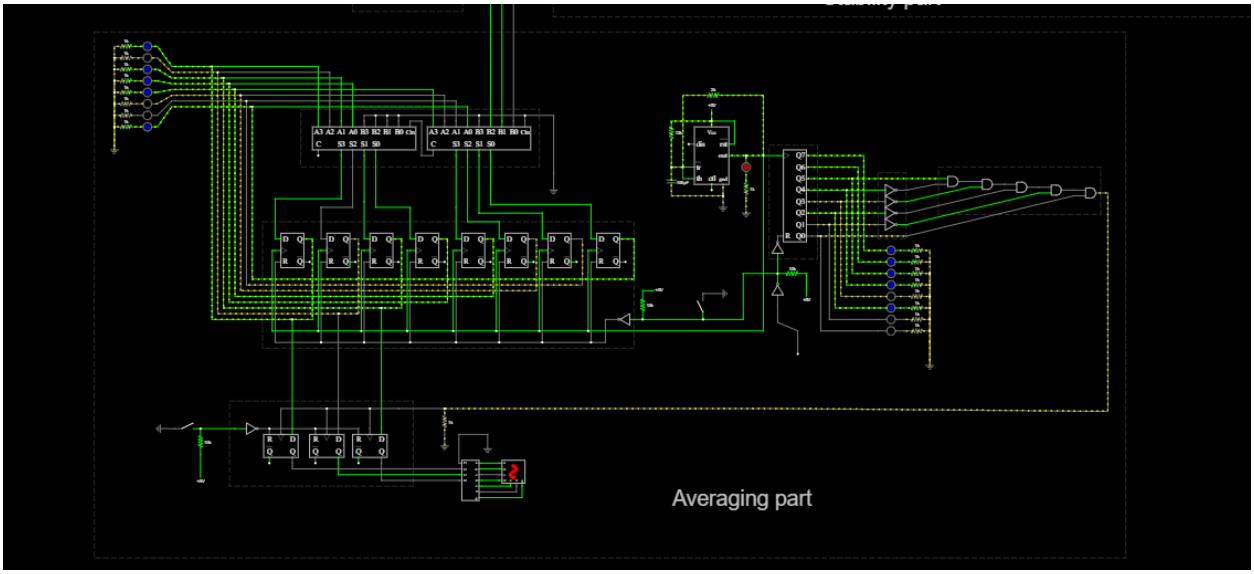
- A push button switch is provided to reset the averaging circuit.
    - When the reset button is pressed, all averaging flip-flops are cleared.
    - The counter reset to zero.
    - A new averaging process begins.
- This makes it possible to begin a new measurement whenever a new cycle is needed or the lighting conditions significantly change.

Average Seven Segment Display Indication

- A separate seven-segment display is connected to the final averaged 3-bit digital output.

- The display ranges from 0 (very low light) to 7 (very high light).
- Since the value is averaged over a long period :
    - No flickering
    - Very smooth display transition
    - Highly stable output

Falstad Simulation



Assumptions made

- All flip-flops and logic gates work ideally.
- Input from Feature 03 is stable and noise-free.
- Clock frequency remains constant.
- Push-button reset works without bouncing.
- Power supply voltage remains constant.