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## High Frequency Amplifier

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Submission Date : February 27, 2023

This report is submitted as a partial fulfilment of module EN2091

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# Abstract

This report offers a comprehensive discussion concerning the design criteria of a high frequency amplifier, which is aimed at amplifying a sinusoidal wave in the frequency range of 20 kHz to 100 kHz from a speaker with an  $8\ \Omega$  output impedance. Within the scope of the project guidelines, our design was restricted to using only transistors, with a minimum of three transistors to be used. The ultimate goal was to achieve a high power gain output without any distortion. To initiate our design process, we utilized the small signal model for transistors in our initial calculations. To further evaluate and simulate the circuit design, we employed LTspice XVII. Furthermore, the printed circuit board (PCB) was designed using Altium Designer(22.9.1). The physical circuit was implemented on a bread board before the PCB design process. Finally, the enclosure was designed using Solidworks2020. At the end of the project, a comprehensive data sheet comprising all relevant data was produced.

## 1 Introduction

A high frequency amplifier is a device used to amplify signals of higher frequencies with a high gain and no distortions. With an ordinary amplifier, the gain typically decreases as the frequency increases. Due to bandwidth restrictions, there is also a high possibility that the signal will get distorted. This problem is fixed by the high frequency amplifier, which amplifies the signal with high power gain and no distortions. Finally, the signal is sent through a speaker with a lower impedance. The appropriate steps were carried out to decrease the distortions there as well.

## 2 Functionality

The objective of our project is to have a distortion free output for an input signal with a single-tone sine wave of 0.1 V peak to peak; through a speaker with  $8\ \Omega$  impedance.

When the amplitude of the input signal is very low, the power of the signal is also very low, and 0.1 V of amplitude is insufficient for the speaker action. The signal power and signal-to-noise ratio must then be increased. When amplitudes are tiny, the noise effect will be very strong.

The input sine wave's amplitude should therefore be increased first. For this, a voltage amplifier is used as pre Amplifying stage.

### 2.1 Stage One - Voltage Amplifier

The voltage amplifier should be implemented using one of the three configurations because the project should only be completed using transistors.

The BJT transistor can be used in three different configurations as a Voltage Amplifier.

- Common Collector Configuration
- Common Emitter Configuration
- Common Base Configuration

The **common collector** has a voltage gain almost equal to one, whereas it acts as a buffer due to its active current gain. The Power gain is equal to the voltage gain since the current gain of the **common base** configuration is equal to one.

We have chosen to use common emitter configuration as the pre amplifying stage due to the largest power gain that can be achieved with a BJT transistor in the **common emitter** configuration.

A high power gain is preferable when driving the output signal to a headset.

The next step is to obtain a power amplification since we have increased the signal amplitude.

A smaller current ( $50\ mA$ ) produced by the pre-amplifier is insufficient to drive the speaker. The preamplifier had a considerable power gain, but we still needed to increase it to provide distortion-free, pure output when used with an  $8\ \Omega$  resistance speaker.

### 2.2 Stage Two - Power Amplifier

For the second stage; to generate the required output, a power amplifier made of transistors is needed.

Only transistor-based power amplifiers are divided into a few classes: i.e. A, B, AB and C[4].

- **Class A** : The Q point is almost in the middle i.e.  $\frac{V_{cc}}{2}$ . As a result, even without an input signal, a current will flow through the transistor.

There is significant power loss as a result. The power efficiency of the **class A** power amplifiers is hence lower ( Theoretically 50% - The efficiency also depend on the nature

of the output: i.e. inductive or capacitive )

Thus, this type is unsuitable for our objectives.

- **Class B** : Q point is in the cutoff region. Due to the fact that current will only flow through when an input is provided, this type is significantly more power efficient. ( Theoretically 78.5% )

Nevertheless, crossover distortion is a negative consequence of this B-class type.

Each transistor's base-emitter junctions should be made forward-biased. The biasing will use a portion of the input voltage, which results in crossover distortion.[3]

- **Class AB** : At the edge of the cutoff and active regions, the Q point operates.

The voltage required to forward bias the base-emitter junctions of each transistor is already present. As a result, the input signal won't be used to bias those junctions. By doing so, the crossover distortion will be eliminated.

In considering the above factors, we will now use **class AB** for power amplification.

Initially forward biasing the two junctions is required before sending the input signal.

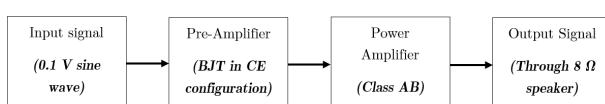
Transistors, diodes or resistors can be used to do this. However, if resistors are used, the impedance will be imbalanced.

Using the **common collector transistors** results in favorable outputs.

In addition to providing an initial forward bias for the two junctions, the transistor's buffer also aids in impedance matching when cascading two stages: the pre-amplifier and the power amplifier.

We made an effort to construct our system model using the aforementioned key factors.

## 2.3 Block Diagram



## 3 System Model

### 3.1 Stage One - Voltage Amplifier

Since we are preparing a High-frequency amplifier, we need to consider the transition frequency of the transistor. When comparing<sup>1</sup> the most common transistors, the highest **transition frequency** has the BC547 transistor.

Also, we can have high **current gain** (especially stable current gain with collector current and temperature) through BC547.

For the voltage amplifying stage, we have selected BC547 to create the Common Emitter amplifier based on the previously mentioned qualities as well as other features like relatively **fast switching and fast responding time**.

#### 3.1.1 DC Analysis

Through the datasheet, we observed that we can have the highest gain bandwidth product at nearly 20 mA. There we have decided to choose 20 mA as the **quiescent current**.

Since the supply voltage is 12 V, to maintain the quiescent point near the mid point, we need to maintain  $V_{CE} = 6 V$ .

To maintain the thermal stability of the transistor, we need to have an emitter degeneration resistor.

**Calculate  $R_C$ : From KCL:**

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

As a rule of thumb, we need to maintain  $V_E$  less than 10% of  $V_{CC}$ .

Therefore;  $12 V = 20 mA \times R_C + 6 V + 1.2 V$

$$R_C = 240 \Omega$$

Since  $I_B$  is a very small current, Let assume that  $I_C = I_E$

Using Ohm's law for  $R_E$ :

$$1.2 = 20 mA \times R_E$$

$$R_E = 60 \Omega$$

Let consider the input side:

Since we are using **Potential Divider Bias** method as the biasing technique,

$$\text{Thevenin voltage} = V_{BE} + V_E$$

$$V_{TH} = 0.7 V + 1.2 V$$

$$V_{TH} = 1.9 V$$

Let the  $R_{B1} = 10 k\Omega$

Then the value for  $R_{B2} = 1.88 k\Omega$

<sup>1</sup>Table 1 in the appendix compares the three most common general-purpose transistors (BC107, BC547, and 2N2222).

### 3.1.2 AC Analysis

We need to put a bypass capacitor to prevent the emitter degeneration resistor's negative feedback.

For an AC signal, to neglect the emitter resistance, the impedance of the capacitor should be very low when compared with the resistance of the emitter resistor.

Let's take the minimum impedance of the capacitor as  $2 \text{ m}\Omega$ .

Since our maximum frequency is  $100 \text{ kHz}$ , the minimum capacitance of the capacitor is:

$$C = \frac{1}{2\pi \times 10^5 \times 0.002} = 795 \mu\text{F}$$

Therefore, we decided to take  $1 \text{ mF}$  capacitor as the emitter bypass capacitor

We found the following values for **coupling capacitors** in the hybrid  $\pi$  model for BJT using small signal analysis for lower frequencies to prevent distortion.

For input coupling capacitor =  $3 \mu\text{F}$

For output coupling capacitor =  $100 \mu\text{F}$

## 3.2 Stage Two - Power Amplifier

There is a significant current flowing through the transistors in the power amplification stage.

**Power transistors** are required to control high currents.

We observed that the output of the voltage amplifier is  $2.9 \text{ V}$  peak-to-peak voltage using the **LT spice** simulations.

The output voltage signal should have a  $2.9 \text{ V}$  peak-to-peak voltage (or  $1.45 \text{ V}$  amplitude) if there are no voltage drops in the signal. Then the maximum current that can flow through the resistor will be  $181 \text{ mA}$  as we are connecting the output signal to  $8 \Omega$  resistor.

As a result, we require a power transistor with a  $200 \text{ mA}$  control capacity. We also need a **complementary symmetry** pair for AB class operation. Due to the requirement for through-hole transistors, we have selected the complementary symmetry pair of **TIP31** and **TIP32**, which has a maximum collector current of  $5 \text{ A}$ .<sup>[5]</sup>

To maintain the **thermal stability** of an AB push-pull amplifier, resistors are required. But,

in order to maximize power gain, power dissipation through the resistors must be minimized. Thus, we use resistors with  $2.2 \Omega$  resistance.  $68 \Omega$  resistors have been used with emitter follower transistors to maintain stability with less power loss.

## 4 Schematic

<sup>2</sup> The component values should be used in a practical manner. As a result, we modified some of the results of our computations.<sup>3</sup>

$$R_C = 220 \Omega$$

$$R_E = 68 \Omega$$

$$R_{B2} = 2 \text{ k}\Omega$$

$$\text{For input coupling capacitor} = 4.7 \mu\text{F}$$

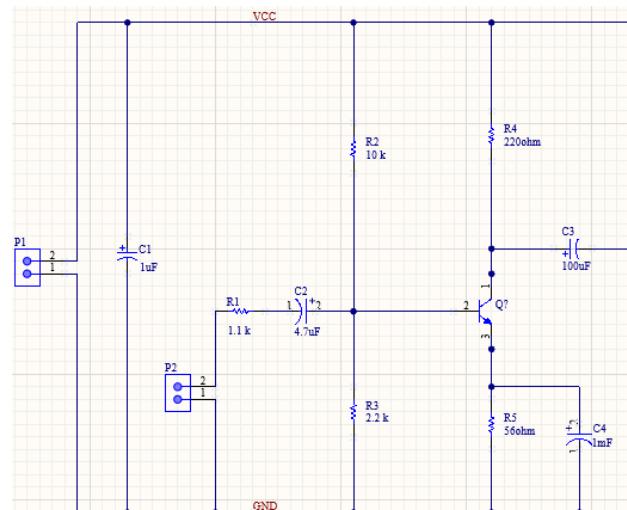
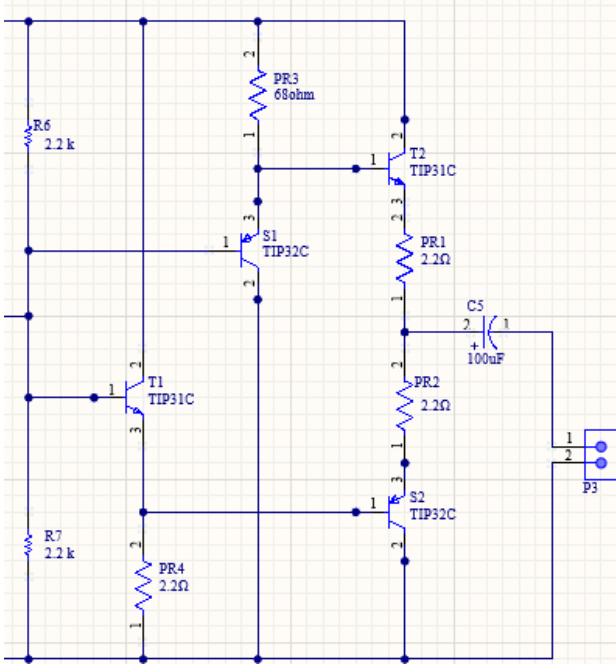


Figure 1: Stage 01 : Voltage Amplifier

<sup>2</sup>This section only includes the schematics for the two stages: the voltage and power amplifiers. The Figure 5 diagram in the appendix contains the entire schematic for the entire circuit.

<sup>3</sup>After the Breadboard implementation, we have to change the values as we can not use ideal values as we have to consider the wire resistance. Therefore to maintain the Q point in the linear region in the output characteristic,  $R_E = 56 \Omega$  and  $R_{B2} = 2.2 \text{ k}\Omega$ .



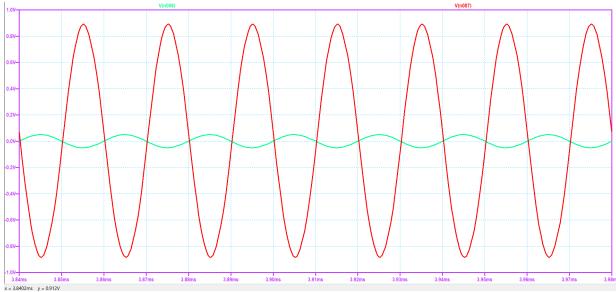
**Figure 2:** Stage 02 : Power Amplifier

## 5 Results

### 5.1 LTspice Simulations

The initial simulations in LTspice revealed that the output sine wave deviated slightly from the expected waveform. The output of the power amplifier stage exhibited significant distortion, which was also observed at the pre amplifier output. This finding led us to conclude that the distortion was not an issue specific to the power amplifier stage. To address this, we modified the value of the emitter degeneration resistor to bring the transistor within the linear range, leading to a clipped output. We then adjusted the input resistance to achieve a precise sine wave output signal with minimal distortion.

After we changed the values, we observed the following graphs for the input (*green colour graph*) and output (*red colour graph*) signals through the LTspice simulations

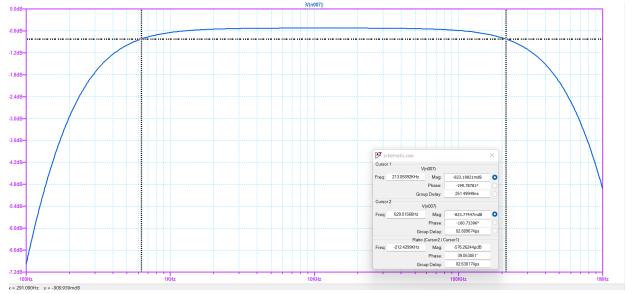


**Figure 3:** Input and Output signals

### Simulation Parameters

#### With Load(8 Ω)

- Input Current (pk to pk) :  $64.39 \mu A$
- Input Voltage (pk to pk) :  $0.1 V$
- Output Voltage (pk to pk) :  $1.556 V$
- Bandwidth The frequency response provides valuable information that can be used to determine bandwidth. This is referred to as the frequency range with a good gain. The range of frequencies for which the gain is more than  $\frac{1}{\sqrt{2}}$  or the range of frequencies for which the gain is more significant than  $-3 dB$  compared to the mid-frequency can be used to define bandwidth. The figure shows the bandwidth and frequency response.



**Figure 4:** Bandwidth

According to the Graph: Bandwidth of the simulation is,  $212 kHz$

### 5.2 Breadboard Implementation

Following the simulation, we implemented the proposed design on a breadboard. During this process, we encountered minor distortions in the output, which we attributed to the wire and breadboard internal resistance. We adjusted the resistor values to mitigate this to obtain the expected waveform. Furthermore, we encountered ground instability issues, which we resolved by introducing a capacitor between the ground and the power line. To manage thermal power, we have used several techniques. Some of them are as follows.

Resistors with high power ratings have been used. For emitter followers and class AB amplifiers, respectively, 2W and 5W resistors are used. Power transistors were connected to heat sinks to disperse the power effectively.

A significant distance separated the above high-power components. It will help reduce the surrounding warmth by maintaining proper **ventilation**.

Component	Quantity
BC547 Transistor	1
TIP31 Transistor	2
TIP32 Transistor	2
2.2 $k\Omega$ Resistors	3
10 $k\Omega$ Resistors	1
220 $\Omega$ Resistors	1
56 $\Omega$ Resistors	1
1.2 $k\Omega$ Resistors	1
68 $\Omega$ 2W Power Resistors	2
2.2 $\Omega$ 5W Power Resistors	2
1 $\mu F$ Capacitors	1
4.7 $\mu F$ Capacitors	1
100 $\mu F$ Capacitors	2
1 $mF$ Capacitors	1
Heat sinks	4
Red LED	1
Connectors	3

### 5.3 Measurements for the data-sheet

we then proceeded to design the printed circuit board (PCB) and performed a series of tests to evaluate its performance. Specifically, we tested the device by transmitting various sinusoidal signals within the frequency range of 20kHz to 100kHz, with the aim of identifying any potential output distortions. Next, we conducted experiments to measure the device parameters of the high frequency amplifier, such as the input and output impedance, open loop gain, closed loop gain, and bandwidth, to produce data for the device data sheet. These measurements were taken using a specific signal frequency as a reference<sup>4</sup>.

<sup>4</sup>Our Reference is 20 kHz

### Input Impedance

Initially, the multi meter measured the current being pulled from the source. Once the measured current value was obtained, the input impedance was calculated by dividing the input voltage by it. The prototype circuit's obtained input impedance value was  $1.55 k\Omega$ .

### Output Impedance

The input of the high-frequency amplifier was short-circuited, and a multi meter was used to measure the voltage across the output. The impedance value can be calculated by dividing the measured value by the amount of current flowing through the output. The prototype circuit's output impedance measurement came out to  $12 \Omega$ .

### Open Loop Gain

The voltage gain obtained without the load(Speaker) is an open loop gain. The gain was determined by connecting the input and output terminals to the oscilloscope. The ratio of the input and output peak-to-peak voltage values can be used to calculate the voltage gain (refer Figure 14). We are changing the frequencies between 20 and 100 kHz allowed to measure the gain value. In the frequency range mentioned above, the gain value remains constant. The obtained open loop gain in the prototype circuit was

$$Gain(for\ 20\ kHz) = \frac{2.38}{0.1} = 23.8$$

$$\therefore Open\ Loop\ Gain = 27.53\ dB$$

### Closed loop gain

Output peak-to-peak voltage is measured after connecting the speaker( with eight ohms impedance). Then using input peak-to-peak voltage, we measured the closed-loop gain( refer ??). The value is

$$Gain(for\ 20\ kHz) = \frac{2.04}{0.1} = 20.4$$

$$\therefore Closed\ Loop\ Gain = 26.19\ dB$$

### Bandwidth

We have used the oscilloscope<sup>5</sup> to determine the amplifier's bandwidth. We first measured the output peak-to-peak voltage at a frequency of 20 kHz and then increased the frequency by 10 kHz. The output voltage initially rises before starting

<sup>5</sup>In the appendix, oscilloscope images of Figure 9 i.e. 20 kHz and 360 kHz are included.

to fall. We then discovered the frequency that produces an output voltage equal to the stage of  $20\text{kHz}$ .  $360\text{kHz}$  is that frequency.

$$\text{Bandwidth} = 360 - 20 = 340 \text{ kHz}$$

### Total Harmonic Distortion

We observed **Fast Fourier Transformations** at various frequencies in order to compute the total harmonic distortion. Only the fundamental and the first three harmonics were taken into account for the calculations<sup>6</sup>.

Frequency (kHz)	THD(Percentage)
20	4.972
50	6.00
100	6.30

## 6 PCB design

The PCB layout is created to accommodate the requirements for high-frequency applications while minimizing temperature increase. The angle between two adjacent current passing lines is taken at an obtuse angle to minimize interference. Trace widths are determined based on the maximum current, and the average temperature rises to allow the current to flow quickly.

We used two layers in the PCB to reduce high-frequency noise and ground the signal as rapidly as feasible.

As the two transistors of TIP31c and TIP32c are power related, they get heated quickly; therefore, we place them in the four corners of the PCB board.

After the board's design was complete, we sent it to JLPCB to obtain a high-quality PCB to reduce noise.

## 7 Enclosure design

<sup>7</sup> The minimum dimensions  $110 \times 62 \times 107 \text{ mm}^3$  that really can fit the PCB inside the enclosure have been taken into consideration when designing the enclosure, which consists of an upper half and a lower half joined by eight tiny nails.

The thickness of the walls of the enclosure is

$2 \text{ mm}$  to achieve both strength and lightness simultaneously. Several vents are suitably positioned according to the placement of the power transistors on the PCB to allow the heated air to flow out. Therefore it **prevents the overheating** of the power transistors.

Due to the use of two top sides in the arrangement of vents, more attention has been given to the aesthetics of the enclosure. Power ON/OFF the **SPST** ( Single Pole Single Throw ) switch and a red LED that indicates the power ON/OFF is placed on the backside of the enclosure.

Also, there are three ports on the backside: RCA port, DC Base Barrel Female Socket, and 2-way speaker connector. These ports allow respectively to connect of the audio jack, which gives the input signal, a 12v power supply jack, and a speaker, which allows observing the output signal from the device as sound. The PCB and all the ports are connected to the lower part of the enclosure for easy maintenance.

## 8 Individual contributions of each group member

Group Members	
Name.	Contribution
M.I.A. ABSAR (200010J)	Data Sheet Preparation
K.N.A.L. FERNANDO (200164H)	PCB design, Prototyping (soldering) and Initial Calculations
G.W.C.M. LUCKSHAN (200358G)	Data Sheet Preparation, Initial Calculations and Overall Project Report
R.D.P.M. Ranasinghe (200512B)	Enclosure Design and Soldering

<sup>6</sup>The values are obtained using the [Figure 12](#)

<sup>7</sup>The enclosure design was created using *SOLIDWORKS 2020*.

## 9 Conclusion & Future Works

Since this is a high frequency amplifier, still there remains the possibility of slight output distortions. To further reduce the potential for noise, we could use constant current differential amplifier that utilizes transistors in place of a voltage amplifier.

Moreover, while the **TIP 31** and **TIP 32** power amplifier stage offers a lower gain, it is possible to further improve the power gain by using complementary symmetry power transistors with a Darlington pair. Such an approach would result in a high-current output. But the use of transistors with Darlington pairs not implemented in this instance because of the cost concerns.

## 10 Acknowledgement

The success of this project was dependent on various factors, one of which was the guidance and assistance of numerous individuals. We express our utmost gratitude to our project guides, Mr. Tharindu, Ms. Yomali, and Ms. Amashi, whose unwavering dedication and keen interest in our work helped in the successful completion of our project. Furthermore, we would like to thank everyone who contributed even in small ways to the success of this endeavor.

## References

- [1] DISCRETE SEMICONDUCTORS. “2N2222; 2N2222A”. In: (1997).
- [2] DISCRETE SEMICONDUCTORS. “BC107; BC108; BC109”. In: (1997).
- [3] Mihai Albulet. *RF power amplifiers*. Vol. 2. SciTech Publishing, 2001.
- [4] Rosalfonso Bortoni, Rui Seara, et al. “On the design and efficiency of class A, B, AB, G, and H audio power amplifier output stages”. In: *Journal of The Audio Engineering Society* 50.7/8 (2002), pp. 547–563.
- [5] Paul Tobin. “Operational Amplifier Characteristics”. In: *PSpice for Circuit Theory and Electronic Devices*. Springer, 2007, pp. 127–154.

## 11 Appendix-I Data Sheet

### High Frequency Amplifier

#### FEATURES

- Input Signal - Sinusoid with 0.1 V peak to peak Amplitude
- Supply Voltage - 12 V.

#### APPLICATIONS

- High frequency amplifier(for single tone sinusoid) which can drive a load impedance of  $8 \Omega$  (head-phone)

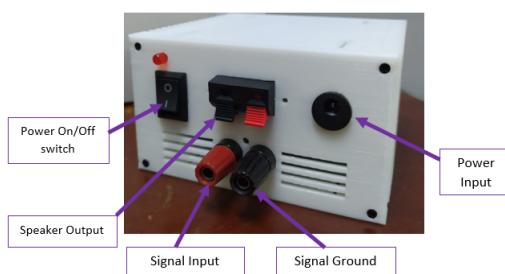
#### DESCRIPTION

- Low Noise Output
- Class AB Solid State Amplifier

#### ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$BW$	Bandwidth	$R_L = 8 \Omega$	20		360	kHz
$A_{vo}$	Voltage Gain	$R_L = \infty$		27.5		dB
$A_v$	Voltage Gain	$R_L = 8 \Omega$		26.1		dB
$R_{in}$	Input Impedance	$R_L = \infty$		1.55		$k\Omega$
$R_{out}$	Output Impedance	$R_S = 0$		12		$\Omega$
$P_{out}$	Output Power	$R_L = 8 \Omega$	0.225	0.25	0.33	W
$T_o$	Operation Temperature	$R_L = 8 \Omega$	25		32	$^{\circ}C$

#### PINNING



## 12 Appendix-II Tables and Figures

Characteristic	BC107[2]	BC547	2N2222[1]
Trans. Freq.	150	300	250
Gain	110-450	110-800	30-300

Table 1: General Purpose Transistors

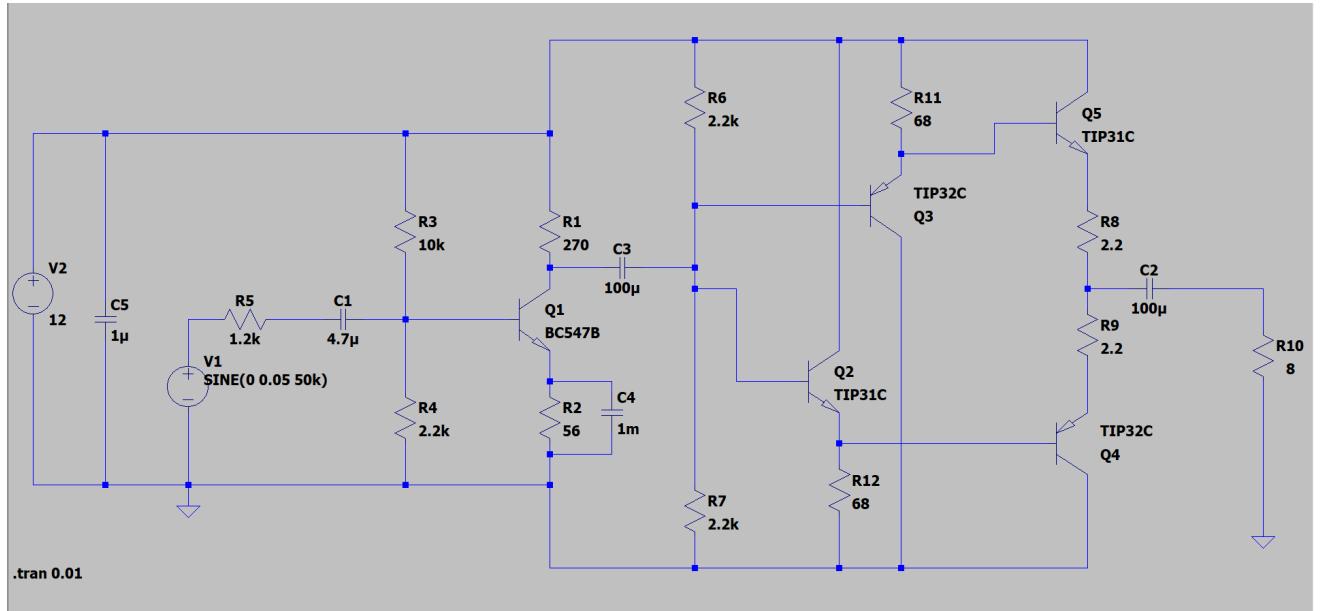


Figure 5: Full circuit - LTspice XVII

Wave forms from the prototype

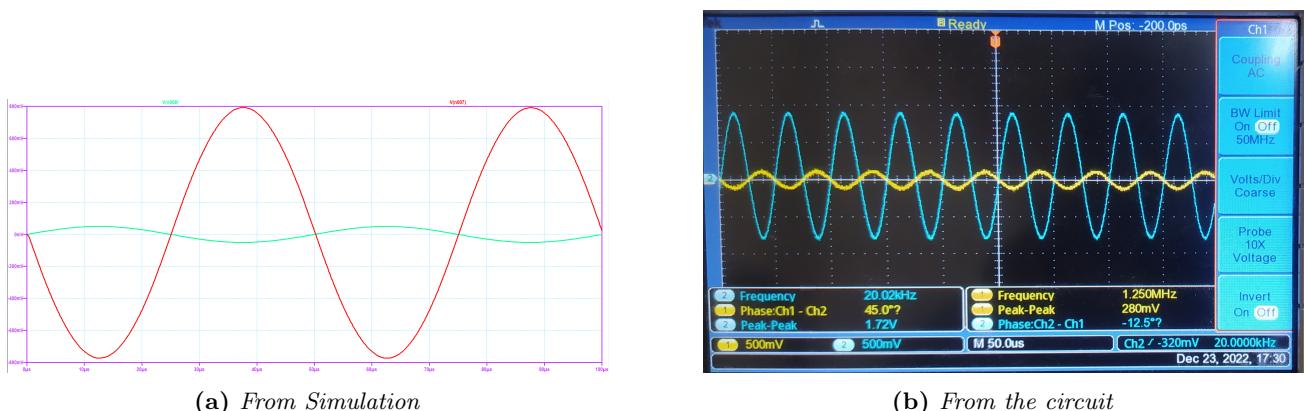
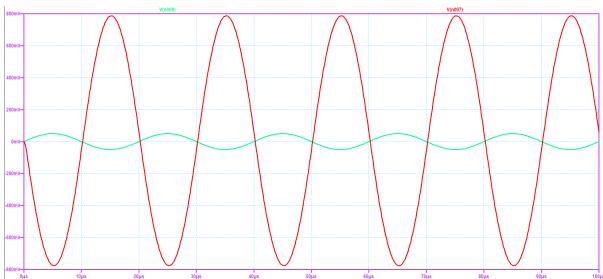
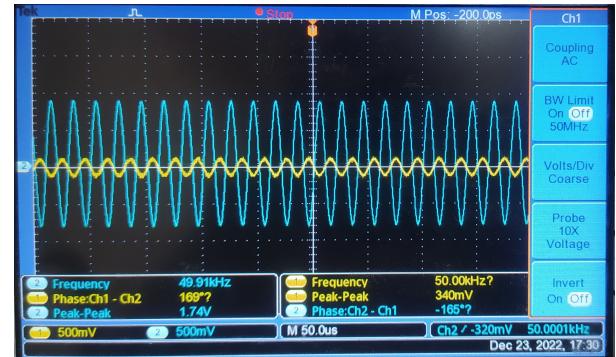


Figure 6: For 20 kHz

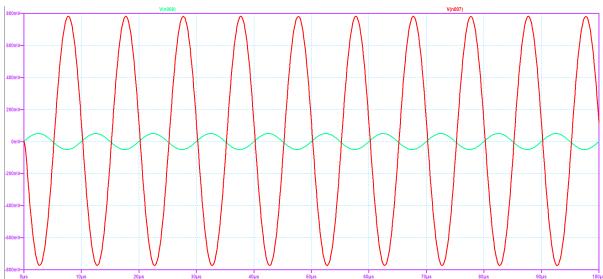


(a) From Simulation

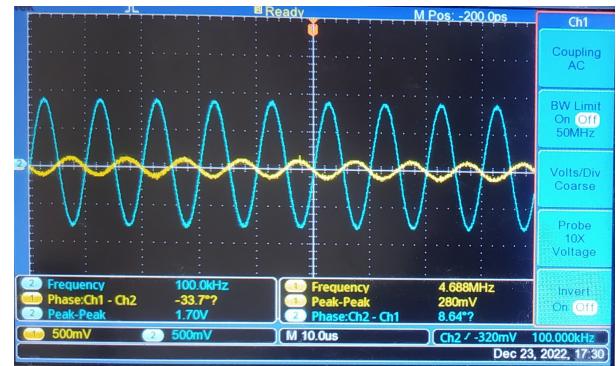


(b) From the circuit

Figure 7: For 50 kHz



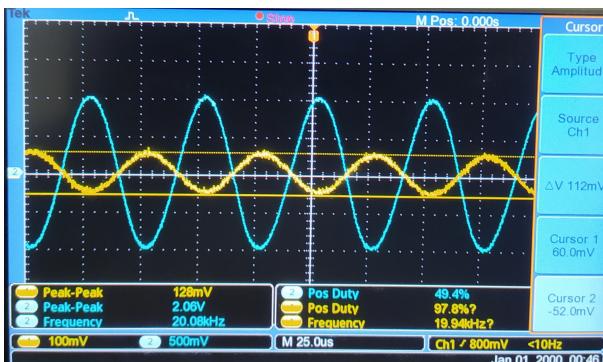
(a) From Simulation



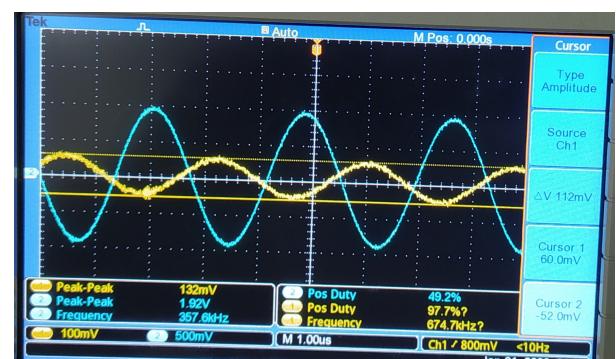
(b) From the circuit

Figure 8: For 100 kHz

### Bandwidth Calculations



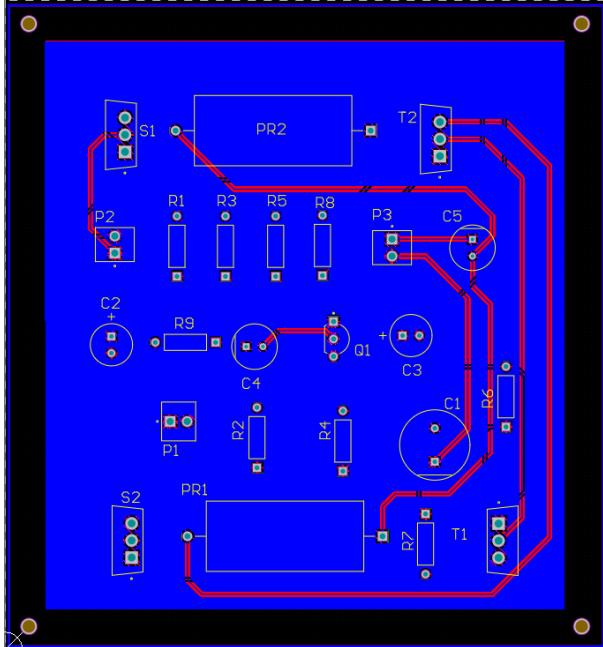
(a) 20 kHz



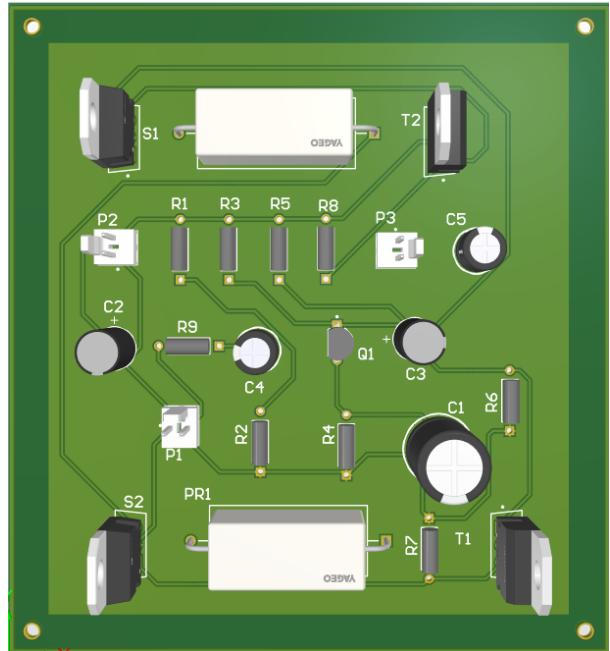
(b) 360 kHz

Figure 9: 3 dB cutoff points

## PCB Design and Enclosure

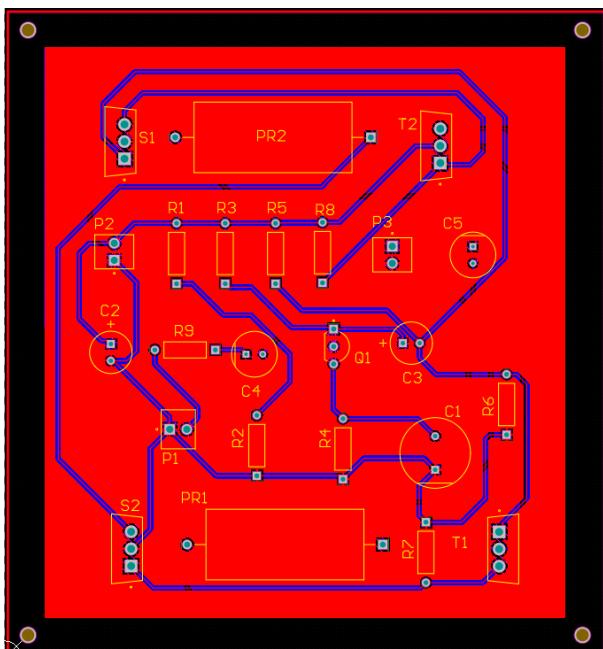


(a) Bottom Layer

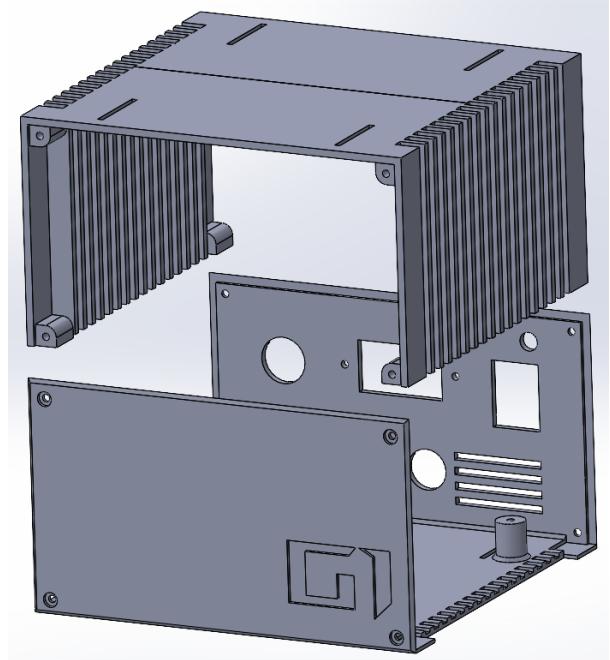


(b) 3-D View

Figure 10: PCB Design



(a) PCB Design



(b) Enclosure

Figure 11: PCB Design

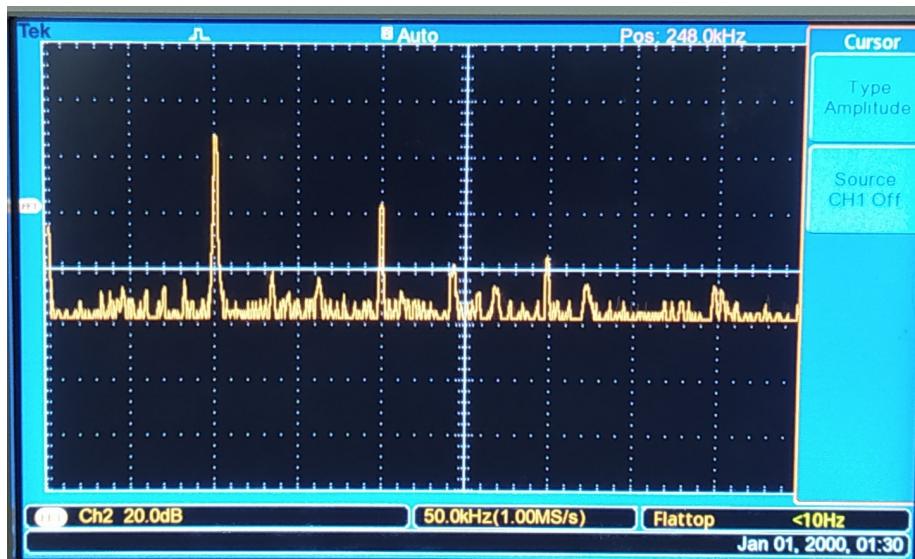


Figure 12: FFT Plot

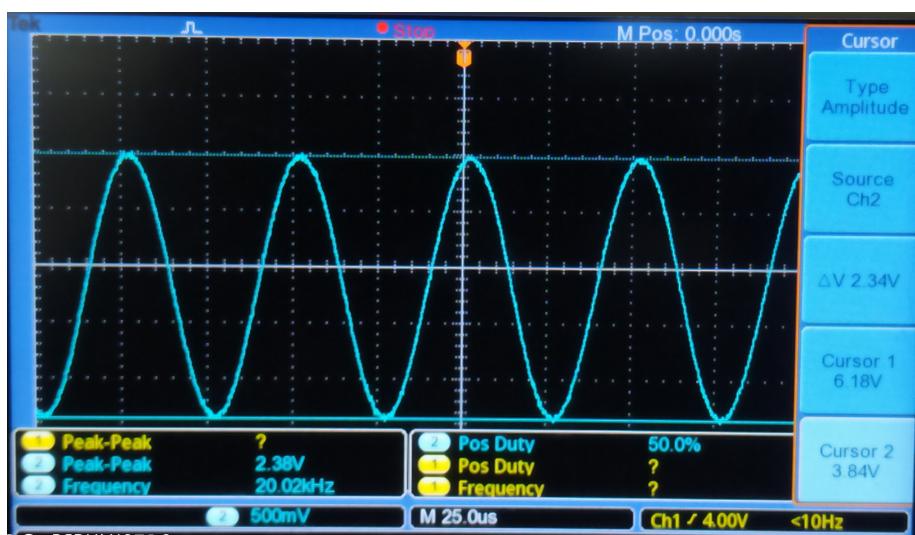


Figure 13: pk-to-pk Voltage (without Load)

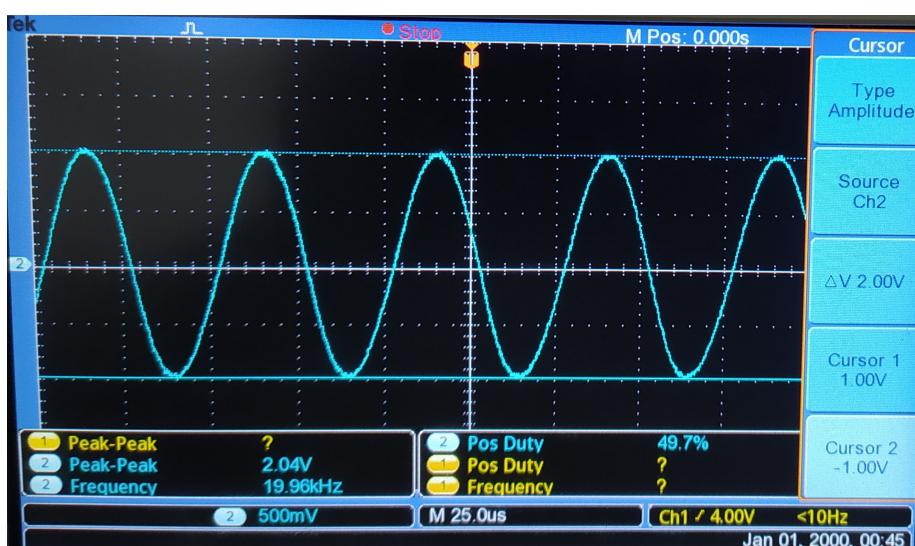


Figure 14: pk-to-pk Voltage (with Load)