COUNTERS

Counter is an instrument used for measuring time and therefore frequency. A counter is simply a device that counts. They will count up or down by one's, two's or more.

Counters are a series of flipflops wired together to perform the type of counting desired.

The total numbers of counts or stable states a counter can indicate is called Modulus.

e.g. — Modulus of four bit counter is 16 (it is capable of counting 0000_2 to 1111_2)

Binary counters can be classified as —

(1) Asynchronous counter or Ripple counter
(2) Synchronous counter

Asynchronous Counter / Ripple Counter →

It is constructed by use of clocked T-flipflop.

In this, the output of a flipflop is used as clock inputs of next flipflop.

The term Asynchronous refers to events that do not occur at same time.

The clock is connected to flipflop A. The flipflop B is triggered by Q_A (output of flipflop A).

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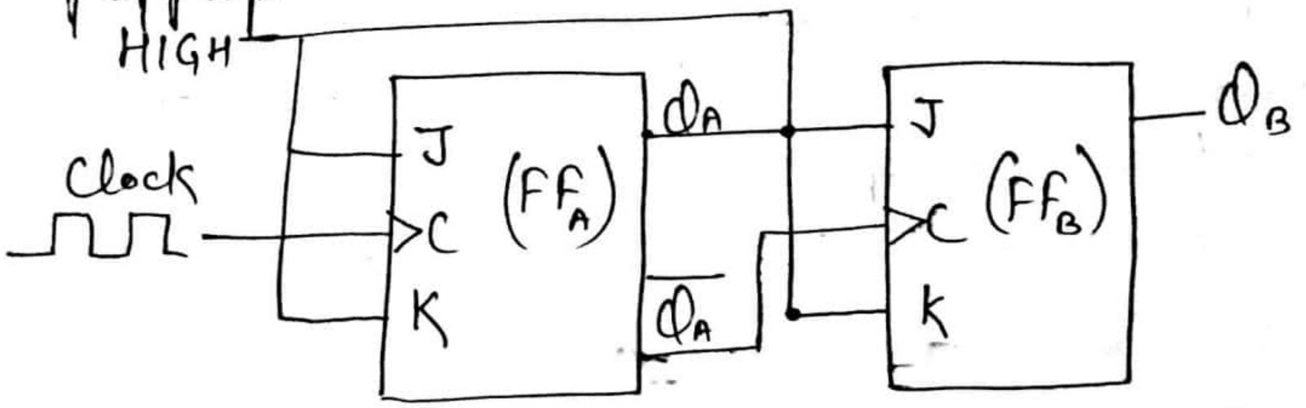
The clock to all flipflops in this counter is not applied at the same time instead of this, output of one flipflop is clock pulse applied to another flipflop.



Two bit Asynchronous Binary Counter

Initially $Q_A = 0$, $Q_B = 0$, when the first clock pulse is applied, the output of FF_A (Q_A) goes to high & $\overline{Q_A} = 0$.

After first clock pulse $Q_A = 1$, $Q_B = 0$

After second clock pulse $Q_A = 0$ & therefore $\overline{Q_A} = 1$

This $\overline{Q_A} = 1$ acts as clock pulse for FF_B and the output of FF_B $Q_B = 1$

Clockpulse	Q_B	Q_A	Count
0	0	0	0
1	0	1	1
2	1	0	2
3	1	1	3

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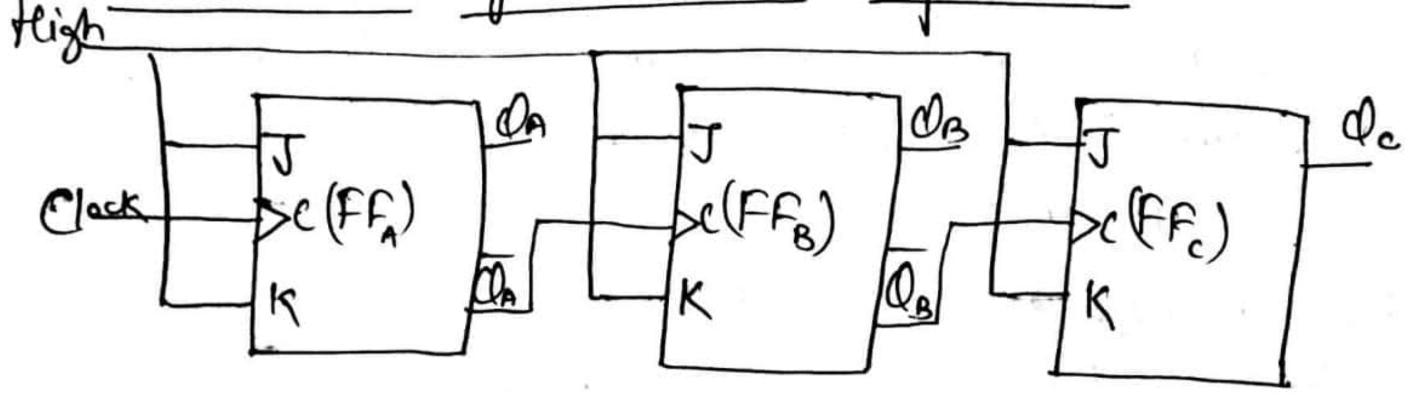
Three Bit Asynchronous Binary Counter →



Clock	Q_C	Q_B	Q_A	Counter
0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7

Modulus Counter OR Divide By N Counter

A four bit i.e. four flipflop counter is refessed as Mod 16 or modulus 16 counter since it has 16 states i.e. 2^4. Similarly a 3 bit flipflop counter is called Modulus 8 or mod 8 counter since it has 8 states only (2^3).

Modulus or Mod of counter is defined as numbes of states through which the counter progresses.

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But sometimes for a particular digital system we may require to construct a counter having Modulus 3, 5, 7 or 9 i.e not equal to normal binary number.

Asynchronous MOD 12 counter :-

For constructing a Mod-12 counter we require four flip flops (2^4). Mod-12 counter will count 12 states from 0000 to 1100.

Q_D	Q_C	Q_B	Q_A	Counter
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
0	0	0	0	Reset / Recycle

Already Zero

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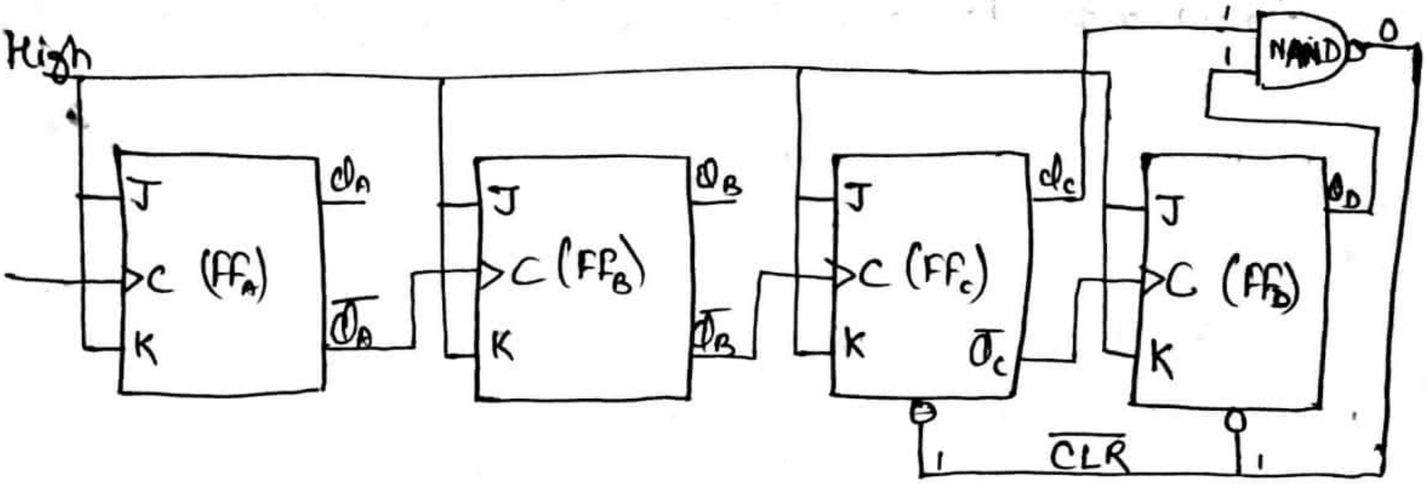


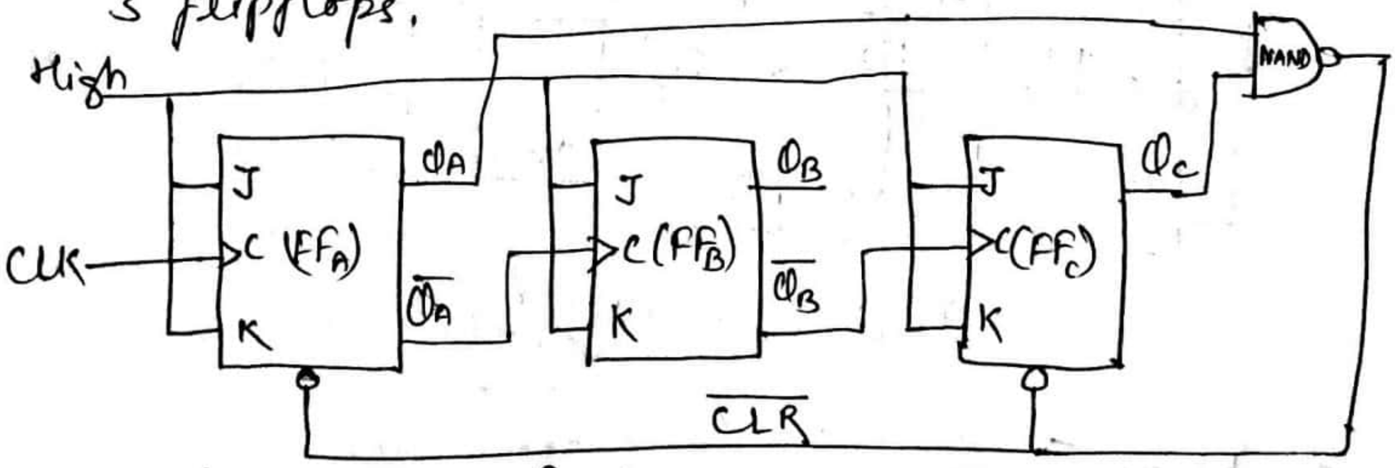
Asynchronous Mod-5 Counter ⇒

3 flip flops = 2^3 counts = 8 counts

2 flip flops = 2^2 counts = 4 counts

$$2^2 < 5 < 2^3 \text{ maximum}$$

For constructing Mod-5 counter, we require 3 flipflops.



Q_C	Q_B	Q_A	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
0	0	0	Reset

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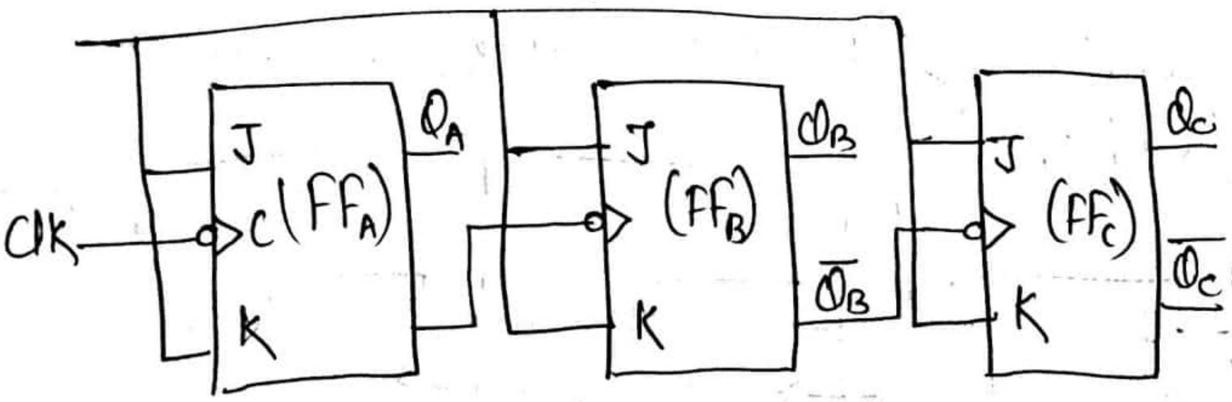
Q Draw Asynchronous Decade Counter / Mod-10 Counter

Asynchronous Down Counters

A down counter is a counter that will count downward from maximum to zero.

C	B	A	Counter
1	1	1	7
1	1	0	6
1	0	1	5
1	0	0	4
0	1	1	3
0	1	0	2
0	0	1	1
0	0	0	0



Mod-8 counter / Down Counter

* Negative Edge triggered clock pulse

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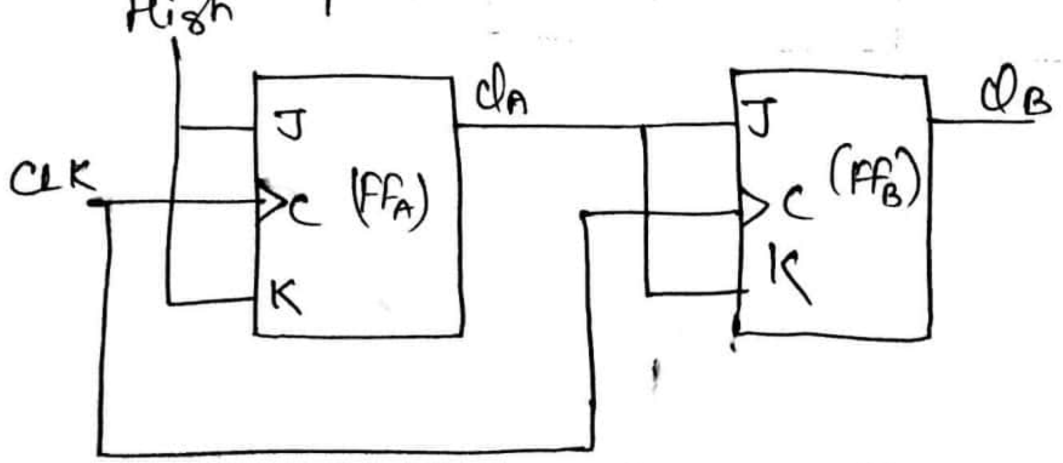
Synchronous Counter →

Synchronous means at the same time. In synchronous counters, clock pulse is applied to all the flipflops at the same time.

* Asynchronous counters are simple but speed is low, since output of one flipflop drives the other flipflop. Each flipflop has a delay time (i.e. time required for getting the output from the instant the input is applied) & when we use a number of flipflops, the total delay or cumulative delay is the sum of delay-time of each flipflop used. This results in speed limitation for asynchronous counter.

⇒ The speed of operation improves significantly if all the flipflops are clocked simultaneously as in case of synchronous counters.



Two bit Synchronous Binary Counter

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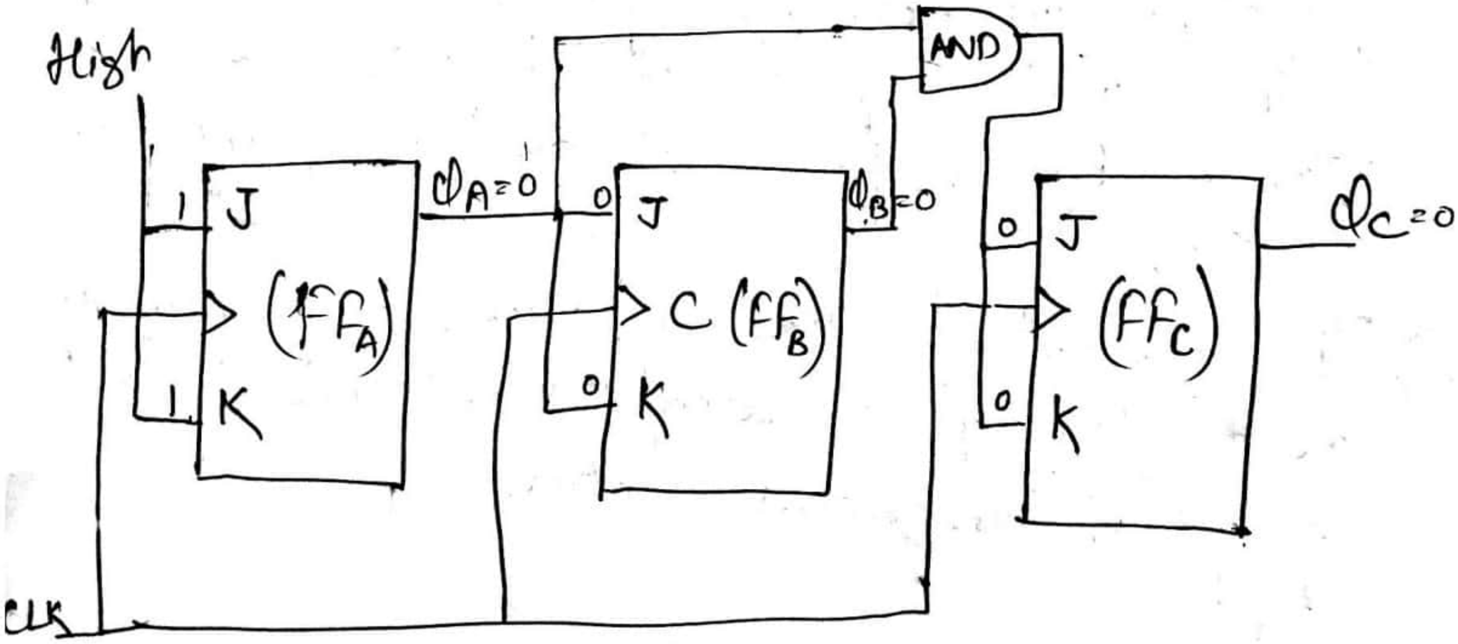
Three Bit Synchronous Binary Counter

Clock	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1



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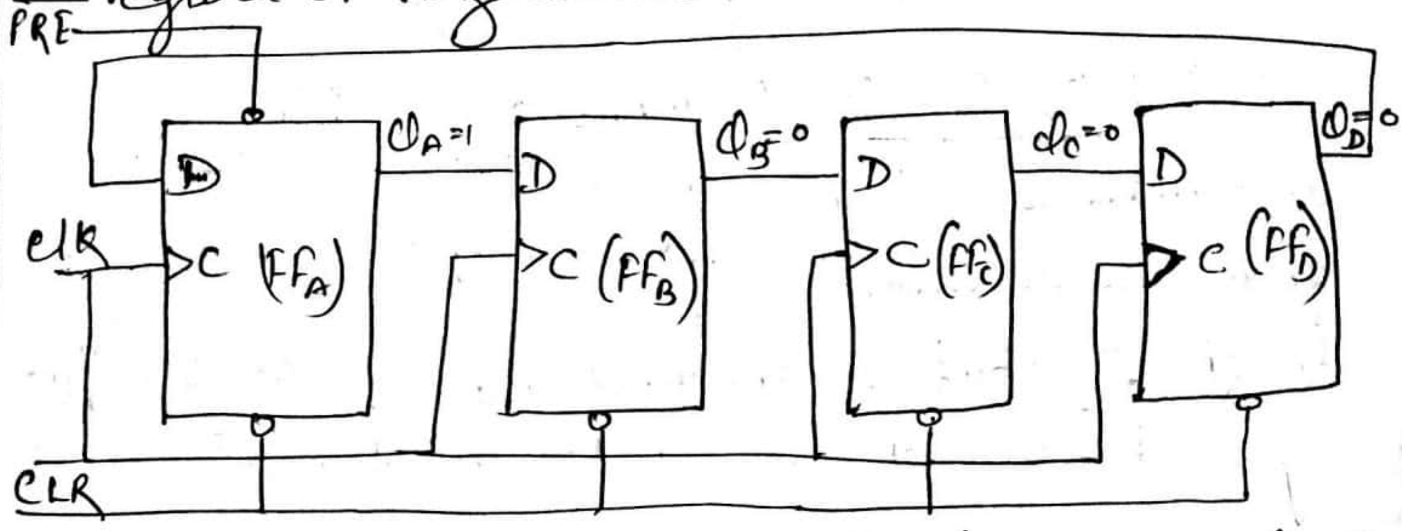
Ring Counters → It works on the principle of feedback.

Four bit Ring Counter → In this, 1 circulates around the register as long as clock pulse keeps on arriving. For this reason, these counters are called circulating register or ring counter.



It is constructed using D-flipflop. In D-flipflop

D = 0 , o/p = 0 (reset)

D = 1 , o/p = 1 (set)

Initially $Q_A = 1$ and other flipflops, $Q_B = Q_C = Q_D = 0$

After clockpulse	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1

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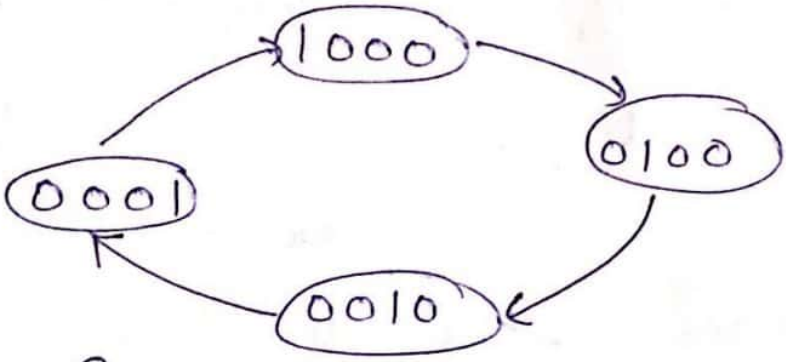
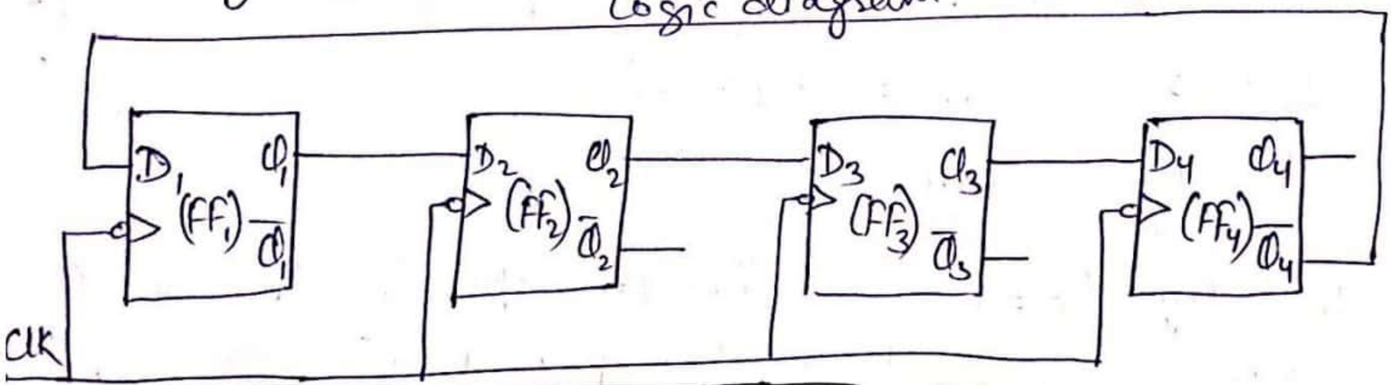


State diagram of 4 bit ring counter

Twisted Ring Counter / Johnson Counter ⇒

This counter is obtained by providing a feedback from the inverted output of the last flipflop to the D input of the first flipflop. The Q output of each stage is connected to the D input of next stage.

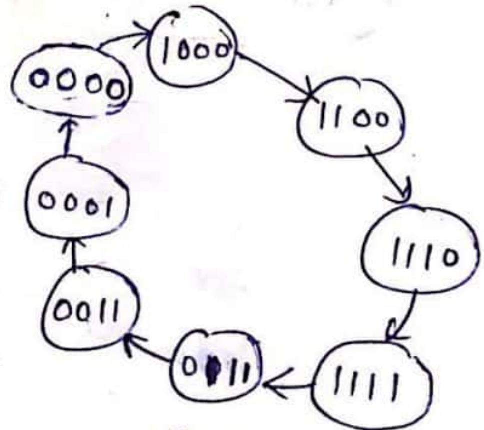
Logic diagram.



After clock pulse	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

Recycle

← sequence diagram



State diagram

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