1. Description

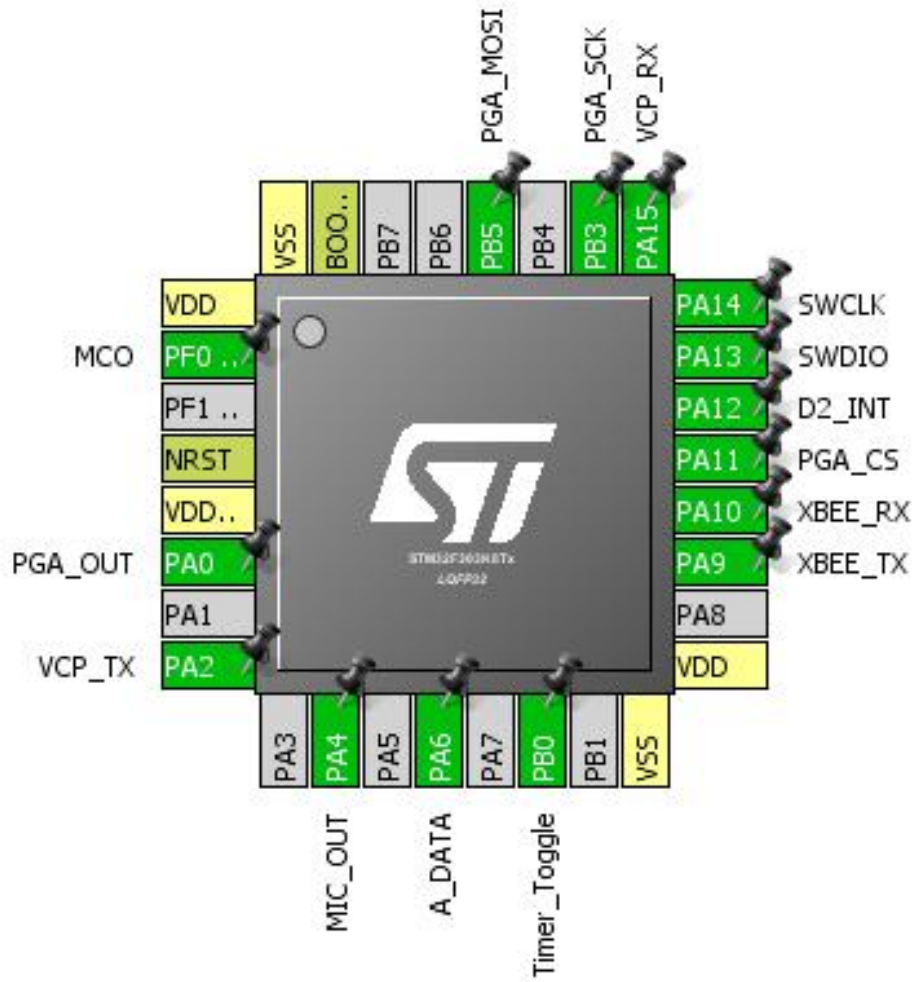
1.1. Project

Project Name	Smart_Mic_V01
Board Name	NUCLEO-F303K8
Generated with:	STM32CubeMX 4.26.1
Date	08/21/2018

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303K8Tx
MCU Package	LQFP32
MCU Pin number	32

2. Pinout Configuration

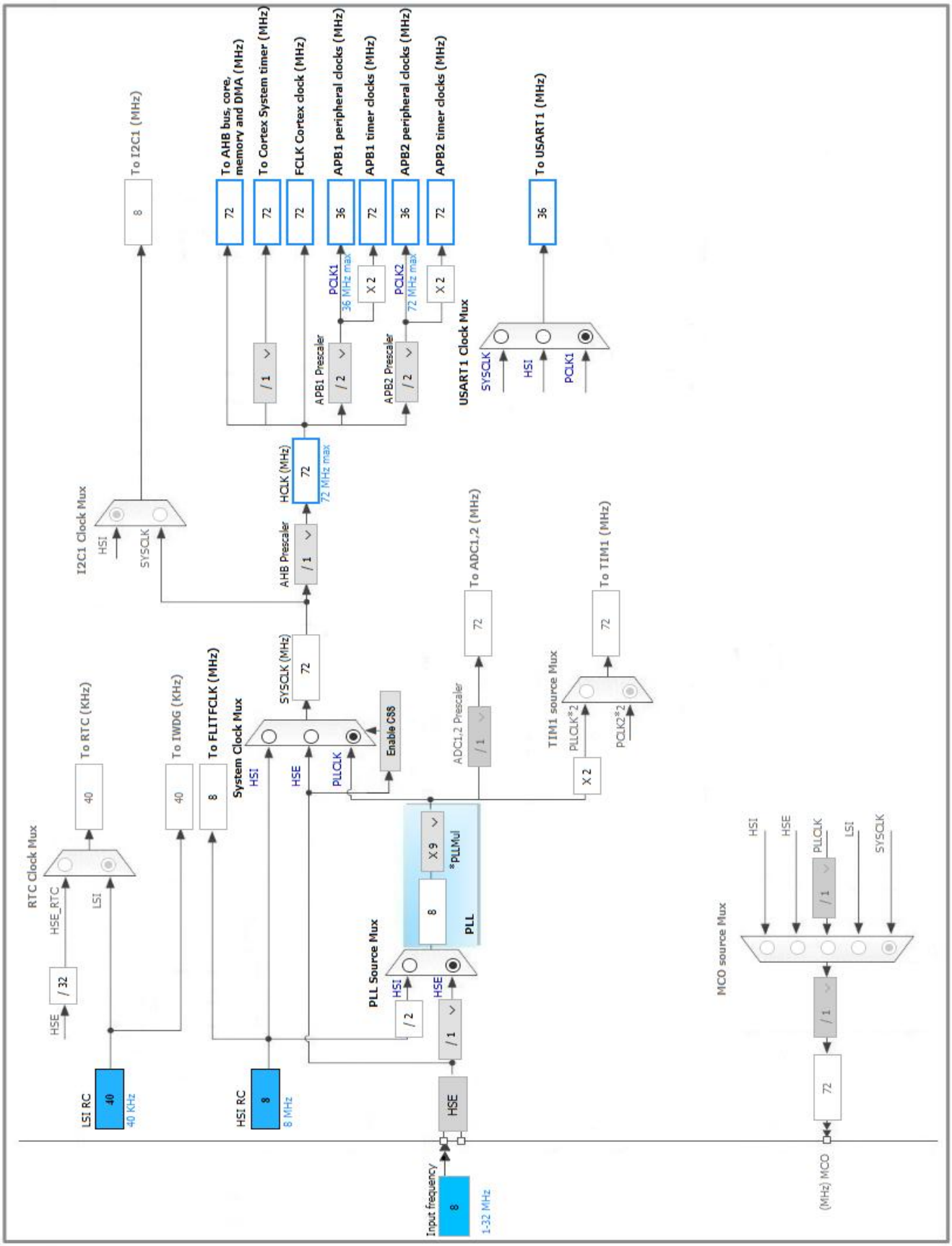


3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0 / OSC_IN	I/O	RCC_OSC_IN	MCO
4	NRST	Reset		
5	VDDA/VREF+	Power		
6	PA0	I/O	ADC1_IN1	PGA_OUT
8	PA2	I/O	USART2_TX	VCP_TX
10	PA4	I/O	DAC1_OUT1	MIC_OUT
12	PA6	I/O	DAC2_OUT1	A_DATA
14	PB0	I/O	TIM3_CH3	Timer_Toggle
16	VSS	Power		
17	VDD	Power		
19	PA9	I/O	USART1_TX	XBEE_TX
20	PA10	I/O	USART1_RX	XBEE_RX
21	PA11 *	I/O	GPIO_Output	PGA_CS
22	PA12 *	I/O	GPIO_Output	D2_INT
23	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
24	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
25	PA15	I/O	USART2_RX	VCP_RX
26	PB3	I/O	SPI1_SCK	PGA_SCK
28	PB5	I/O	SPI1_MOSI	PGA_MOSI
31	BOOT0	Boot		
32	VSS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Single-ended

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**7.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. DAC1

mode: OUT1 Configuration

5.2.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	**Timer 3 Trigger Out event ***
Wave generation mode	Disabled

5.3. DAC2

OUT1 Configuration: DAC Output switch Enable

5.3.1. Parameter Settings:

DAC Out1 Settings:

Trigger	None

5.4. RCC

High Speed Clock (HSE): BYPASS Clock Source

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.5. SPI1

Mode: Transmit Only Master

5.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**4.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

5.6. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.7. TIM3

Clock Source : Internal Clock

Channel3: Output Compare CH3

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**59 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

Output Compare Channel 3:

Mode	**Toggle on match ***

Pulse (16 bits value)	0
CH Polarity	High

5.8. USART1

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	**57600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.9. USART2

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	**57600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit

Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	PGA_OUT
DAC1	PA4	DAC1_OUT1	Analog mode	No pull up pull down	n/a	MIC_OUT
DAC2	PA6	DAC2_OUT1	Analog mode	No pull up pull down	n/a	A_DATA
RCC	PF0 / OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull up pull down	**High ***	PGA_SCK
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull up pull down	**High ***	PGA_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull up pull down	Low	Timer_Toggle
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull up pull down	**High ***	XBEE_TX
	PA10	USART1_RX	Alternate Function Push Pull	No pull up pull down	**High ***	XBEE_RX
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull up pull down	**High ***	VCP_TX
	PA15	USART2_RX	Alternate Function Push Pull	No pull up pull down	**High ***	VCP_RX
GPIO	PA11	GPIO_Output	Output Push Pull	No pull up pull down	**High ***	PGA_CS
	PA12	GPIO_Output	Output Push Pull	No pull up pull down	Low	D2_INT

6.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low
DAC1_CH1	DMA1_Channel3	Memory To Peripheral	**High ***
ADC1	DMA1_Channel1	Peripheral To Memory	**Very High ***

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_TX: DMA1_Channel7 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

DAC1_CH1: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word

Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	5	0
Pre-fetch fault, memory access fault	true	5	0
Undefined instruction or illegal state	true	5	0
System service call via SWI instruction	true	5	0
Debug monitor	true	5	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	1	0
DMA1 channel3 global interrupt	true	1	0
DMA1 channel4 global interrupt	true	5	0
DMA1 channel7 global interrupt	true	5	0
USART1 global interrupt / USART1 wake-up interrupt through EXT line 25	true	5	0
USART2 global interrupt / USART2 wake-up interrupt through EXT line 26	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM3 global interrupt	unused		
SPI1 global interrupt	unused		
TIM6 global and DAC1 underrun error interrupts	unused		
TIM7 global and DAC2 underrun error interrupts	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303K8Tx
Datasheet	025083_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Smart_Mic_V01
Project Folder	C:\WorkSpace\Atollic_WorkSpace\Smart_Mic_V01
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F3 V1.10.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report