VHDL files

LogicalStep_Lab3_top.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;


entity LogicalStep_Lab3_top is port (
  clkin_50                  : in      std_logic;
pb                                  : in      std_logic_vector(3 downto 0);
 sw                         : in  std_logic_vector(7 downto 0); -- The switch inputs
  leds                      : out std_logic_vector(7 downto 0);       -- for displaying the switch content
  seg7_data      : out std_logic_vector(6 downto 0); -- 7-bit outputs to a 7-segment
          seg7_char1  : out         std_logic;                                      -- seg7 digi selectors
          seg7_char2  : out         std_logic                                       -- seg7 digi selectors

);
end LogicalStep_Lab3_top;

architecture Energy_Monitor of LogicalStep_Lab3_top is
component Compx4 port(
a                                   : in      std_logic_vector(3 downto 0);
b                                   : in      std_logic_vector(3 downto 0);
gt                          : out std_logic;
eq                          : out std_logic;
lt                          : out std_logic
```

```
);
end component;
--
component segment7_mux port (
                clk :in std_logic :='0';
                DIN2 : in std_logic_vector(6 downto 0);
                DIN1 : in std_logic_vector(6 downto 0);
                DOUT : out std_logic_vector(6 downto 0);
                DIG2 :out std_logic;
                DIG1 :out std_logic
        );
        end component;

component SevenSegment port (
  hex           :  in  std_logic_vector(3 downto 0);   -- The 4 bit data to be displayed
  sevenseg      :  out std_logic_vector(6 downto 0)    -- 7-bit outputs to a 7-segment
  );



  end component;
component mode_control port (
sw: in std_logic_vector (3 downto 0);
WindowOpen: in std_logic;
DoorOpen: in std_logic;
CGTD: in std_logic;
```

```
CLED: in std_logic;
CEQD: in std_logic;
VacationMode: in std_logic;
AC_ON: out std_logic;
BLOWER_ON: out std_logic;
FURNACE_ON: out std_logic;
SYSTEM_AT_TEMP: out std_logic;
Desired_temp: out std_logic_vector (3 downto 0)
        );
        end component;
-- Components Used
------------------------------------------------------------------
```

```
signal Current_Temp: std_logic_vector (3 downto 0);
signal Desired_Temp: std_logic_vector (3 downto 0);
signal VacationMode: std_logic;
signal MC_TESTMODE: std_logic;
signal WindowOpen: std_logic;
signal DoorOpen: std_logic;
signal FURNACE_ON: std_logic;
signal SYSTEM_AT_TEMP: std_logic;
signal AC_ON : std_logic;
signal BLOWER_ON: std_logic;
```

```
signal TEST_PASS: std_logic;
signal VACATION_MODE: std_logic;

signal seg7_A    : std_logic_vector(6 downto 0);
signal seg7_B                : std_logic_vector(6 downto 0);
signal CEQD, CGTD, CLED : std_logic;


begin

Current_Temp <= sw (3 downto 0);
VacationMode <= not pb(3);
MC_TESTMODE <= not pb(2);
WindowOpen <= pb(1);
DoorOpen <= pb(0);
leds(0)<= FURNACE_ON ;
leds(1)<=SYSTEM_AT_TEMP;
leds(2)<= AC_ON ;
leds(3)<=BLOWER_ON;
leds(4)<= DoorOpen;
leds(5)<= WindowOpen;
leds(7)<= VacationMode;
INST1: SevenSegment port map(Current_Temp, seg7_A);
INST2: SevenSegment port map(Desired_temp, seg7_B);
INST3: segment7_mux port map(clkin_50, seg7_A, seg7_B,seg7_data, seg7_char2, seg7_char1);
INST4: Compx4 port map (Current_Temp, Desired_Temp, CGTD, CEQD, CLED);
```

```
INST5: mode_control port map (sw(7 downto 4),WindowOpen, DoorOpen, CGTD, CLED, CEQD, VacationMode, AC_ON, BLOWER_ON, FURNACE_ON, SYSTEM_AT_TEMP,
Desired_temp);

PROCESS (sw, CEQD, CGTD, CLED, pb(2)) is

variable EQ_PASS, GE_PASS, LE_PASS :std_logic := '0';

begin

        IF ((sw(3 downto 0) =sw (7 downto 4)) AND (CEQD='1')) THEN

        EQ_PASS :='1';

        GE_PASS :='0';

        LE_PASS :='0';

        ELSIF ((sw(3 downto 0) >=sw (7 downto 4)) AND (CGTD='1')) THEN

        EQ_PASS :='0';

        GE_PASS :='1';

        LE_PASS :='0';

        ELSIF ((sw(3 downto 0) <=sw (7 downto 4)) AND (CLED='1')) THEN

        EQ_PASS :='0';

        GE_PASS :='0';

        LE_PASS :='1';

        ELSE

        EQ_PASS :='0';

        GE_PASS :='0';

        LE_PASS :='0';

        END IF;

        TEST_PASS<= MC_TESTMODE AND ( EQ_PASS OR GE_PASS or LE_PASS);

        leds(6) <= TEST_PASS;

end process;

end Energy_Monitor;
```

Compx1.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity Compx1 is port
(
a                                   : in      std_logic;
b                                   : in      std_logic;
gt                                  : out std_logic; --a greater than b
eq                                  : out std_logic; -- a equals b
lt                                  : out std_logic   -- a less than b
);
end Compx1;

architecture dataflow of Compx1 is
begin
        gt<=a and (not b);
        eq<=a xnor b;
        lt<=b and (not a);
end dataflow;
```

Compx4.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity Compx4 is port
(
a                                   : in      std_logic_vector(3 downto 0);
b                                   : in      std_logic_vector(3 downto 0);
gt                          : out std_logic;
eq                          : out std_logic;
lt                          : out std_logic
);
end Compx4;

architecture Structural of Compx4 is
component Compx1 port(
a                                   : in      std_logic;
b                                   : in      std_logic;
gt                          : out std_logic; --a greater than b
eq                          : out std_logic; -- a equals b
lt                          : out std_logic   -- a less than b
);
end component;
```

```
signal greater: std_logic_vector (3 downto 0);
signal equal: std_logic_vector (3 downto 0);
signal less: std_logic_vector (3 downto 0);


begin
Comp0:Compx1 port map (a(0),b(0), greater(0),equal(0),less(0));
Comp1:Compx1 port map (a(1),b(1), greater(1),equal(1),less(1));
Comp2:Compx1 port map (a(2),b(2), greater(2),equal(2),less(2));
Comp3:Compx1 port map (a(3),b(3), greater(3),equal(3),less(3));
gt<= greater(3) or (equal(3) and greater(2)) or(equal(3) and equal(2) and greater(1))or(equal(3) and equal(2) and equal(1) and greater(0));
lt<=less(3) or (equal(3) and less(2)) or(equal(3) and equal(2) and less(1))or(equal(3) and equal(2) and equal(1) and less(0));
eq<=equal(0) and equal(1) and equal(2) and equal(3);
end Structural;
```

mode_control.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity mode_control is port
(
sw: in std_logic_vector (3 downto 0);
WindowOpen: in std_logic;
DoorOpen: in std_logic;
CGTD: in std_logic;
CLED: in std_logic;
CEQD: in std_logic;
VacationMode: in std_logic;
AC_ON: out std_logic;
BLOWER_ON: out std_logic;
FURNACE_ON: out std_logic;
SYSTEM_AT_TEMP: out std_logic;
Desired_temp: out std_logic_vector (3 downto 0)
);
end mode_control;
architecture dataflow of mode_control is
signal a,b:std_logic;
begin
a <= CGTD and (not WindowOpen) and (not DoorOpen);
BLOWER_ON <= (a or b);
b <= CLED and (not WindowOpen) and (not DoorOpen);
```

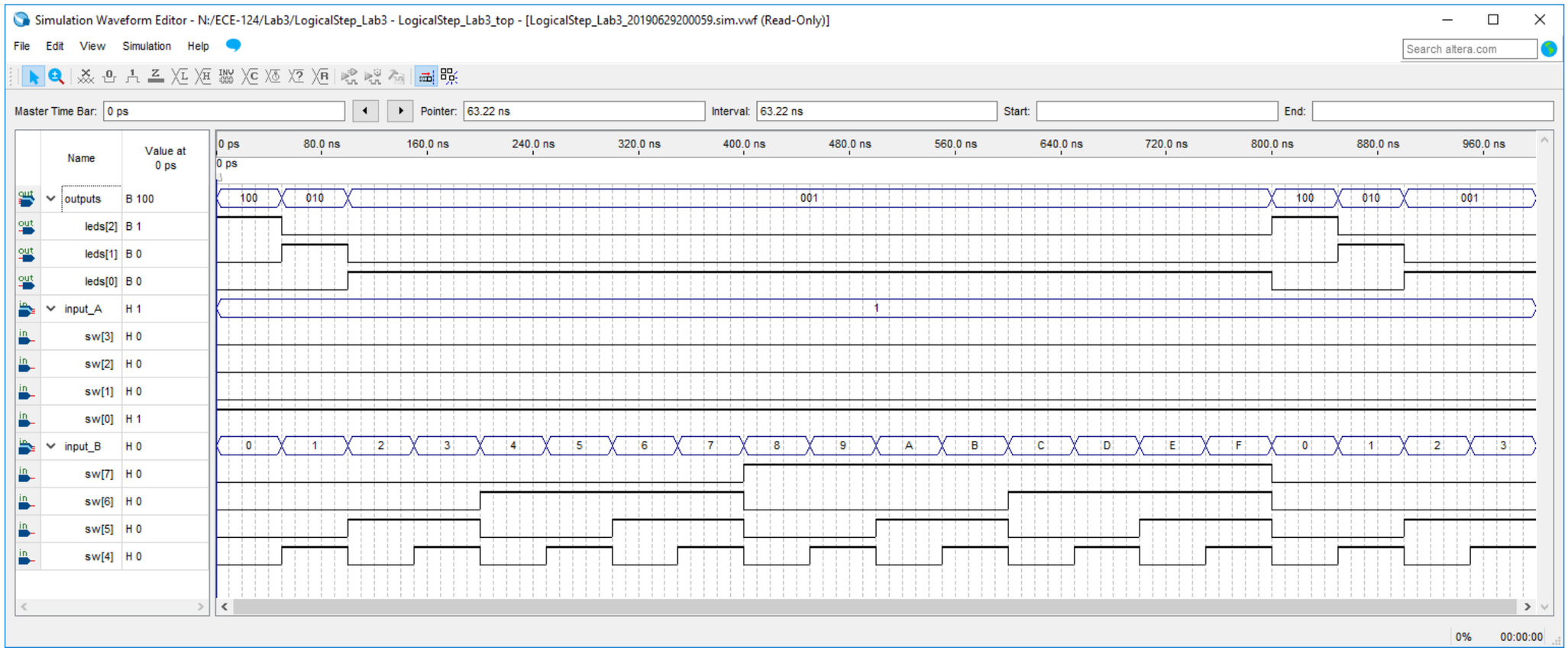
```
AC_ON <=a;
FURNACE_ON<=b;
SYSTEM_AT_TEMP<= CEQD;
PROCESS(VacationMode) is
begin
case VacationMode is
when'1' =>Desired_temp <= "0100" ;  --when vacationmode is on, set temperature to "0100
when'0' =>Desired_Temp <= sw (3 downto 0);  --when vacation mode is off, use sw to set desired temperature.
end case;
end process;
end dataflow;
```

Truth Table for 4-bit Comparator

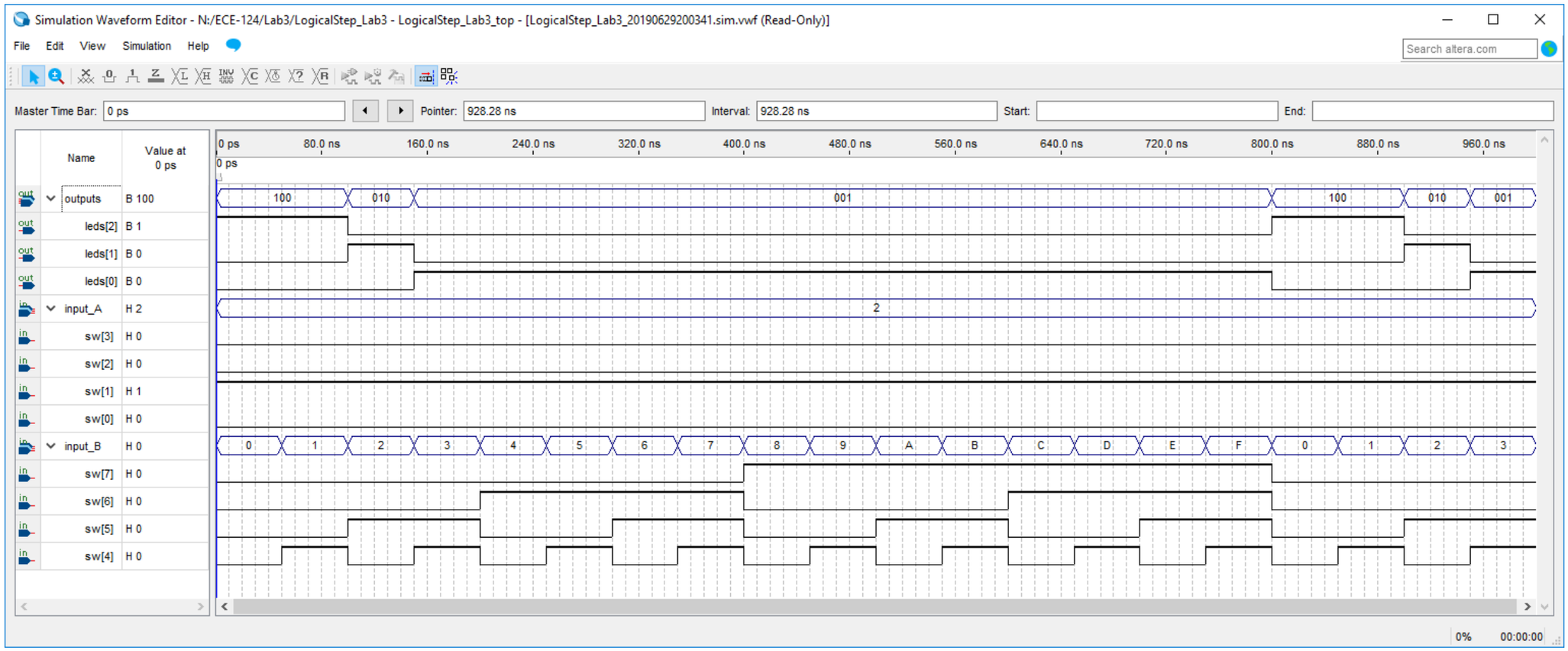
A3>B3	A3=B3	A3<B3	A2>B2	A2=B2	A2<B2	A1>B1	A1=B1	A1<B1	A0>B0	A0=B0	A0<B0	A>B	A=B	A<B
1	X	X	X	X	X	X	X	X	X	X	X	1	0	0
X	1	X	X	1	X	X	1	X	X	1	X	0	1	0
X	X	1	X	X	X	X	X	X	X	X	X	0	0	1
X	1	X	1	X	X	X	X	X	X	X	X	1	0	0
X	1	X	X	1	X	1	X	X	X	X	X	1	0	0
X	1	X	X	1	X	X	1	X	1	X	X	1	0	0
X	1	X	X	X	1	X	X	X	X	X	X	0	0	1
X	1	X	X	1	X	X	X	1	X	X	X	0	0	1
X	1	X	X	1	X	X	1	X	X	X	1	0	0	1

Simulation of Comparator

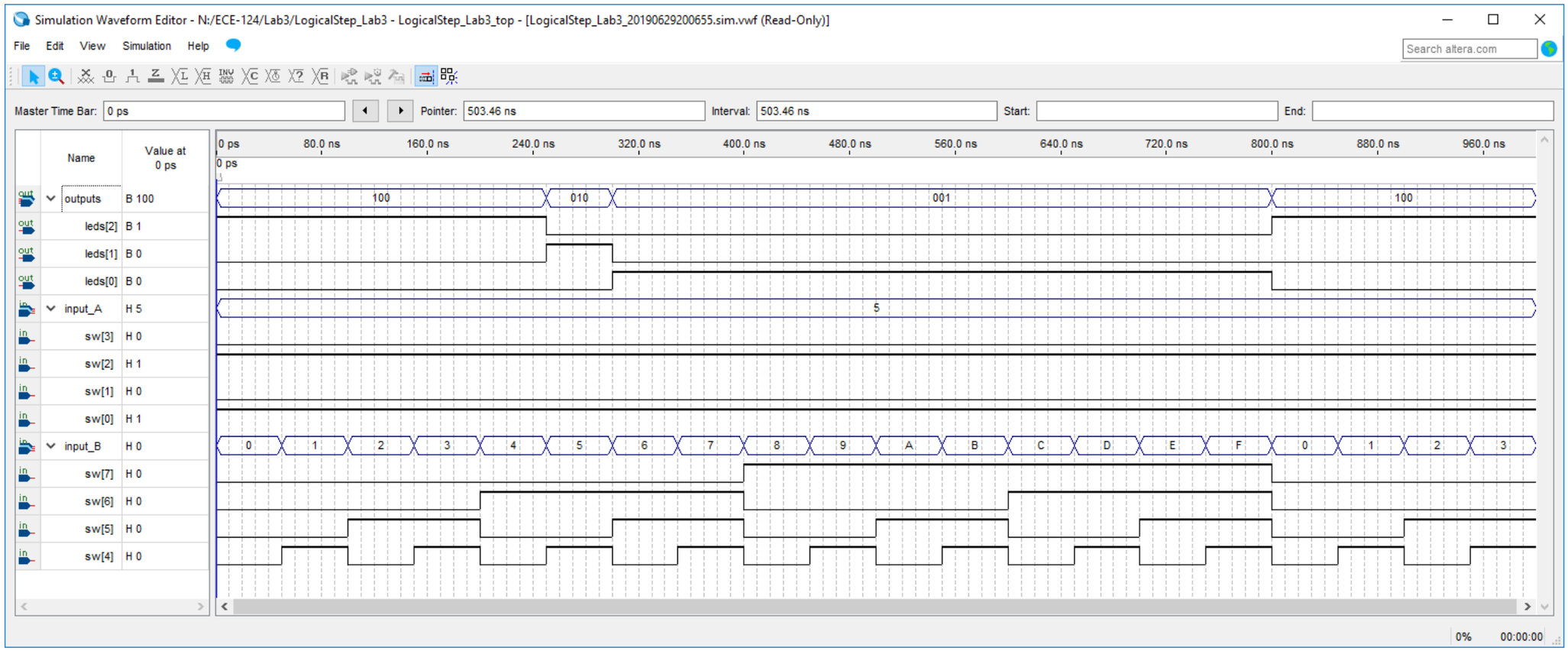
S1



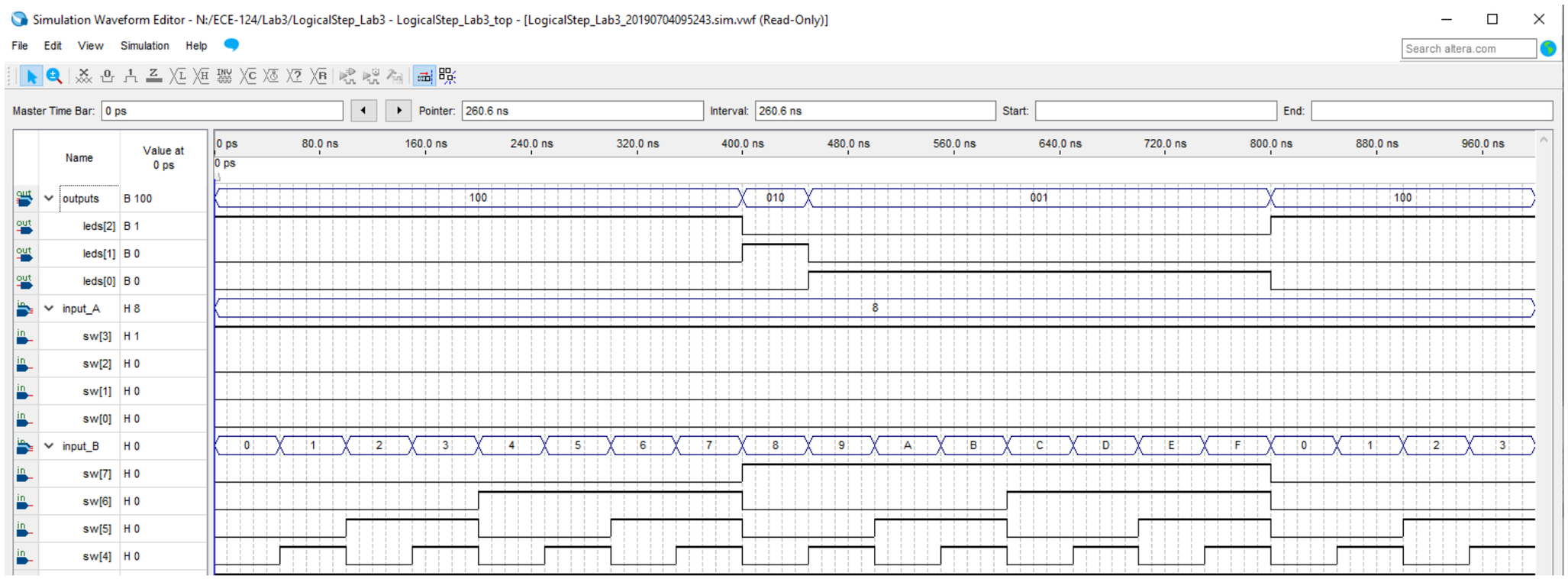
S2


Simulation Waveform Editor - N:/ECE-124/Lab3/LogicalStep_Lab3 - LogicalStep_Lab3_top - [LogicalStep_Lab3_20190629200341.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 928.28 ns
Interval: 928.28 ns
Start:
End:
Name
Value at 0 ps
outputs B 100
leds[2] B 1
leds[1] B 0
leds[0] B 0
input_A H 2
sw[3] H 0
sw[2] H 0
sw[1] H 1
sw[0] H 0
input_B H 0
sw[7] H 0
sw[6] H 0
sw[5] H 0
sw[4] H 0
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
960.0 ns
100
010
001
2
0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F
0%
00:00:00

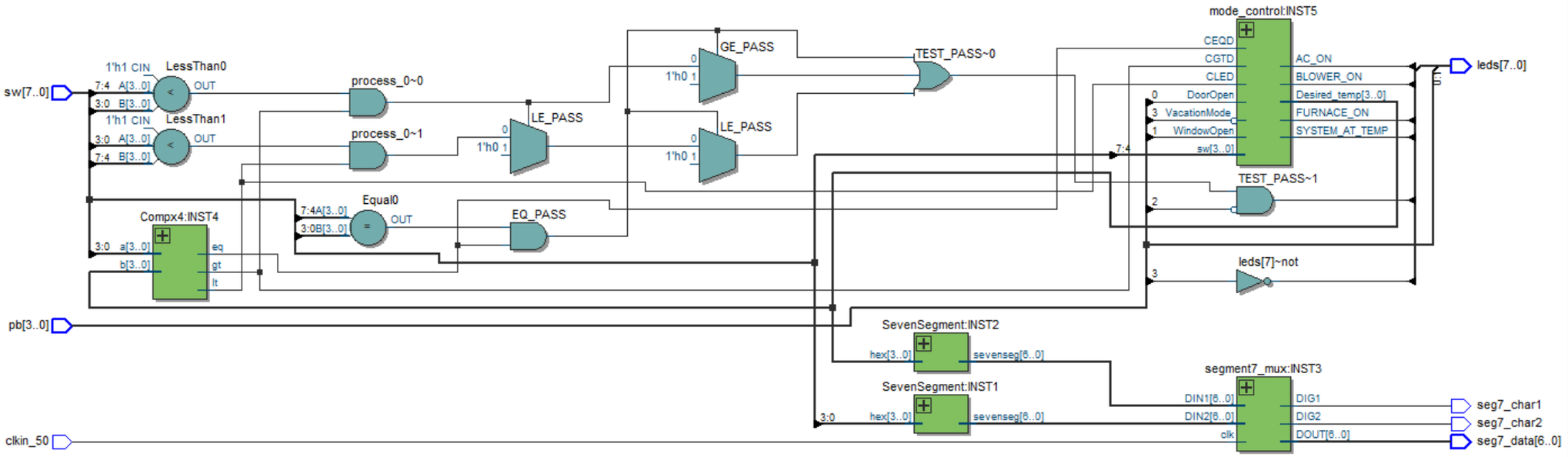
S3


Simulation Waveform Editor - N:/ECE-124/Lab3/LogicalStep_Lab3 - LogicalStep_Lab3_top - [LogicalStep_Lab3_20190629200655.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 503.46 ns
Interval: 503.46 ns
Start:
End:
Name
Value at 0 ps
outputs B 100
leds[2] B 1
leds[1] B 0
leds[0] B 0
input_A H 5
sw[3] H 0
sw[2] H 1
sw[1] H 0
sw[0] H 1
input_B H 0
sw[7] H 0
sw[6] H 0
sw[5] H 0
sw[4] H 0
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
960.0 ns
100
010
001
100
5
0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3
0%
00:00:00

S4


Simulation Waveform Editor - N:/ECE-124/Lab3/LogicalStep_Lab3 - LogicalStep_Lab3_top - [LogicalStep_Lab3_20190704095243.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 260.6 ns
Interval: 260.6 ns
Start:
End:
Name
Value at 0 ps
outputs B 100
leds[2] B 1
leds[1] B 0
leds[0] B 0
input_A H 8
sw[3] H 1
sw[2] H 0
sw[1] H 0
sw[0] H 0
input_B H 0
sw[7] H 0
sw[6] H 0
sw[5] H 0
sw[4] H 0
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
960.0 ns
100
010
001
100
8
0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3

RTL view


mode_control:INST5
CEQD
CGTD
CLED
DoorOpen
VacationMode
WindowOpen
sw[3..0]
AC_ON
BLOWER_ON
Desired_temp[3..0]
FURNACE_ON
SYSTEM_AT_TEMP
leds[7..0]
TEST_PASS~0
TEST_PASS~1
leds[7]~not
GE_PASS
LE_PASS
LE_PASS
process_0~0
process_0~1
LessThan0
LessThan1
1'h1 CIN
A[3..0]
B[3..0]
OUT
Equal0
EQ_PASS
Compx4:INST4
a[3..0]
b[3..0]
eq
gt
lt
sw[7..0]
pb[3..0]
clkin_50
SevenSegment:INST2
SevenSegment:INST1
hex[3..0]
sevenseg[6..0]
segment7_mux:INST3
DIN1[6..0]
DIN2[6..0]
clk
DIG1
DIG2
DOUT[6..0]
seg7_char1
seg7_char2
seg7_data[6..0]

Total Design Logic Elements Used: 60/8064

Flow Summary	
Flow Status	Successful - Thu Jul 04 10:45:25 2019
Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Standard Edition
Revision Name	LogicalStep_Lab3_top
Top-level Entity Name	LogicalStep_Lab3_top
Family	MAX 10
Device	10M08SAE144C8G
Timing Models	Final
Total logic elements	60 / 8,064 (< 1 %)
Total combinational functions	60 / 8,064 (< 1 %)
Dedicated logic registers	11 / 8,064 (< 1 %)
Total registers	11
Total pins	30 / 101 (30 %)
Total virtual pins	0
Total memory bits	0 / 387,072 (0 %)
Embedded Multiplier 9-bit elements	0 / 48 (0 %)
Total PLLs	0 / 1 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 1 (0 %)