

Structural VHDL used in top level VHDL design

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Quartus Prime Standard Edition - N:/ECE-124/Lab2/LogicalStep_Lab2 - LogicalStep_Lab2_top
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LogicalStep_Lab2_top.vhd

1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6
7  entity LogicalStep_Lab2_top is port (
8      clk_in_50      : in  std_logic;
9      pb             : in  std_logic_vector(3 downto 0);
10     sw              : in  std_logic_vector(7 downto 0); -- The switch inputs
11     leds            : out std_logic_vector(7 downto 0); -- for displaying the switch content
12     seg7_data       : out std_logic_vector(6 downto 0); -- 7-bit outputs to a 7-segment
13     seg7_char1      : out std_logic;                  -- seg7 digit1 selector
14     seg7_char2      : out std_logic;                  -- seg7 digit2 selector
15 );
16 end LogicalStep_Lab2_top;
17
18 architecture SimpleCircuit of LogicalStep_Lab2_top is
19     -- Components Used ---
20     -----
21     component SevenSegment port (
22         hex      : in  std_logic_vector(3 downto 0); -- The 4 bit data to be displayed
23         sevenseg : out std_logic_vector(6 downto 0); -- 7-bit outputs to a 7-segment
24     );
25
26 end component;
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30
31     component segment7_mux port (
32         clk : in std_logic := '0';
33         DIN2 : in std_logic_vector(6 downto 0);
34         DIN1 : in std_logic_vector(6 downto 0);
35         DOUT : out std_logic_vector(6 downto 0);
36         DIG2 : out std_logic;
37         DIG1 : out std_logic;
38     );
39 end component;
40
41
42     component my_mux port (
43         input1 : in  std_logic_vector(3 downto 0); --pb
44         input2 : in  std_logic_vector(7 downto 0); --logic result
45         input3 : in  std_logic_vector(4 downto 0); --bit add
46         input4 : in  std_logic_vector(3 downto 0); --first 7seg after bit add
47         input5 : in  std_logic_vector(3 downto 0); --first 4 bit input
48         input6 : in  std_logic_vector(3 downto 0); --second 4 bit input
49         output1 : out std_logic_vector(3 downto 0); --hex_A
50         output2 : out std_logic_vector(3 downto 0); --hex_B
51         output3 : out std_logic_vector(7 downto 0); --leds
52     );
53 end component;
54
55     component bit_add port (
56         input1 : in  std_logic_vector(3 downto 0); --first 4-bit input
57         input2 : in  std_logic_vector(3 downto 0); --second 4--bit input
58         output1 : out std_logic_vector(4 downto 0); --result in a 5-bit number
59     );
60 end component;
61
62     component hex_logic port (
63         input1 : in  std_logic_vector(3 downto 0); --first 4-bit input
64         input2 : in  std_logic_vector(3 downto 0); --second 4--bit input
65         input3 : in  std_logic_vector(3 downto 0); --pb
66         output1 : out std_logic_vector(7 downto 0); --concat "0000" with logic output
67     );
68 end component;
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```

Quartus Prime Standard Edition - N:/ECE-124/Lab2/LogicalStep_Lab2 - LogicalStep_Lab2_top
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LogicalStep_Lab2_top.vhd
267
268

36      DOUT : out std_logic_vector(6 downto 0);
37      DIG2 :out std_logic;
38      DIG1 :out std_logic
39  );
40  end component;
41
42  component my_mux port (
43      input1      : in std_logic_vector(3 downto 0); --pb
44      input2      : in std_logic_vector(7 downto 0); --logic result
45      input3      : in std_logic_vector(4 downto 0); --bit add
46      input4      : in std_logic_vector(3 downto 0); --first 7seg after bit add
47      input5      : in std_logic_vector(3 downto 0); --first 4 bit input
48      input6      : in std_logic_vector(3 downto 0); --second 4 bit input
49      output1     : out std_logic_vector(3 downto 0); --hex_A
50      output2     : out std_logic_vector(3 downto 0); --hex_B
51      output3     : out std_logic_vector(7 downto 0) --leds
52  );
53  end component;
54
55  component bit_add port (
56      input1      : in std_logic_vector(3 downto 0); --first 4-bit input
57      input2      : in std_logic_vector(3 downto 0); --second 4--bit input
58      output1     : out std_logic_vector(4 downto 0) --result in a 5-bit number
59  );
60  end component;
61
62  component hex_logic port (
63      input1      : in std_logic_vector(3 downto 0); --first 4-bit input
64      input2      : in std_logic_vector(3 downto 0); --second 4--bit input
65      input3      : in std_logic_vector(3 downto 0); --pb
66      output1     : out std_logic_vector(7 downto 0) --concat "0000" with logic output
67  );
68  end component;
69
70  -- Create any signals, or temporary variables to be used
71  --
72  -- std_logic_vector is a signal which can be used for logic operations such as OR, AND, NOT, XOR
73  --
74  signal seg7_A      : std_logic_vector(6 downto 0);
75  signal hex_A       : std_logic_vector(3 downto 0);
76  signal hex_B       : std_logic_vector(3 downto 0);
77  signal seg7_B      : std_logic_vector(6 downto 0);
78  signal temp1       : std_logic_vector(3 downto 0); --first 4-bit input
79  signal temp2       : std_logic_vector(3 downto 0); --second 4--bit input
80
81  signal logic_result : std_logic_vector(7 downto 0);
82  signal add_result1  : std_logic_vector(4 downto 0); -- 4 bits + 4 bit is a 5-bit number
83  signal add_result2  : std_logic_vector(3 downto 0); --the value shouble be shown in the fitst 7seg(the
84  -- Here the circuit begins
85
86  begin
87      temp1<= sw(3 downto 0); --store the inputs
88      temp2<= sw(7 downto 4);
89      add_result2<= "0001" when add_result1(4) = '1' else --determine the output on the first 7seg after addi
90                  "0000" when add_result1(4) = '0';
91      INST1: SevenSegment port map(hex_A, seg7_A);
92      INST2: SevenSegment port map(hex_B, seg7_B);
93      INST3: segment7_mux port map(clkin_50, seg7_A, seg7_B, seg7_data, seg7_char2, seg7_char1);
94      INST4: hex_logic port map(temp1, temp2, pb, logic_result);
95      INST5: bit_add port map(temp1, temp2, add_result1);
96      INST6: my_mux port map(pb, logic_result, add_result1, add_result2, temp1, temp2, hex_A, hex_B, leds);
97
98  end simplecircuit;
99
100
101

```

100% 00:00:50

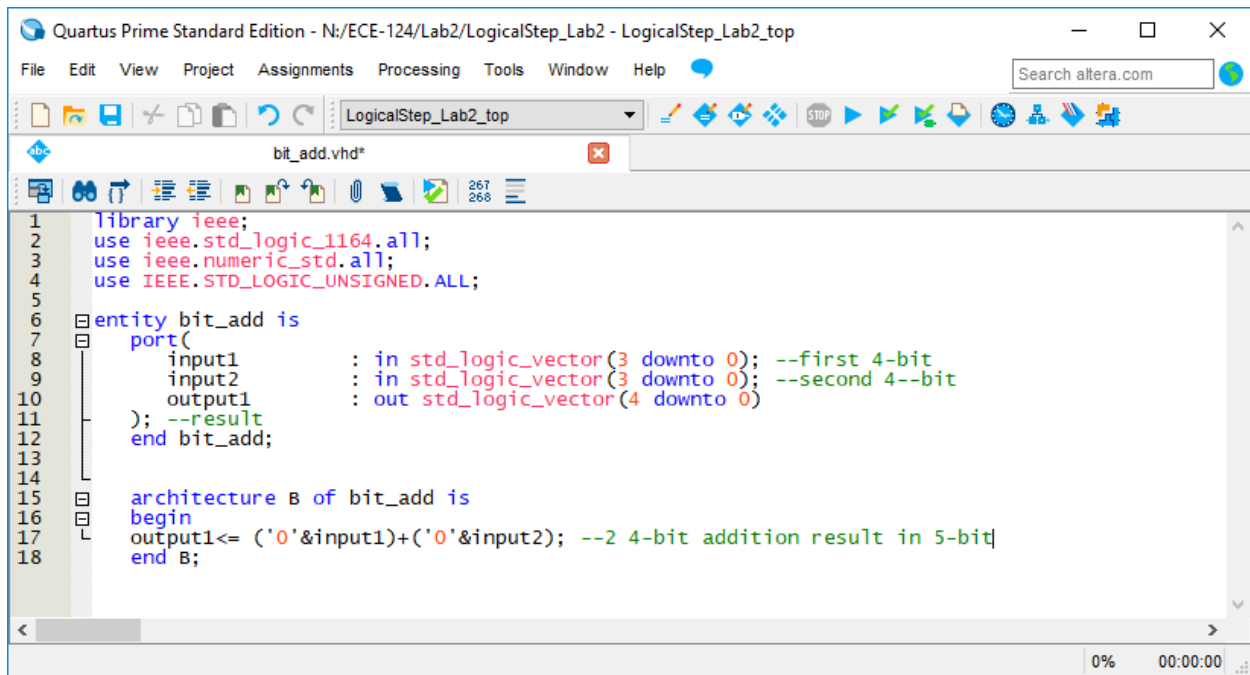
Sub-block my_mux

```
Quartus Prime Standard Edition - N:/ECE-124/Lab2/LogicalStep_Lab2 - LogicalStep_Lab2_top
File Edit View Project Assignments Processing Tools Window Help Search altera.com

LogicalStep_Lab2_top
my_mux.vhd
267
268

1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.numeric_std.all;
4 use IEEE.STD_LOGIC_UNSIGNED.ALL;
5 entity my_mux is
6 port(
7     input1      : in std_logic_vector(3 downto 0); --pb
8     input2      : in std_logic_vector(7 downto 0); --logic
9     input3      : in std_logic_vector(4 downto 0); --bit add
10    input4      : in std_logic_vector(3 downto 0); --the value should be shown in the first(the one on the right) 7seg
11    input5      : in std_logic_vector(3 downto 0); --first 4 bit input
12    input6      : in std_logic_vector(3 downto 0); --second 4 bit input
13    output1     : out std_logic_vector(3 downto 0); --hex_A
14    output2     : out std_logic_vector(3 downto 0); --hex_B
15    output3     : out std_logic_vector(7 downto 0) --leds
16 );
17 end my_mux;
18
19 architecture A of my_mux is
20 begin
21 process(input1)
22 begin
23 case input1 is
24 when "0111" => output3 <= ("000"&input3); --when PB4 is pressed, bit-add result should be shown
25               output1 <= input3(3 downto 0);
26               output2 <= input4(3 downto 0);
27 when "1110" => output3 <= input2; --PB0 is pressed, logical AND is applied to the inputs, shown in leds
28               output1 <= input5(3 downto 0);
29               output2 <= input6(3 downto 0);
30 when "1101" => output3 <= input2; --when PB1 is pressed, logical OR is applied
31               output1 <= input5(3 downto 0);
32               output2 <= input6(3 downto 0);
33 when "1011" => output3 <= input2; --when PB2 is pressed, logical XOR is applied
34               output1 <= input5(3 downto 0);
35               output2 <= input6(3 downto 0);
36 when "1111" => output3 <= "00000000"; --PBs are not pressed, nothing is done, two 7segs show the result respectively, leds are off
37               output1 <= input5(3 downto 0);
38               output2 <= input6(3 downto 0);
39 when others => output3 <= "11111111"; --more than 2 PBs are pressed, show error messages!!!
40               output1 <= "1000";
41               output2 <= "1000";
42 end case;
43 end process;
44 end A;
```

Sub-block bit_add



Quartus Prime Standard Edition - N:/ECE-124/Lab2/LogicalStep_Lab2 - LogicalStep_Lab2_top

File Edit View Project Assignments Processing Tools Window Help

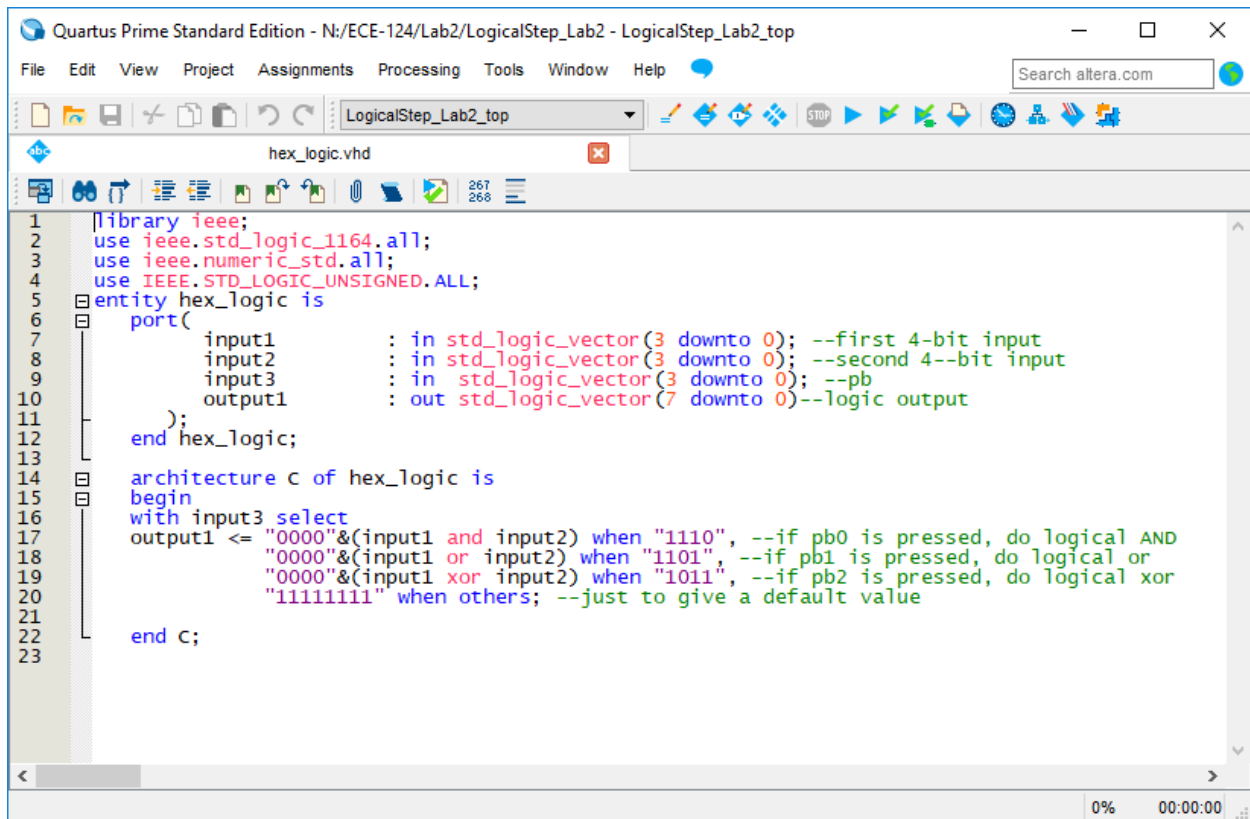
LogicalStep_Lab2_top

bit_add.vhd*

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6  entity bit_add is
7  port(
8      input1      : in std_logic_vector(3 downto 0); --first 4-bit
9      input2      : in std_logic_vector(3 downto 0); --second 4--bit
10     output1     : out std_logic_vector(4 downto 0)
11 ); --result
12 end bit_add;
13
14
15 architecture B of bit_add is
16 begin
17     output1<= ('0'&input1)+('0'&input2); --2 4-bit addition result in 5-bit
18 end B;
```

0% 00:00:00

Sub-block hex_logic



The screenshot shows the Quartus Prime Standard Edition interface. The title bar reads "Quartus Prime Standard Edition - N:/ECE-124/Lab2/LogicalStep_Lab2 - LogicalStep_Lab2_top". The menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. A search bar on the right contains "Search altera.com". The toolbar shows various icons for file operations and simulation. The main editor window displays the VHDL code for "hex_logic.vhd". The code defines an entity "hex_logic" with three 4-bit inputs (input1, input2, input3) and one 8-bit output (output1). The architecture "c" uses a case statement to perform logical operations based on the value of input3.

```
1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.numeric_std.all;
4 use IEEE.STD_LOGIC_UNSIGNED.ALL;
5 entity hex_logic is
6     port(
7         input1      : in std_logic_vector(3 downto 0); --first 4-bit input
8         input2      : in std_logic_vector(3 downto 0); --second 4--bit input
9         input3      : in std_logic_vector(3 downto 0); --pb
10        output1     : out std_logic_vector(7 downto 0)--logic output
11    );
12 end hex_logic;
13
14 architecture c of hex_logic is
15 begin
16     with input3 select
17     output1 <= "0000"&(input1 and input2) when "1110", --if pb0 is pressed, do logical AND
18              "0000"&(input1 or input2) when "1101", --if pb1 is pressed, do logical or
19              "0000"&(input1 xor input2) when "1011", --if pb2 is pressed, do logical xor
20              "11111111" when others; --just to give a default value
21
22 end c;
```

The status bar at the bottom shows "0%" and "00:00:00".

	Name	Value at 300.0 ns	0 ps	80.0 ns	160.0 ns	240.0 ns	320.0 ns	400.0 ns	
sw3-0	B 0110	0000	0001	0010	0011	0100	0101	0110	0111
sw7-4	B 0101	1000	1001	1010	1111	1101	0010	0101	1110
pb	B 1110	0111	1011	1101	1110	1110	1110	1110	1110
pb[3]	B 1	do addition							
pb[2]	B 1	do logical XOR							
pb[1]	B 1	do logical OR							
pb[0]	B 0	do logical AND							
leds[7]	B 0								
leds[6]	B 0								
leds[5]	B 0								
leds4-0	B 00100	01000	01010	01000	01100	01101	00111	00100	00110

The diagram illustrates the execution of a program over time. The top section shows the state of variables (sw3-0, sw7-4, pb, and leds) at various time points (0 ps, 80.0 ns, 160.0 ns, 240.0 ns, 320.0 ns, 400.0 ns). The bottom section shows the execution of instructions: do addition, do logical XOR, do logical OR, do logical AND, and do nothing. The diagram is divided into two sections by a vertical line at 300.0 ns. The first section shows the initial state and the first instruction. The second section shows the state after the first instruction and the subsequent instructions.

Compilation Report

Flow Summary	
Flow Status	Successful - Thu Jun 13 09:52:16 2019
Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Standard Edition
Revision Name	LogicalStep_Lab2_top
Top-level Entity Name	LogicalStep_Lab2_top
Family	MAX 10
Device	10M08SAE144C8G
Timing Models	Final
Total logic elements	72 / 8,064 (< 1 %)
Total combinational functions	72 / 8,064 (< 1 %)
Dedicated logic registers	11 / 8,064 (< 1 %)
Total registers	11
Total pins	30 / 101 (30 %)
Total virtual pins	0
Total memory bits	0 / 387,072 (0 %)
Embedded Multiplier 9-bit elements	0 / 48 (0 %)
Total PLLs	0 / 1 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 1 (0 %)