4.3 When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance trade-off. In the following three problems, assume that we are starting with a datapath from Figure 4.2, where I-Mem, Add, Mux, ALU, Regs, D-Mem, and Control blocks have latencies of 400 ps, 100 ps, 30 ps, 120 ps, 200 ps, 350 ps, and 100 ps, respectively, and costs of 1000, 30, 10, 100, 200, 2000, and 500, respectively. Consider the addition of a multiplier to the ALU. This addition will add 300 ps to the latency of the ALU and will add a cost of 600 to the ALU. The result will be 5% fewer instructions executed since we will no longer need to emulate the MUL instruction.

4.3.1 What is the clock cycle time with and without this improvement?

The critical path is:

PC > I-mem > Regs > Mux > ALU > D-mem > Mux

The total latency of this path without improvement is:

400+200+30+120+350+30 = 1130ps

The clock cycle time after the improvement is:

1330+300 = 1430ps

4.3.2 What is the speedup achieved by adding this improvement?

From the last question, we can know that the new processor is worse. There is no speedup.

1130 < 1430 × 0.95

4.3.3 Compare the cost/performance ratio with and without this improvement.

The cost of the processor is the sum of the costs of all units.

The old cost is:

1000 + 2 × 30 + 3 × 10 +100 + 200 + 2000 + 500 = 3890

The new cost adds the increased cost of ALU:

3890 + 600 = 4490

The cost ratio is

new cost /old cost = 4490 /3890 =1.15

1130/1430 × 0.95 = 0.83

Cost/performance = 1.15/0.83 = 1.39

4.4 Problems in this exercise assume that logic blocks needed to implement a processor's datapath have the following latencies:

I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-Left-2
200ps	70ps	20ps	90ps	90ps	250ps	15ps	10ps

4.4.1 If the only thing we need to do in a processor is fetch consecutive instructions (Figure 4.6), what would the cycle time be?

The clock cycle time is the latency of the critical path.

PC > ADD > PC – latency of this path is 70 ps

PC > I-mem – latency of this path is 200 ps

The clock cycle time is 200ps.

4.4.2 Consider a datapath similar to the one in Figure 4.11, but for a processor that only has one type of instruction: unconditional PC-relative branch. What would the cycle time be for this datapath?

The critical path is:

PC > I-mem > Sign-extend > Shilf-left-2 > Add > Mux > PC

The latency of this path is the sum of the latencies of its elements:

200 + 15 + 10 + 70 + 20 = 315 ps

4.5 For the problems in this exercise, assume that there are no pipeline stalls and that the breakdown of executed instructions is as follows:

add	addi	not	beq	lw	sw
20%	20%	0%	25%	25%	10%

4.5.1 In what fraction of all cycles is the data memory used?

The data memory used in lw and sw, so the fraction value is 25+15 = 35%

4.5.2 In what fraction of all cycles is the input of the sign-extend circuit needed? What is this circuit doing in cycles in which its input is not needed?

20+25+25+10 = 80%

The sign-extend circuit is computing a result in every cycle, it gives the result to AL and MUX. However the output is ignored in add and not instructions. The input of the sign-extend circuit is needed for addi, beq, lw and sw .

4.8 In this exercise, we examine how pipelining affects the clock cycle time of the processor. Problems in this exercise assume that individual stages of the datapath have the following latencies:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

Also, assume that instructions executed by the processor are broken down as follows:

Ale	beq	lw	sw
45%	20%	20%	15%

4.8.1 What is the clock cycle time in a pipelined and non-pipelined processor?

Clock cycle time in pipelined processor

Max latency of {IF, ID, EX, MEM, WB} = 350 ps

Clock cycle time in non-pipelined processor

250+450+150+300+200=1250ps

4.8.2 What is the total latency of an LW instruction in a pipelined and non-pipelined processor?

Pipeline processor:

There is one cycle per instructions in pipeline.
The total latency of the lw instructions in pipeline processor is:
Number of lw instructions $\times$ cycle time = 5 $\times$ 350 = 1750 ps

Non-pipeline processor:
clock cycle time = 1250 ps
The total latency of lw instructions in non-pipelined processor is:
Number of lw instructions $\times$ clock cycle time in non-pipeline = 1 $\times$ 1250 ps
= 1250 ps