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Chapter-2 2.22 Exercises: 2.23, 2.29 (Last line of 2.29 "bne $t2, $s0, LOOP" should be "bne $t2, $0, LOOP")

2.23 Assume $t0 holds the value 0x00101000. What is the value of $t2 after the following instructions?

        slt $t2, $0, $t0 $t2 = 1
        bne $t2, $0, ELSE $t2 > 0 , so the ELSE is executed
        j DONE
ELSE: addi $t2, $t2, 2 $t2 = 1+2 = 3
DONE:

2.29 Translate the following loop into C. Assume that the C-level integer i is held in register $t1, $s2 holds the C-level integer called result, and $s0 holds the base address of the integer MemArray.

        addi $t1, $0, $0
LOOP: lw $s1, 0($s0)
        add $s2, $s2, $s1
        addi $s0, $s0, 4
        addi $t1, $t1, 1
        slti $t2, $t1, 100
        bne $t2, $0, LOOP

for (i =0; i<100; i++){
   result = result +Array[i];
}

Chapter-4 4.17 Exercises: 4.1

4.1 Consider the following instruction: Instruction: AND Rd,Rs,Rt Interpretation: Reg[Rd] = Reg[Rs] AND Reg[Rt]

4.1.1 What are the values of control signals generated by the control in Figure 4.2 for the above instruction?

RegWrite	MemRead	ALUMux	MemWrite	ALUop	RegMux	Branch
0	0	1	1	ADD	X	0

ALUMux is the control signal that controls the Mux at the ALU input, 0 (Reg) selects the output of the register file, and 1 (Imm) selects the immediate from the instruction word as the second input to the ALU. RegMux is the control signal that controls the Mux at the Data input to the register file, 0 (ALU) selects the output of the ALU, and 1 (Mem) selects the output of memory. A value of X is a dont care (does not matter if signal is 0 or 1)
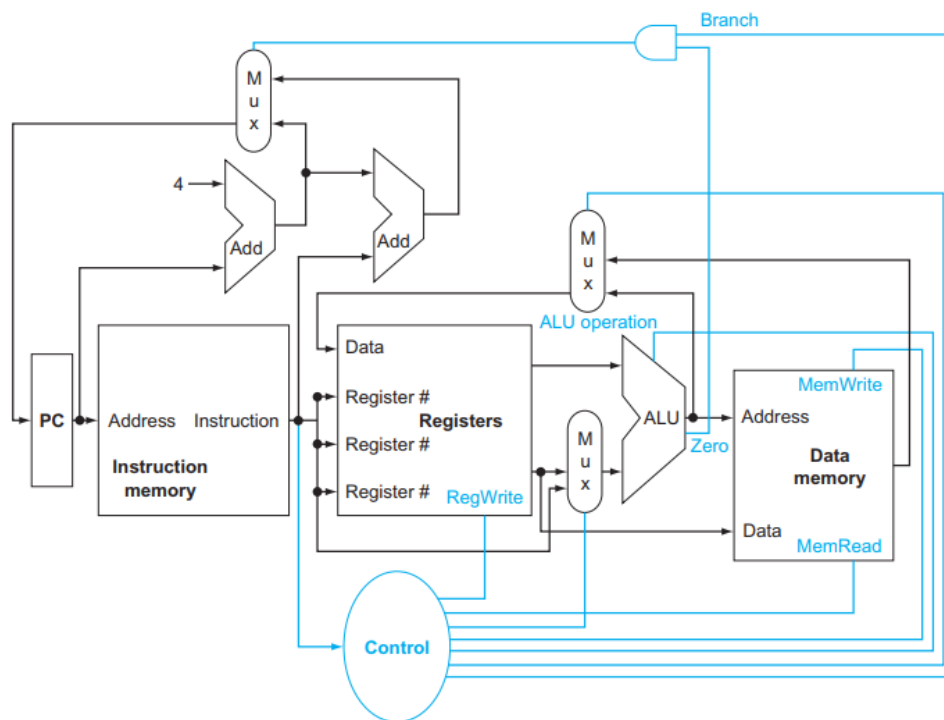
4.1.2   Which resources (blocks) perform a useful function for this instruction?

All except branch Add unit and write port of the Registers

4.1.3   Which resources (blocks) produce outputs, but their outputs are not used for this instruction? Which resources produce no outputs for this instruction?

Outputs that are not used: Branch Add, write port of Registers

No outputs: None (all units produce outputs)