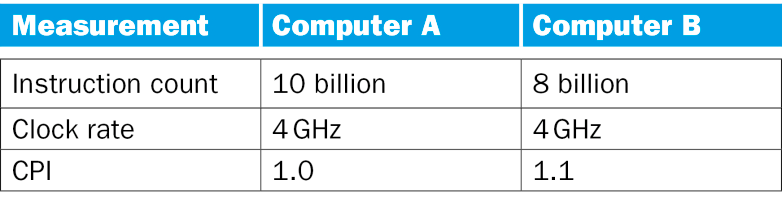
• Access time comparison  
a) SSD < DRAM < 7200RPM HD  
b) DRAM < SSD < 7200RPM HD  
c) DRAM < 7200RPM HD < SSD

• Volatile vs. Non Volatile Type  
a) SSD and DRAM are volatile, 7200RPM HD is non-volatile  
b) DRAM and 7200RPM HD are volatile, SSD is non-volatile  
c) DRAM is volatile, SSD and 7200RPM HD are non-volatile

A given application in Java runs 15 seconds on a desktop processor. A new Java compiler is released that requires only 0.6 as many instructions as the old compiler. Unfortunately, it increases the CPI by 1.1. How fast can we expect the application to run using this new compiler?  
a) (15 x 0.6) / 1.1 = 8.2sec  
b) 15 x 0.6 x 1.1 = 9.9 sec  
c) (15 x 1.1) / 0.6 = 27.5 sec

Consider the following performance measurements for a program:

  
a) Which computer has the higher MIPS rating? A  
b) Which computer is faster? B

Assume variables f, g, h, i are assigned to registers $s0-$s3 respectively. For the following MIPS assembly instructions, what is the corresponding C code?  
add $s0, $s2, $s1

sub $s1, $s3, $s0

g = i - (g + h)

What is the decimal value of this 32-bit two’s complement number?  
1111 1111 1111 1111 1111 1111 1111 1000  
a) -4ten  
b) -8ten  
c) -16ten  
d) -32ten

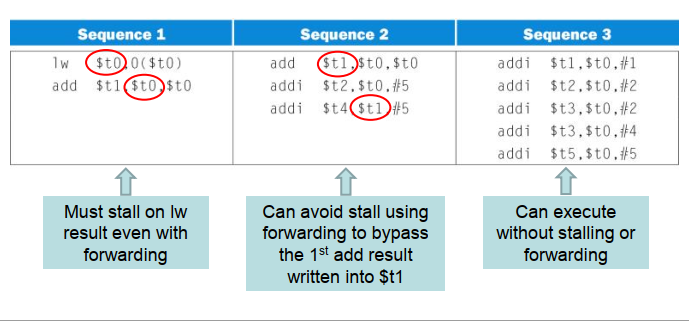
Assume variables f, g, h, i are assigned to registers $s0- $s3 respectively. Assume the base address of array A is in register $s4. Assume arrays A is 4-byte word. For the following MIPS assembly instructions, what is the corresponding C code?  
sll $t0, $s2, 2  
add $t1, $t0, $s4  
lw $t0, 0($t1)  
add $s1, $t0, $s0

g = A[h] + f

Which of the following is correct for a load instruction?  
a) MemtoReg should be set to cause the data from memory to be sent to the register file.  
b) MemtoReg should be set to cause the correct register destination to be sent to the register  
file.

c) We don not care about the setting of MemtoReg for loads.

For each code sequence below, which one is must stall, can avoid stalls using only forwarding, or can execute without stalling or forwarding.



1. Pipeline can help performance with split stages with pipeline stages visible to programmer. No
2. Pipeline speed up is achieved through increase a circle. YES
3. While pipeline help improved the performance, it also induces the increase latency of pipeline hazard and decreases the stages. YES