

Digital Logic CS207

2024 Fall Assignment 3

- Write neatly and submit a **PDF** file to Blackboard before deadline.
- Write down **ALL procedures**. Only presenting the final answer will lead to a zero, even the answer is correct.
- **When drawing the state diagram, arrange your state circles counter clockwise (画状态图时请按逆时针方向画状态圈)**

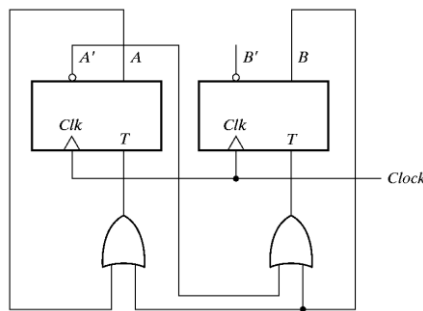
1. A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations:

$$\mathbf{J}_A = \mathbf{x}, \quad \mathbf{K}_A = \mathbf{B}$$

$$J_B = X, \quad K_B = A,$$

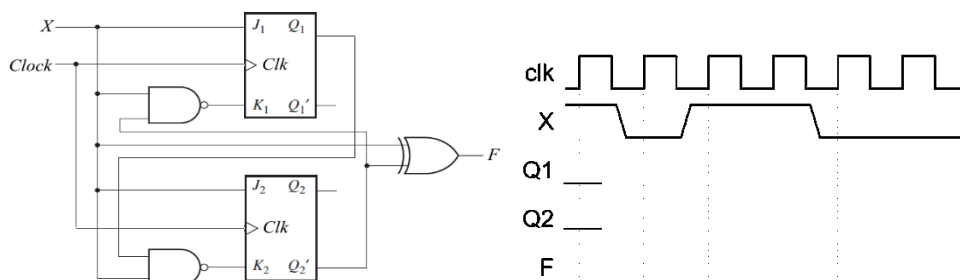
- Derive the state equations $A(t+1)$ and $B(t+1)$ by substituting the input equations for the J and K variables.
- Draw the state table and state diagram of the circuit.

2. Derive the input/state/output function, state table/diagram if applicable for the sequential circuit shown in the block diagram blow. Explain the function that the circuit performs.



3. For the block diagram below

- Derive the input/state/output function, state table/diagram of the sequential circuit if applicable.
- Is it a Mealy machine or a Moore machine? Why?
- Construct a timing diagram for the circuit for an input sequence $X = 101100$. (Assume that initially $Q1 = Q2 = 0$, X always change midway during the clock low level, Complete the following waveform for $Q1$, $Q2$ and F .)



4. For the following state table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
<i>a</i>	<i>f</i>	<i>b</i>	0	0
<i>b</i>	<i>d</i>	<i>c</i>	0	0
<i>c</i>	<i>f</i>	<i>e</i>	0	0
<i>d</i>	<i>g</i>	<i>a</i>	1	0
<i>e</i>	<i>d</i>	<i>c</i>	0	0
<i>f</i>	<i>f</i>	<i>b</i>	1	1
<i>g</i>	<i>g</i>	<i>h</i>	0	1
<i>h</i>	<i>g</i>	<i>a</i>	1	0

- Draw the corresponding state diagram.
 - Minimize the state table, show your procedures, and then draw the reduced table and its corresponding state diagram.
 - Determine the output sequence for input sequence 01010010111 (from left to right) with the original state table and the reduced state table, starting from *a*.
5. The following latch is constructed from OR, AND and NOT gate, P is always equal to Q'.
- Construct a function table for the latch and describe the behavior. Show the procedure.
 - Draw a valid timing graph to represent the behavior of the latch by covering all the valid combination of R and H. Pay attention to the forbidden state.

