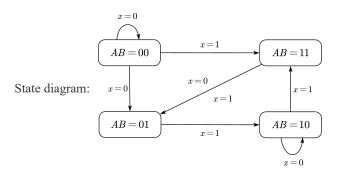
Digital Logic Theory Assignment 3

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1. a) $A(t+1) = J_A A(t)' + K_A' A(t) = xA' + B'A, B(t+1) = J_B B(t)' + K_B' B(t) = xB' + AB.$

b) State table:

x	A	J_A	K_A	A(t+1)	B	J_B	K_{B}	B(t+1)
0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0
0	1	0	0	1	0	0	1	0
0	1	0	1	0	1	0	1	1
1	0	1	0	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	1	1	0	1	0	1	1	1
1	1	1	1	0	1	1	1	1

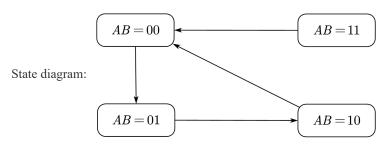


2. In the T Flip-Flop for $A, T_A = A + B$. In the T Flip-Flop for $B, T_B = A' + B$.

$$\therefore A(t+1) = T_A'A + TA' = A'B, B(t+1) = T_B'B + T_BB' = A'B'.$$

State table:

Clk	A	B	A(t+1)	B(t+1)
0	x	x	last A	last B
1	x	x	last A	last B
$0 \rightarrow 1$	0	0	0	1
0→1	0	1	1	0
$0 \rightarrow 1$	1	0	0	0
0 -> 1	1	1	0	0



This circuit performs as a binary counter with $00 \rightarrow 01 \rightarrow 10 \rightarrow 00$.

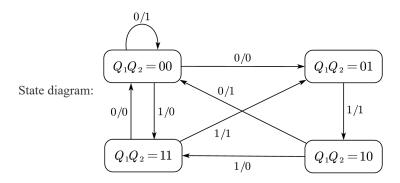
3. a)
$$J_1=J_2=X, K_1=(XQ_2')'=X'+Q_2, K_2=(XQ_1)'=X'+Q_1', F=X\oplus Q_2'=XQ_2+X'Q_2'.$$

$$\therefore Q_1(t+1) = J_1Q_1' + K_1'Q_1 = XQ_1' + XQ_1Q_2' = X(Q_1' + Q_2').$$

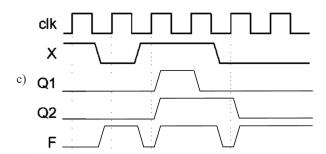
$$Q_2(t+1) = J_2Q_2' + K_2'Q_2 = XQ_2' + XQ_1Q_2 = X(Q_1 + Q_2').$$

State table:

Clk	X	Q_1	Q_2	$Q_1(t+1)$	$Q_2(t+1)$	F
0 -> 1	0	0	0	0	0	1
0→1	0	0	1	0	0	0
0 -> 1	0	1	0	0	0	1
0 -> 1	0	1	1	0	0	0
0→1	1	0	0	1	1	0
0 -> 1	1	0	1	1	0	1
0 -> 1	1	1	0	1	1	0
0→1	1	1	1	0	1	1



b) It is a mealy machine, because the output F depends on the current state Q_2^\prime and the input X.



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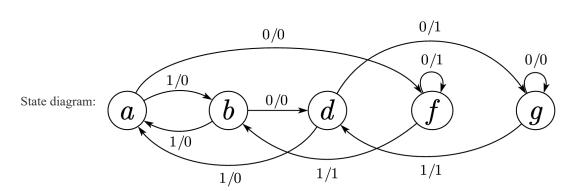
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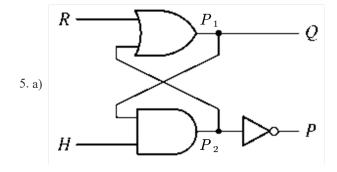
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b) Reduced table:

Present State	Next State		Output	Output		
	x = 0	x = 1	x = 0	x = 1		
a	f	b	0	0		
b	d	a	0	0		
d	g	a	1	0		
f	f	b	1	1		
g	g	d	0	1		



c)												
Origin	nal Table											
t		0	1	2	3	4	5	6	7	8	9	10
S	а	f	b	d	а	f	f	b	d	а	b	
Χ		0	1	0	1	0	0	1	0	1	1	1
У		0	1	0	0	0	1	1	0	0	0	0
Redu	ced Table											
t		0	1	2	3	4	5	6	7	8	9	10
S	а	f	b	d	а	f	f	b	d	а	b	
X		0	1	0	1	0	0	1	0	1	1	1
V		0	1	0	0	0	1	1	0	0	0	0



... When R = 0, $Q = P_2$; R = 1, $Q = P_1 = 1$. When H = 0, $Q = P_2 = 0$; H = 1, $Q = P_1$.

.: Function Table:

R	H	Q	P	Function
0	0	0	1	Reset State
0	1	last Q	last P	No Change
1	0	1	1	Forbidden
1	1	1	0	Set State

