25 CS202 HW2

Problem 1

Consider two different implementations of the same instruction set architecture. The CPI of the different instruction types is given in the following table.

	Arithmetic	Load/Store	Branch
a.	4	10	3
b.	1	20	2

Assume the following instruction breakdown given for executing a given program:

	Instructions
Arithmetic	$5 * 10^8$
Load/Store	$3 * 10^8$
Branch	$2 * 10^8$

a) What is the global CPI for each implementation?

b) What is the execution time for the processor if the operation frequency is 5 GHz?

c) Suppose that new, more powerful arithmetic instructions are added to the instruction set. On average, through the use of these more powerful arithmetic instructions, we can reduce the number of arithmetic instructions needed to execute a program by 25%, and the cost of increasing the clock cycle time **of all instruction** by only 10%. Is this a good design choice for each implementations? Why?

Problem 2

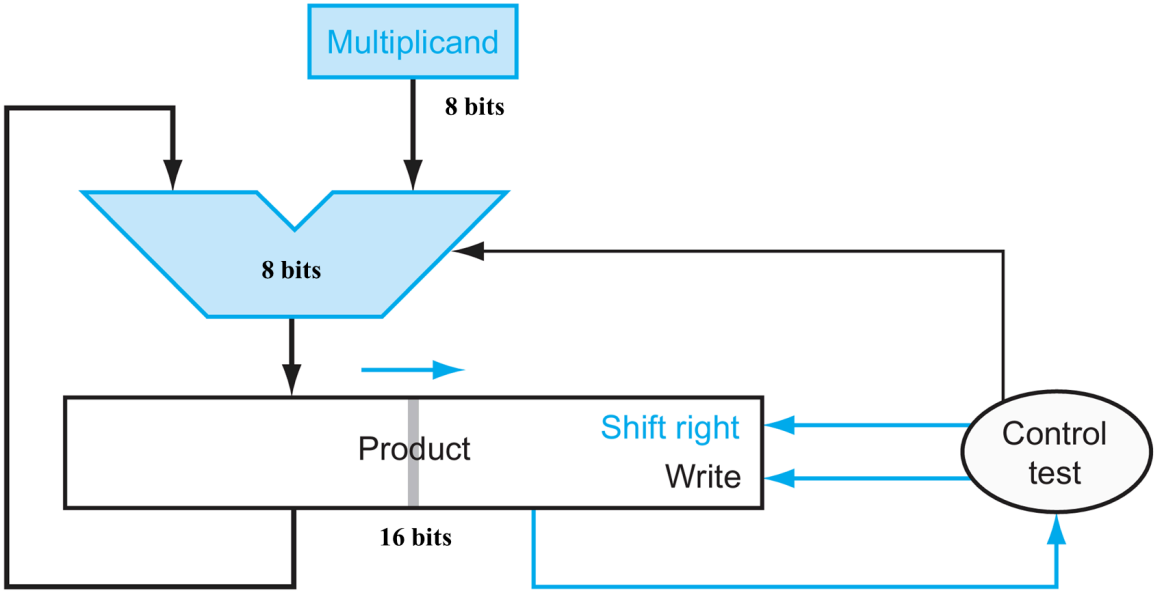
a) Assume -40 and 100 are signed 8-bit **decimal** integers stored in two's complement format. Calculate -40 + 100 using saturating arithmetic. The result should be written in decimal. Show the steps for calculation.

b) Assume -40 and 100 are signed 8-bit **decimal** integers stored in two's complement format. Calculate -40 - 100 using saturating arithmetic. The result should be written in decimal. Show the steps for calculation.

Problem 3

Calculate the product of the **hexadecimal** unsigned 8-bit integers `0x34` and `0x1A` using the hardware described below (Refer to `FIGURE 3.5` on page 181 of the textbook). Show the binary contents of each register on each step. Use a table to document the process. `0x34` is used as the **multiplicand**.

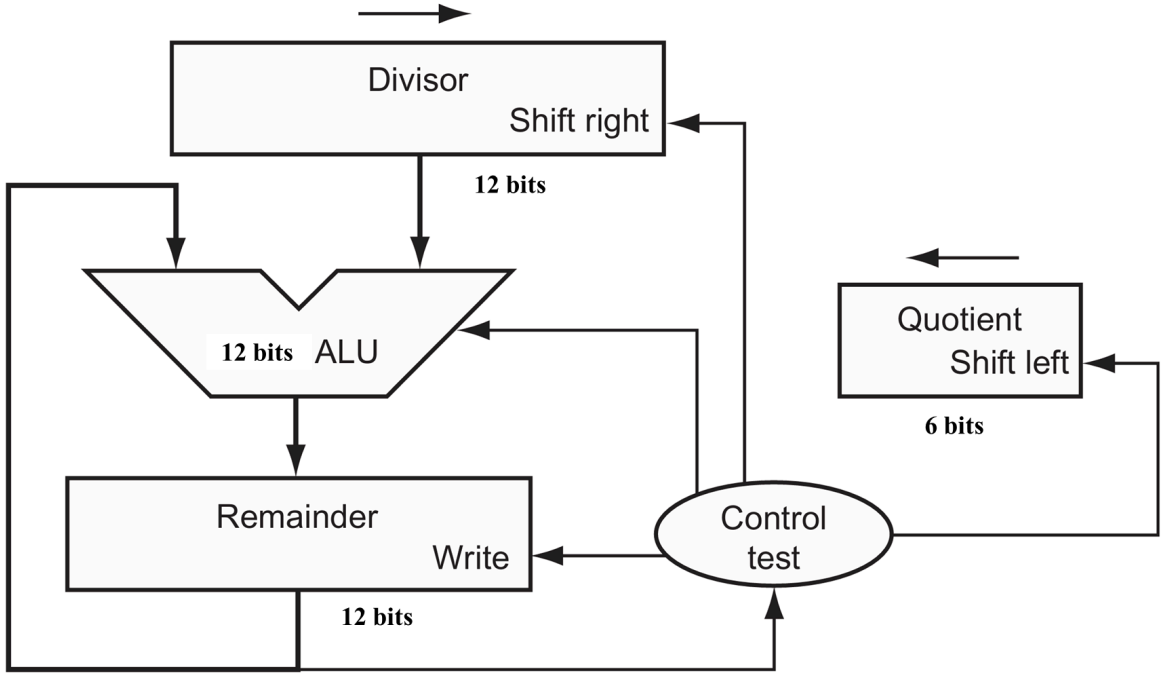
Your answer format must strictly adhere to the table format provided on page 181 of the textbook (`FIGURE 3.6`), and you are not allowed to omit any iterative steps.



Problem 4

Calculate unsigned 6-bit **decimal** integer 54 divided by 17 using the hardware described below (Refer to `FIGURE 3.8` on page 184 of the textbook). Show the binary contents of each register on each step. Use a table to document the process.

Your answer format must strictly adhere to the table format provided on page 186 of the textbook (`FIGURE 3.10`), and you are not allowed to omit any iterative steps.



Problem 5

a) What decimal number does the bit pattern `0x3E800000` represent if it is an IEEE754 single-precision floating-point number? Show the steps for calculation.

b) Write down the binary representation of the decimal number `12.5` assuming the IEEE754 single-precision format. Show the steps for calculation.

c) Perform the addition of the following two IEEE754 single-precision floating-point numbers:

- **Number A**: `0x3F800000`
- **Number B**: `0xBF400000`

Show all steps including:

1. Binary representation of both numbers.
2. Alignment of exponents.
3. Addition of significands.
4. Normalization of the result.
5. Final 32-bit packed result in hexadecimal.

The answer format for steps 1-5 can refer to the example format provided on page 199 of the textbook.