DIGITAL LOGIC

Course Introduction

2024 Fall

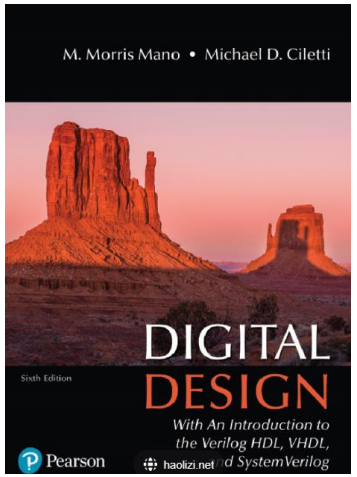
baiyh@sustech.edu.cn

Course Information

- Course website:
  - Blackboard:
- Instructor:
  - Dr. Yuhui BAI (baiyh@sustech.edu.cn)
  - Office: 411 College of Engineering South
  - Office hour: Mon. 14:00-16:00 (by appointment)
- Lecture
  - 10:20-12:10 Monday, Lecture Hall #1
- Lab
  - 14:00 -15:50 Tue.(Yuhui BAI)
  - 16:20 -18:10 Tue. (Wei WANG)
  - 14:00 -15:50 Wed. (Wei WANG)
  - 10:20-12:10 Fri., (Wei WANG)
  - 14:00 -15:50 Fri., (Wei WANG)

Textbook

- Textbook:
  - Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog by *M. Morris Mano and Michael D. Ciletti*, 6th edition.



- Reference book:
  - Digital Principles and Logic Design by A. Saha and N. Manna.
  - Digital Logic Design by B. Holdsworth and C. Woods

Course Outline

1. Digital Systems and Binary Numbers
   - Binary Systems, Conversions, Signed Binary, Codes
2. Boolean Algebra and Logic Gates
   - Theorems, Boolean Functions, operators, gates
3. Gate-level Minimization
   - Truth table, K Map, two-level implementations, NAND, NOR
4. Combinational Logic
   - Combinational circuits, arithmetic logic, mux, de-mux, encoder, decoder
5. Synchronous Sequential Logic
   - Sequential circuit, Latches, Flip flops, State Machines
6. Registers and Counters
7. Memory and Programmable Logic
   - RAM, ROM, FPGA
8. Verilog (Lab)

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Tentative Schedule (available in BB)

WEEK	LEC	LECTURE DATE	LECTURE TOPIC	LAB TOPIC
1	Lec #1	Sep. 9, 2024 (Mon.)	Course Introduction, Binary Numbers	Environment Setup
2	Lec #2	Sep. 14, 2024 (Sun.)	Boolean Algebra and Logic Gates	Structural-Based Design
3	Lec #3	Sep. 23, 2024 (Mon.)	Gate-Level Minimization (*HW1 release*)	Dataflow Design
4	Lec #4	Sep. 30, 2024 (Mon.)	Two-Level Implementation	Testbench
5	/	Oct. 7, 2024 (Mon.)	Holiday	/
6	Lec #5	Oct. 14, 2024 (Mon.)	*HW1 analysis* & Combinational Logic	Behavioral-Based Design
7	Lec #6	Oct. 21, 2024 (Mon.)	Standard Components (*HW2 release*)	Encoder, Decoder
8	Lec #7	Oct. 28, 2024 (Mon.)	*HW2 analysis* & Latches and Flip-flops	Multiplexer, De-multiplexer
9	Mid-term	Nov. 4, 2024 (Mon.)	Mid-term Exam (Lecture 1-6)	Latch, FlipFlop
10	Lec #8	Nov. 11, 2024 (Mon.)	Sequential Logic 1	Finite state machine
11	Lec #8	Nov. 18, 2024 (Mon.)	Sequential Logic 2 (*HW3 release*)	Frequency divider
12	Lec #9	Nov. 25, 2024 (Mon.)	Registers Counters 1	Register
13	Lec #9	Dec. 2, 2024 (Mon.)	*HW3 analysis* & Registers Counters 2	Counter
14	Lec #10	Dec. 9, 2024 (Mon.)	Arithmetic Circuit (*HW4 release*)	Verilog Summary
15	Lec #11	Dec. 16, 2024 (Mon.)	Memory and Programmable Logic	Project Inspection
16	Review	Dec. 23, 2024 (Mon.)	*HW4 analysis* & Revision	Project Inspection

Grading criteria (might be updated)

- Lecture (15%)
  - 5% Attendance
  - 10% Homework
- Exam (55%)
  - 15%~20% Mid-term examination (week 9)
  - 40%~35% Final examination
- Lab (30%)
  - 5% Attendance and Lab practices
  - 10% Lab assignments on OJ
  - 15% Lab Project
    - In groups of 2~3. Please team up as soon as possible.
    - Please try to choose classmates from the same lab class.
    - In special circumstances where cross-class teams are needed, it is important to ensure that all team members can attend the Project Inspection at the end of the semester.