Specifications of the Camera Link Interface Standard for Digital Cameras and Frame Grabbers

Camera Link Specification – v2.1

Includes:

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Camera Link Licensing and Logo Usage

Camera Link is a widely adopted standard and is used on hundreds of products on the market today.

The standard is a hardware specification that standardizes the connection between cameras and frame grabbers. It defines a complete interface which includes provisions for data transfer, camera timing, serial communications, and real time signaling to the camera.

The AIA owns the trademarks and trade names for Camera Link, Power Over Camera Link, and Power Over Camera Link Lite. All commercial products developed using the Camera Link standard must license the standard and qualify for the right to use the name and logo. To qualify, each product must have the proper paperwork submitted to the AIA and must self-certify to be compliant with the Camera Link standard. More information on licensing Camera Link can be found at www.visiononline.org/standards.

The Camera Link name and logos may be used only in conjunction with licensed products which have certified to be compliant with the Camera Link standard.

About this Document

The following specifications provide a framework for Camera Link and Camera Link Lite communication. Version 2.1 resolves problems with the jack screws, updates and adds definitions to the bit assignment section (also rewritten for clarity), adds support for FPGA emulation of the Channel Link chip and adds a new function to the serial API (and deprecates an old one). See the LOC for a complete list of changes. The specifications are deliberately defined to be open, allowing camera and frame grabber manufacturers to differentiate their products. Additional recommendations may be added at a later date, which will not affect the accuracy of the information in this document. Backward compatibility is assured for all products.

Acknowledgments

Participating Companies

The following companies participated in the development, definition and review of this version and previous versions of the Camera Link standard:

3M Company
Active Silicon Ltd.
ADIMEC Advanced Image Systems BV
Alacron, Inc.
AVAL DATA CORPORATION
Basler AG
BitFlow, Inc.
Carrio Cabling Corporation
CIS Corporation
Cognex Corporation
Components Express, Inc.
e2v Semiconductors
ELTEC Elktronik AG
Engineering Design Team, Inc.
EPIX, Inc.
Euresys, Inc.
Fairfield Imaging, Inc.
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W. L. Gore & Associates
Hitachi Kokusai Electric America, Ltd.
Imperx Incorporated
Intercon 1
JAI
Leutron Vision, Inc.
Matrox Electronic Systems Ltd.
Microtechnica Co., Ltd
Mikrotron GmbH
National Instruments
Northwire, Inc.
OCP Group, Inc.
Photonfocus Ltd.
Pleora Technologies Inc.
PPT VISION, Inc.
PULNiX America, Inc.
Redlake MASD, LLC
Sentec America
SICK|IVP AB
Siemens, Inc.
Silicon Software
Sony Visual Imaging Products
STAC Corporation
Stemmer Imaging GmbH
Teledyne DALSA
Thinklogical
TKM Technologies, Inc.
Toshiba Teli Corporation
TVI Vision

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1.0 Camera Link

1.1 Introduction

Camera Link is a communication interface for vision applications. The interface extends the base technology of Channel Link by Texas Instruments (formerly National Semiconductor) to provide a specification more useful for vision applications.

For years, the scientific and industrial digital video market lacked a standard method of communication and data transfer. Both frame grabber and camera manufacturers developed products with different connectors, making cable production difficult for manufacturers and very confusing for consumers. Camera Link 1.2 and its previous revisions provided an extremely useful connectivity standard between digital cameras and frame grabbers which has provided significant value to the machine vision community. Increasingly diverse cameras and advanced signal and data transmissions have made a connectivity standard like Camera Link a necessity. The Camera Link interface reduces support time, as well as the cost of that support. The standard cable is able to handle the increased signal speeds, and the cable assembly allows customers to reduce their costs through volume pricing. Camera Link 2.1 continues this standard of excellence by incorporating previous annexes into one comprehensive document.

1.2 Device Interoperability

The goal of Camera Link is to guarantee interoperability between all Camera Link devices. This is achieved from a combination of this specification and a mandatory Plugfest regime for all active devices. In this case, “active” means any device that uses a Channel Link chip or an FPGA emulation of the Channel Link chip. Compliance to this standard requires completion of the AIA License and the completion of the applicable AIA complacency process, which includes an interoperability test at an AIA hosted Plugfest.

Note: Camera Link specifications 1.0 through 2.0 only required manufacturers pass a self certification check list in order to be considered Camera Link complaint. Version 2.1 adds the requirement that all active devices must pass a live interoperability test at a Plugfest.

1.3 Conventions

“Shall” means a mandatory requirement.

“Can” means an optional feature.

NOTE: Paragraphs labeled “NOTE:” do not form part of the specification, but are intended to help understand the requirements of the specification.

1.4 LVDS Technical Description

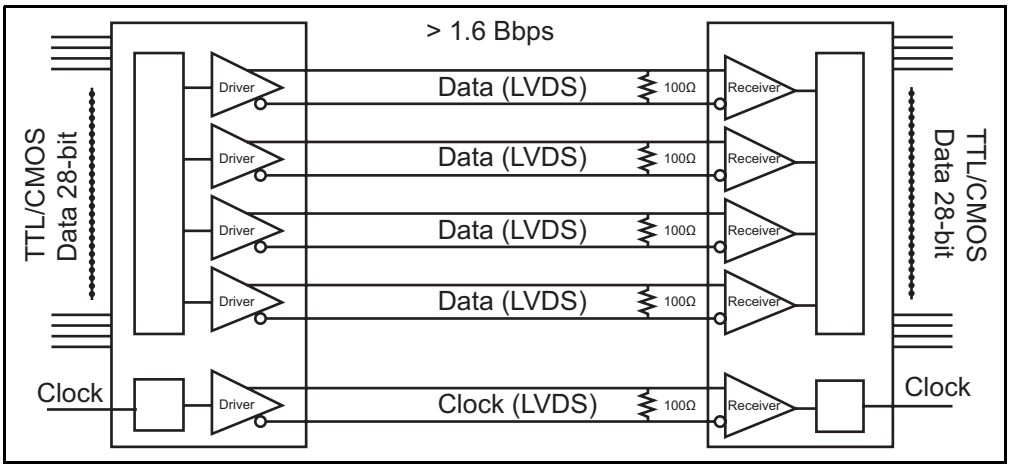
Low-voltage differential signaling (LVDS) is a high-speed, low-power, general-purpose interface standard. The standard, known as ANSI/TIA/EIA-644, was approved in March 1996. LVDS uses differential signaling, with a nominal signal swing of 350 mV differential. The low signal swing decreases rise and fall times to achieve a theoretical maximum transmission rate of 1.923 Gbps into a loss-less medium. The low signal swing also means that the standard is not dependent on a

particular supply voltage. LVDS uses current-mode drivers, which limit power consumption. The differential signals are immune to ±1 V common volt noise.

1.5 Channel Link

National Semiconductor developed the Channel Link technology as a solution for flat panel displays, based on LVDS for the physical layer. The technology was then extended into a method for general purpose data transmission. Channel Link consists of a driver and receiver pair. The driver accepts 28 single-ended data signals and a single-ended clock. The data is serialized 7:1, and the four data streams and a dedicated clock are driven over five LVDS pairs. The receiver accepts the four LVDS data streams and LVDS clock, and then drives the 28 bits and a clock to the board. Figure 1-1 illustrates Channel Link operation.

Figure 1-1: Channel Link Operation



1.6 FPGA Emulation of Channel Link

Camera Link has traditionally required use of the Channel Link chip. However, it has become possible to emulate the functionality of this chip inside of an FPGA. As of Camera Link 2.1, devices that use FPGA emulation are considered Camera Link compliant. Please see Section 6.3 for more information.

Since an FPGA can replicate the functionality of any number of Channel Link chips, manufacturers of devices that use FPGA emulation can ignore text and tables in this specification that refer to “Number of Channel Link Chips”.

1.7 Camera Link’s Six Configurations

The Camera Link standard includes six configurations. Each configuration supports a different number of data bits. The advantage of multiple configurations is that manufacturers can select the configuration that best matches their device. The flexibility provides low cost and space requirements for small cameras, while supporting very high data rates for cameras that have high speed sensors.

The six configurations are:

- lite - Supports up to 10 bits, one connector

- base - Supports up to 24 bits, one connector
- medium - Supports up to 48 bits, two connectors
- full - Supports up to 64 bits, two connectors
- 72 bit - Supports up to 72 bits, two connectors
- 80 bit - Supports up to 80 bits, two connectors, some signals re-purposed for data

1.8 Technology Benefits

1.8.1 Smaller Connectors and Cables

Channel Link's transmission method requires fewer conductors to transfer data. Five pairs of wires can transmit up to 28 bits of data. These wires reduce the size of the connector, allowing smaller cameras to be manufactured.

1.8.2 High Data Transmission Rates

The data transmission rates of the Channel Link family of chipsets (up to 2.38 Gbits/s) support the current trend of increasing transfer speeds.

2.0 Camera Signal Requirements

2.1 Introduction

This section provides definitions for the signals used in the Camera Link and Camera Link Lite interfaces. The standard Camera Link cable provides camera control signals, serial communication, and video data.

2.2 Video Data

The Channel Link technology is integral to the transmission of video data. Image data and image enables are transmitted on the Channel Link bus.

2.2.1 Camera Link Base/Medium/Full/72 Bit

Four enable signals for Camera Link Base/Medium/Full/72 Bit are defined as:

- FVAL—Frame Valid (FVAL) is defined HIGH for valid lines with no offsets between the edge of FVAL and the start of the first valid line.
- LVAL—Line Valid (LVAL) is defined HIGH for valid pixels with no offsets between the start of LVAL and the first valid pixel.
- DVAL—Data Valid (DVAL) is defined HIGH when data is valid.
- Spare—A spare has been defined for future use.

All defined enables must be provided by the camera on each Channel Link chip. All unused data bits must be tied to a known value by the camera.

For more information on image data bit allocations, see Section 4 - Bit Assignments.

2.2.2 Camera Link Lite

The following signals are defined as:

- FVAL – Frame Valid (FVAL) is defined HIGH for valid lines with no offsets between the edge of FVAL and the start of the first valid line.
- LVAL – Line Valid (LVAL) is defined HIGH for valid pixels with no offsets between the start of LVAL and the first valid pixel.
- DVAL – Data Valid (DVAL) is defined HIGH when data is valid.
- Spare –A spare is not assigned for this configuration.

All three enables must be provided by the camera on each Channel Link chip. All unused data bits must be tied to a known value by the camera.

For more information on image data bit allocations, see Section 4 - Bit Assignments.

2.2.3 Camera Link 80 bit

The 80 bit configuration uses some of the signals normally used to carry enable for data. All spares are also used for data. For 80 bit mode the enables are defined as:

- FVAL—Frame Valid (FVAL) is defined HIGH for valid lines, first channel link chip only.
- LVAL—Line Valid (LVAL) is defined HIGH for valid pixels, all channel link chips.

NOTE: The DVAL and Spare signals are used to carry data bits in this configuration.

LVAL and FVAL must be provided by the camera on base Channel Link chip. LVAL only must be provided on the other two chips. All other signals are used by data.

For more information on image data bit allocations, see Section 4 - Bit Assignments.

2.3 Camera Control Signals

2.3.1 Camera Link Base/Medium/Full/72 Bit/80 Bit

Four LVDS pairs are reserved for general-purpose camera control. They are defined as camera inputs and frame grabber outputs. Camera manufacturers can define these signals to meet their needs for a particular product. The signals are:

- Camera Control 1 (CC1)
- Camera Control 2 (CC2)
- Camera Control 3 (CC3)
- Camera Control 4 (CC4)

2.3.2 Camera Link Lite

One LVDS pair is reserved for general-purpose camera control.

This pair is defined as camera input and frame grabber output.

Camera manufacturers can define this signal to meet their needs for a particular product.

- Camera Control (CC)

2.4 Communication

Camera Link uses asynchronous serial communication as a control path between the camera and the frame grabber.

The serial interface has the following characteristics:

- Eight data bits
- One start bit
- One stop bit
- No parity
- No handshaking

Cameras and frame grabbers should support at least 9600 baud.

Frame grabber manufacturers must supply a software application programming interface (API) for using the asynchronous serial communication port. The software API provides functions used by a common DLL for managing serial communication. See Section 8.0 for the required software API.

Additionally, it is recommended that frame grabber manufacturers supply a user interface. The user interface should consist of a terminal program with minimal capabilities of sending and receiving a character string and sending a file of bytes.

2.4.1 Camera Link Base/Medium/Full/72 Bit/80 Bit

Two LVDS pairs have been allocated for asynchronous serial communication to and from the camera and frame grabber. These signals are

- SerTFG—Serial communications to the frame grabber using an LVDS pair.
- SerTC—Serial communications to the camera using an LVDS pair.

2.4.2 Camera Link Lite

One LVDS pair has been allocated for asynchronous serial communication from the frame grabber to the camera. The communication signal from the camera to the frame grabber is embedded into the Channel Link data path. These signals are:

- SerTFG—Serial communications to the frame grabber which is embedded into the Channel Link data. See section 4.4 for the bit allocation for SerTFG in the Channel Link chip. SerTFG is a standard asynchronous serial signal generated at the same baud rate as used for SerTC. Therefore SerTC is not transitioning at pixel clock speed.
- SerTC—Serial communications to the camera using an LVDS pair.

3.0 Port Assignments

As mentioned previously, the Camera Link interface has six configurations. Since a single Channel Link chip is limited to 28 bits, some cameras may require several chips in order to handle higher data rates and/or greater data widths.

The naming conventions for the various configurations are:

- Lite/Base - Single Channel Link chip, single cable connector.
- Medium - Two Channel Link chips, two cable connectors.
- Full/72 bit/80 bit - Three Channel Link chips, two cable connectors.

3.1 Port Definition - all Configurations

A port is defined as an 8-bit word. The Least Significant Bit (LSB) is bit 0, and the Most Significant Bit (MSB) is bit 7. The Camera Link interface utilizes the 8 ports of A–J. Table 3-1 shows the port assignment for the Lite, Base, Medium, and Full/72 bit/80 bit Configurations.

Table 3-1: Port Assignments According to Configuration

Configuration	Ports Supported	Number of Chips	Number of Connectors
Lite	A, B (up to 10 bits only)	1	1
Base	A, B, C	1	1
Medium	A, B, C, D, E, F	2	2
Full	A, B, C, D, E, F, G, H	3	2
72 bit	A, B, C, D, E, F, G, H, I	3	2
80 bit	A, B, C, D, E, F, G, H, I, J	3	2

3.2 Camera Hardware Routing and Block Diagram

3.2.1 Base, Medium, Full and 72 bit Configurations

Figure 3-1 shows the hardware routing for the Base, Medium, Full and 72 bit configurations. Figure 3-2 shows the block diagram for the Base, Medium, Full and 72 bit configurations.

72 bit configurations are similar to the full configurations except that they add port I.

Figure 3-1: Data Routing for Base, Medium, and Full Configurations

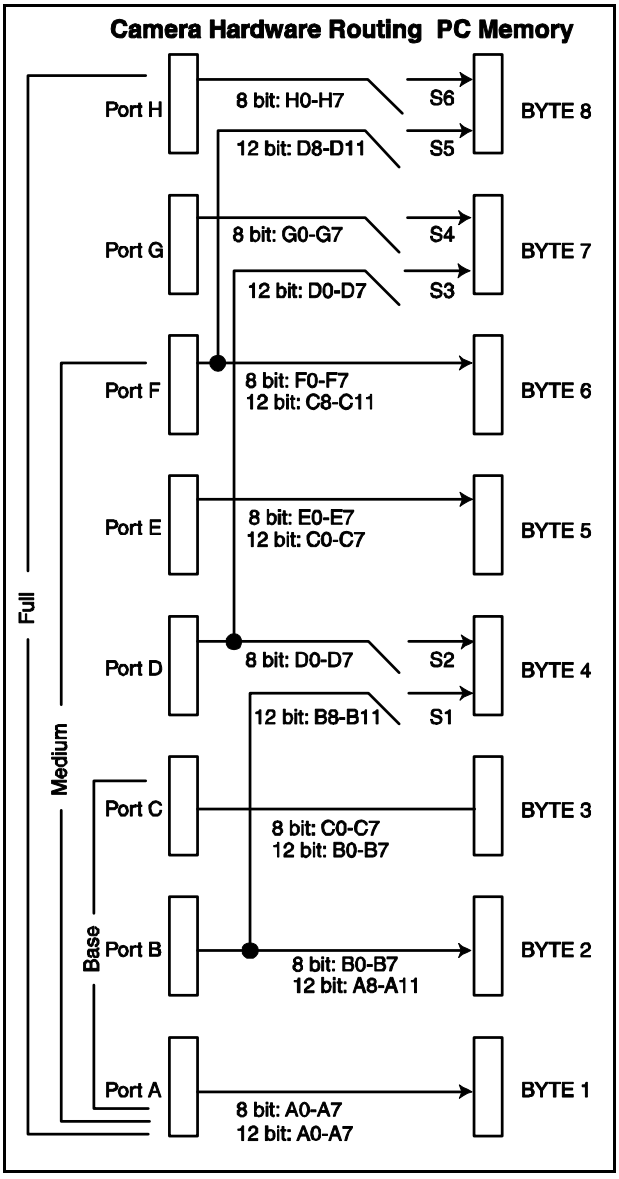
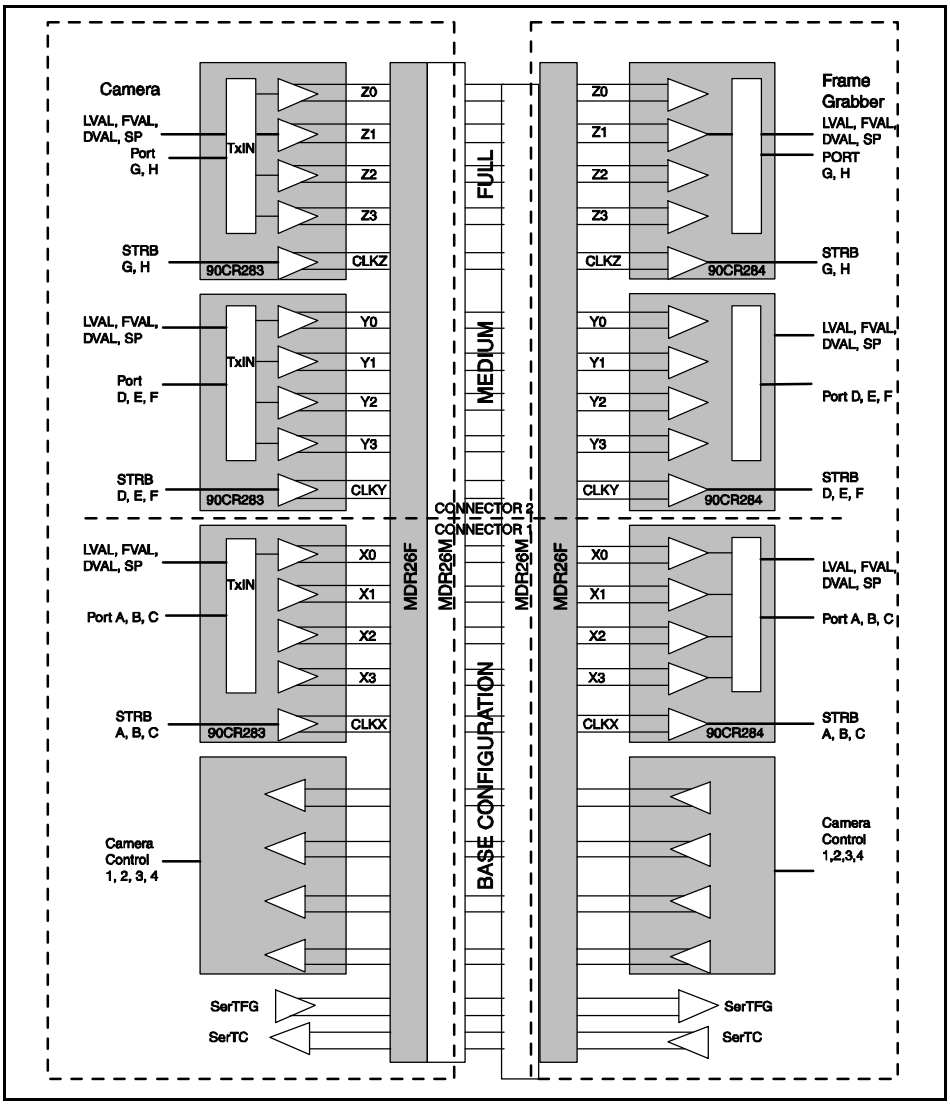


Figure 3-2: Block Diagram of Base, Medium, and Full Configuration



3.2.2 Lite Configurations

Figure 3-3 shows the hardware routing for the Lite configurations. Figure 3-4 shows the block diagram for the Lite configuration.

Figure 3-3: Data Routing for Lite Configurations

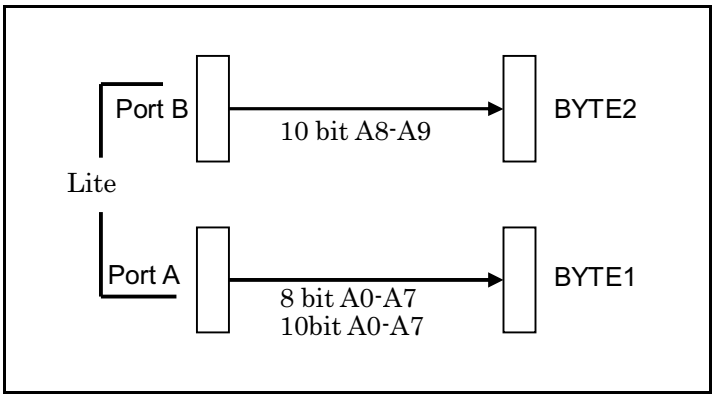
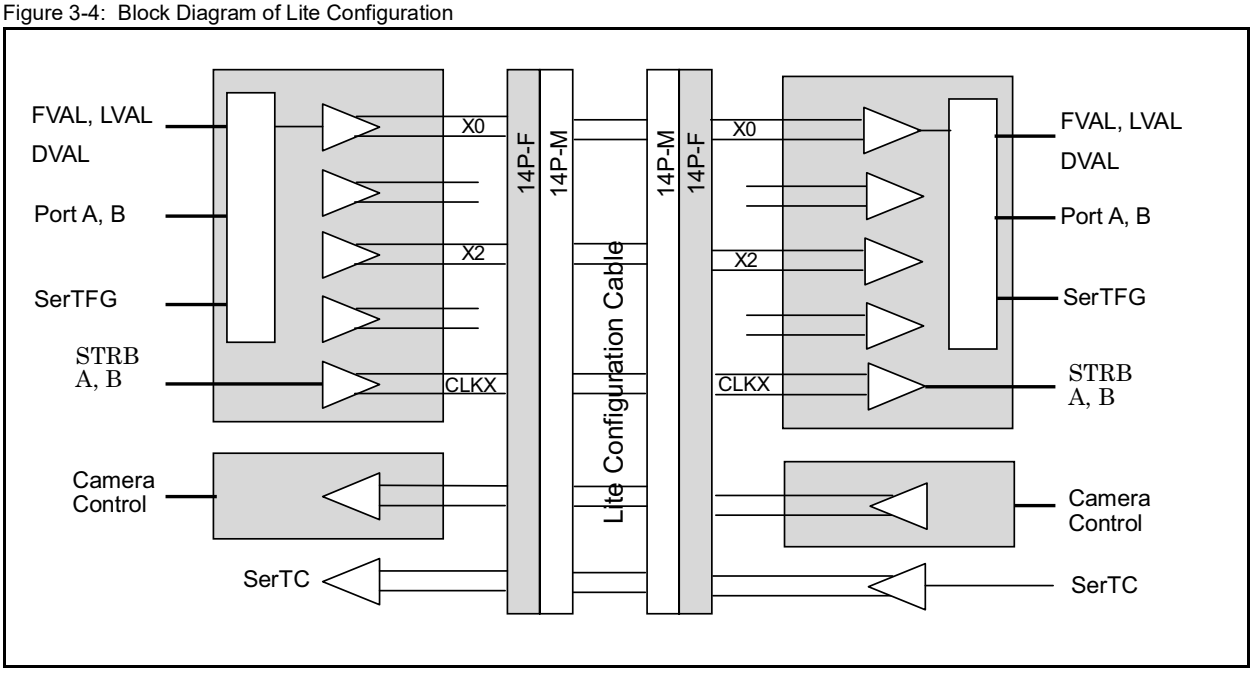


Figure 3-4: Block Diagram of Lite Configuration



3.2.3 80 bit Configuration

Figure 3-5 shows the hardware routing for the 80 bit, 10-tap/8-bit configuration and for the 80 bit, 8-tap/10-bit configuration. Figure 3-6 shows the hardware routing for the 80 bit, 8-tap/10-bit configurations. Figure 3-7 shows the block diagram for the 80 bit, 8-tap/10-bit configuration.

Figure 3-5: Data Routing for 80 bit Configurations

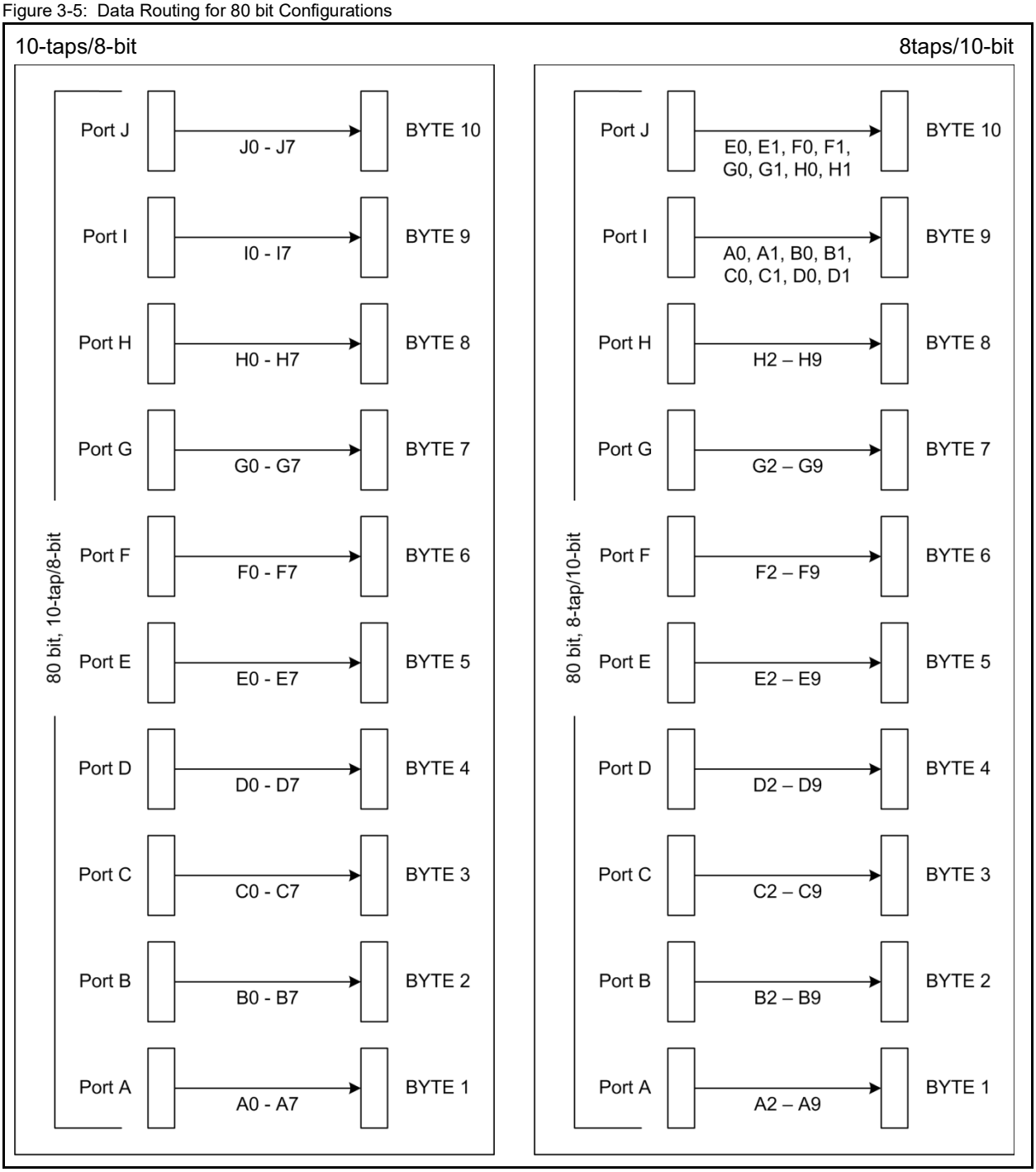


Figure 3-6: Block Diagram of 80 bit, 10-tap/8-bit Configuration

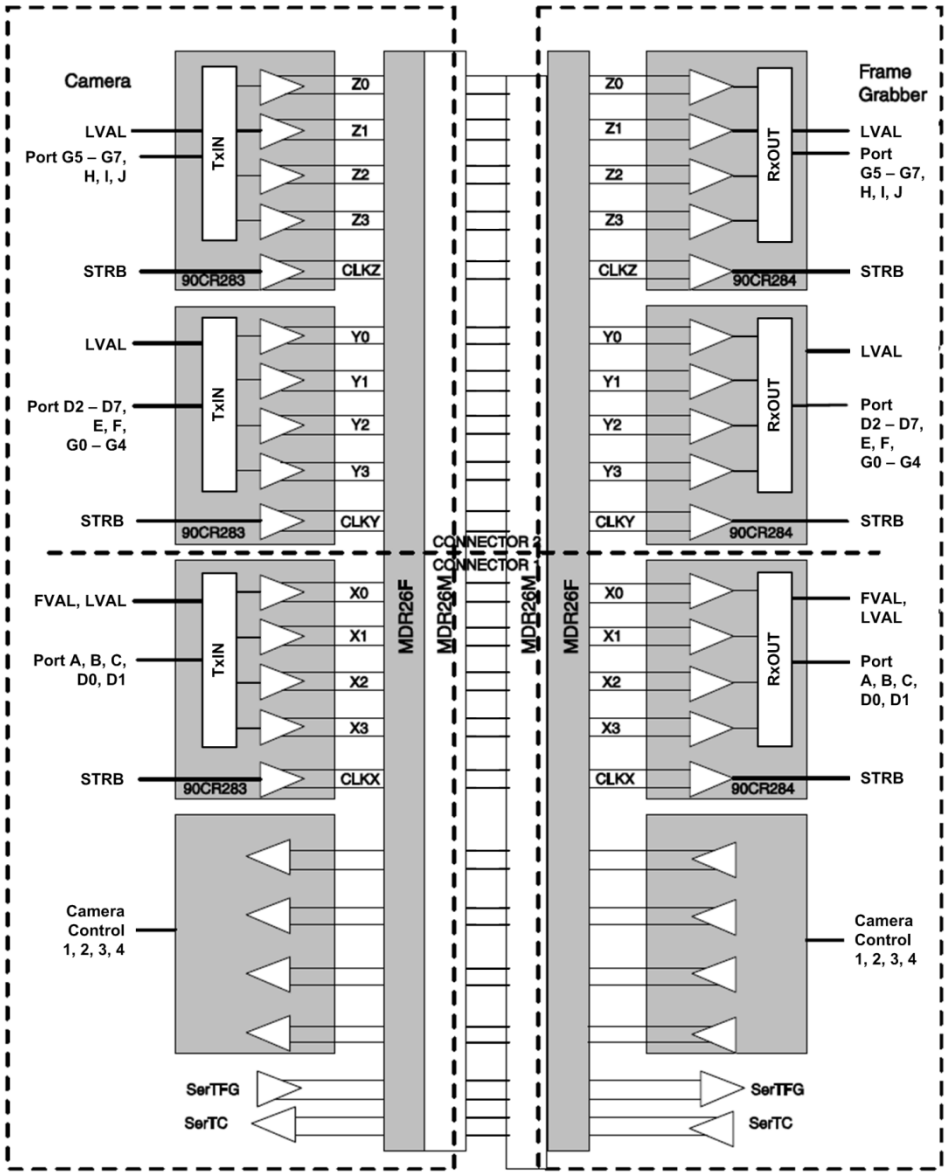
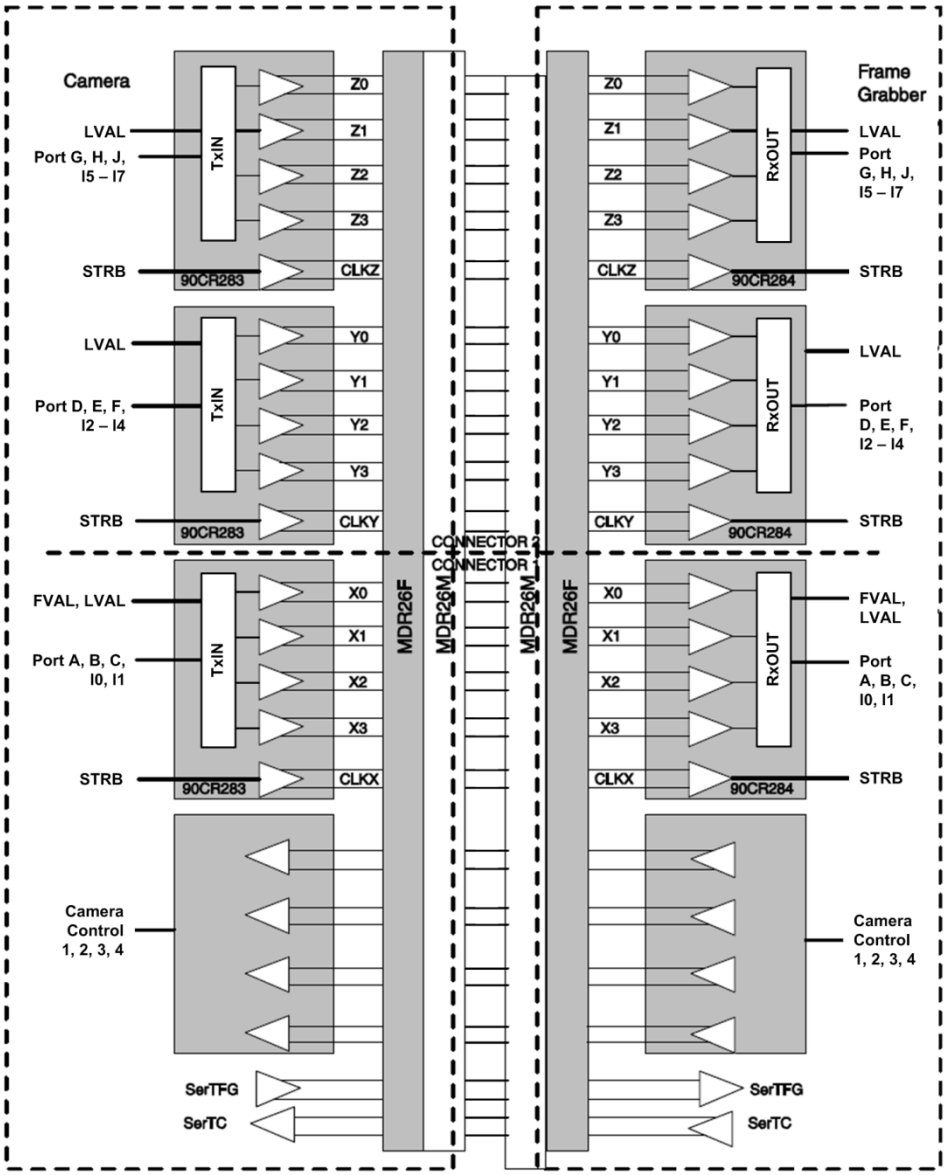


Figure 3-7: Block Diagram of 80 bit, 8-tap/10-bit Configuration



4.0 Bit Assignments

4.1 Official List of Bit Assignments

This document contains the latest bit assignments at the time that it was published. It is possible that newer formats and/or corrections may occur after this specification is released. If a format is not listed here, or there are some questions about an approved format, please go to the AIA website, search for the Camera Link standard's page, and then look for updates to this specification.

4.2 Bit Assignment Tables

The tables in this chapter list the chip, port and signal name for every bit in each Camera Link output format. There are separate tables for each bit depth per channel (e.g. 8 bits per channel, 10 bits per channel) and for each major format group (e.g. Base/Medium/Full/72-Bit, 80-Bit).

Each column of a Bit Assignment Table represents a group of tap formats. All of the tap formats in a group will have the same number of color planes (e.g. Mono, RGB). The groups are also separated by Camera Link format: Base, Medium, Full, 72-Bit and 80-bit. A group may include more than tap count (e.g. Base 2-tap and Base 3-tap). These tables are agnostic with regards to how the taps are physically related to sensor architecture.

Each row of a Bit Assignment Table represents an input/output signal (TX1/RX1 to TX27/RX27) on one of three Channel Link chips (X, Y and Z). The signal assignments are the same on the transmitter and receiver chips. The port assignment is also included (A to J).

Note: This section combines sections 4 and 5 of Camera Link v2.0 to aid clarity.

4.2.1 Bit Assignment Tables Formatting

The first column of the Bit Assignment Tables is the Channel Link chip input/output signal name, it uses the following format:

Chip.Port.Signal

Where:

Chip = The chip: X, Y or Z

Port = The port: A, B, C, D, E, F, G, H, I or J. Note "V" indicates the pin is used for synchronization signals

Signal = The name of input/output signal on the Channel Link chip (TX and RX removed)

For example "X.A.27" is the signal on Chip X, Port A with the name TX27/RX27

Each cell represents the bit that is assigned to that row's pin. These take on the format:

ColorTap.Bit

Where:

Color = The color channel: M (Monochrome), R (Red), G (Green), B (Blue) or I (Infrared or other spectrum)

Tap = The tap number

Bit = The bit number for this tap

For example "M4.2" is bit 2 on tap 4 of a monochrome format.

In all cases, bit 0 is the Least Significant Bit (LSB) in each tap. For example "M4.0" is the LSB for tap 4. The MSB depends on the bit depth. For example, for 10-bit monochrome, "M4.9" will be the MSB for tap 4.

4.2.2 Multiple Time Slice Formats

Some formats require multiple time slices in order to acquire all of the bits of the pixel. Each camera link clock executes one time slice. Time slice formats are shown in the following tables in multiple adjacent columns labeled "time slice tx" where "tx" is the time slice number.

4.3 8-Bit Modes, Base/Medium/Full

Table 4-1: 8-Bit Modes, Base/Medium/Full

Chip.Port.Signal	Mono Base 1,2,3 taps	Mono Medium 4,5,6 taps	Mono Full 7,8,9 taps	RGB Base 1 tap	RGB Medium 2 taps	RGB Full 3 taps	RGBI Medium 1 tap	RGBI Full 2 taps
X.V.24	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
X.V.25	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
X.V.26	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
X.V.23	Spare	Spare	Spare	Spare	Spare	Spare	Spare	Spare
Y.V.24		LVAL	LVAL		LVAL	LVAL	LVAL	LVAL
Y.V.25		FVAL	FVAL		FVAL	FVAL	FVAL	FVAL
Y.V.26		DVAL	DVAL		DVAL	DVAL	DVAL	DVAL
Y.V.23		Spare	Spare		Spare	Spare	Spare	Spare
Z.V.24		LVAL	LVAL			LVAL		LVAL
Z.V.25		FVAL	FVAL			FVAL		FVAL
Z.V.26		DVAL	DVAL			DVAL		DVAL
Z.V.23		Spare	Spare			Spare		Spare
X.A.0	M1.0 (LSB)	M1.0 (LSB)	M1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)
X.A.1	M1.1	M1.1	M1.1	R1.1	R1.1	R1.1	R1.1	R1.1
X.A.2	M1.2	M1.2	M1.2	R1.2	R1.2	R1.2	R1.2	R1.2
X.A.3	M1.3	M1.3	M1.3	R1.3	R1.3	R1.3	R1.3	R1.3
X.A.4	M1.4	M1.4	M1.4	R1.4	R1.4	R1.4	R1.4	R1.4
X.A.6	M1.5	M1.5	M1.5	R1.5	R1.5	R1.5	R1.5	R1.5
X.A.27	M1.6	M1.6	M1.6	R1.6	R1.6	R1.6	R1.6	R1.6
X.A.5	M1.7	M1.7	M1.7	R1.7	R1.7	R1.7	R1.7	R1.7
X.B.7	M2.0 (LSB)	M2.0 (LSB)	M2.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)
X.B.8	M2.1	M2.1	M2.1	G1.1	G1.1	G1.1	G1.1	G1.1
X.B.9	M2.2	M2.2	M2.2	G1.2	G1.2	G1.2	G1.2	G1.2
X.B.12	M2.3	M2.3	M2.3	G1.3	G1.3	G1.3	G1.3	G1.3
X.B.13	M2.4	M2.4	M2.4	G1.4	G1.4	G1.4	G1.4	G1.4
X.B.14	M2.5	M2.5	M2.5	G1.5	G1.5	G1.5	G1.5	G1.5
X.B.10	M2.6	M2.6	M2.6	G1.6	G1.6	G1.6	G1.6	G1.6
X.B.11	M2.7	M2.7	M2.7	G1.7	G1.7	G1.7	G1.7	G1.7
X.C.15	M3.0 (LSB)	M3.0 (LSB)	M3.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)
X.C.18	M3.1	M3.1	M3.1	B1.1	B1.1	B1.1	B1.1	B1.1
X.C.19	M3.2	M3.2	M3.2	B1.2	B1.2	B1.2	B1.2	B1.2
X.C.20	M3.3	M3.3	M3.3	B1.3	B1.3	B1.3	B1.3	B1.3
X.C.21	M3.4	M3.4	M3.4	B1.4	B1.4	B1.4	B1.4	B1.4
X.C.22	M3.5	M3.5	M3.5	B1.5	B1.5	B1.5	B1.5	B1.5
X.C.16	M3.6	M3.6	M3.6	B1.6	B1.6	B1.6	B1.6	B1.6
X.C.17	M3.7	M3.7	M3.7	B1.7	B1.7	B1.7	B1.7	B1.7
Y.D.0		M4.0 (LSB)	M4.0 (LSB)		R2.0 (LSB)	R2.0 (LSB)	I1.0 (LSB)	I1.0 (LSB)
Y.D.1		M4.1	M4.1		R2.1	R2.1	I1.1	I1.1
Y.D.2		M4.2	M4.2		R2.2	R2.2	I1.2	I1.2
Y.D.3		M4.3	M4.3		R2.3	R2.3	I1.3	I1.3
Y.D.4		M4.4	M4.4		R2.4	R2.4	I1.4	I1.4
Y.D.6		M4.5	M4.5		R2.5	R2.5	I1.5	I1.5
Y.D.27		M4.6	M4.6		R2.6	R2.6	I1.6	I1.6
Y.D.5		M4.7	M4.7		R2.7	R2.7	I1.7	I1.7
Y.E.7		M5.0 (LSB)	M5.0 (LSB)		G2.0 (LSB)	G2.0 (LSB)		R2.0 (LSB)
Y.E.8		M5.1	M5.1		G2.1	G2.1		R2.1
Y.E.9		M5.2	M5.2		G2.2	G2.2		R2.2
Y.E.12		M5.3	M5.3		G2.3	G2.3		R2.3
Y.E.13		M5.4	M5.4		G2.4	G2.4		R2.4
Y.E.14		M5.5	M5.5		G2.5	G2.5		R2.5
Y.E.10		M5.6	M5.6		G2.6	G2.6		R2.6
Y.E.11		M5.7	M5.7		G2.7	G2.7		R2.7
Y.F.15		M6.0 (LSB)	M6.0 (LSB)		B2.0 (LSB)	B2.0 (LSB)		G2.0 (LSB)
Y.F.18		M6.1	M6.1		B2.1	B2.1		G2.1
Y.F.19		M6.2	M6.2		B2.2	B2.2		G2.2
Y.F.20		M6.3	M6.3		B2.3	B2.3		G2.3
Y.F.21		M6.4	M6.4		B2.4	B2.4		G2.4
Y.F.22		M6.5	M6.5		B2.5	B2.5		G2.5
Y.F.16		M6.6	M6.6		B2.6	B2.6		G2.6
Y.F.17		M6.7	M6.7		B2.7	B2.7		G2.7
Z.G.0			M7.0 (LSB)			R3.0 (LSB)		B2.0 (LSB)
Z.G.1			M7.1			R3.1		B2.1
Z.G.2		M7.2		R3.2			B2.2	
Z.G.3		M7.3		R3.3			B2.3	
Z.G.4		M7.4		R3.4			B2.4	
Z.G.6		M7.5		R3.5			B2.5	
Z.G.27		M7.6		R3.6			B2.6	
Z.G.5		M7.7		R3.7			B2.7	
Z.H.7		M8.0 (LSB)		G3.0 (LSB)			I2.0 (LSB)	
Z.H.8		M8.1		G3.1			I2.1	
Z.H.9		M8.2		G3.2			I2.2	
Z.H.12		M8.3		G3.3			I2.3	
Z.H.13		M8.4		G3.4			I2.4	
Z.H.14		M8.5		G3.5			I2.5	
Z.H.10		M8.6		G3.6			I2.6	
Z.H.11		M8.7		G3.7			I2.7	
Z.I.15		M9.0 (LSB)		B3.0 (LSB)				
Z.I.18		M9.1		B3.1				
Z.I.19		M9.2		B3.2				
Z.I.20		M9.3		B3.3				
Z.I.21		M9.4		B3.4				
Z.I.22		M9.5		B3.5				
Z.I.16		M9.6		B3.6				
Z.I.17		M9.7		B3.7				

4.4 8-Bit Modes, 80-bit

Table 4-2: 8-Bit Modes, 80-bit

Chip.Port.Signal	Mono 10 tap	RGB 10-tap		
		time slice t1	time slice t2	time slice t3
X.V.24	LVAL	LVAL	LVAL	LVAL
X.V.25	FVAL	FVAL	FVAL	FVAL
Y.V.27	LVAL	LVAL	LVAL	LVAL
Z.V.27	LVAL	LVAL	LVAL	LVAL
X.A.0	M1.0 (LSB)	R1.0 (LSB)	G4.0 (LSB)	B7.0 (LSB)
X.A.1	M1.1	R1.1	G4.1	B7.1
X.A.2	M1.2	R1.2	G4.2	B7.2
X.A.3	M1.3	R1.3	G4.3	B7.3
X.A.4	M1.4	R1.4	G4.4	B7.4
X.A.5	M1.5	R1.5	G4.5	B7.5
X.A.6	M1.6	R1.6	G4.6	B7.6
X.A.7	M1.7	R1.7	G4.7	B7.7
X.B.8	M2.0 (LSB)	G1.0 (LSB)	B4.0 (LSB)	R8.0 (LSB)
X.B.9	M2.1	G1.1	B4.1	R8.1
X.B.10	M2.2	G1.2	B4.2	R8.2
X.B.11	M2.3	G1.3	B4.3	R8.3
X.B.12	M2.4	G1.4	B4.4	R8.4
X.B.13	M2.5	G1.5	B4.5	R8.5
X.B.14	M2.6	G1.6	B4.6	R8.6
X.B.15	M2.7	G1.7	B4.7	R8.7
X.C.16	M3.0 (LSB)	B1.0 (LSB)	R5.0 (LSB)	G8.0 (LSB)
X.C.17	M3.1	B1.1	R5.1	G8.1
X.C.18	M3.2	B1.2	R5.2	G8.2
X.C.19	M3.3	B1.3	R5.3	G8.3
X.C.20	M3.4	B1.4	R5.4	G8.4
X.C.21	M3.5	B1.5	R5.5	G8.5
X.C.22	M3.6	B1.6	R5.6	G8.6
X.C.23	M3.7	B1.7	R5.7	G8.7
X.D.26	M4.0 (LSB)	R2.0 (LSB)	G5.0 (LSB)	B8.0 (LSB)
X.D.27	M4.1	R2.1	G5.1	B8.1
Y.D.0	M4.2	R2.2	G5.2	B8.2
Y.D.1	M4.3	R2.3	G5.3	B8.3
Y.D.2	M4.4	R2.4	G5.4	B8.4
Y.D.3	M4.5	R2.5	G5.5	B8.5
Y.D.4	M4.6	R2.6	G5.6	B8.6
Y.D.5	M4.7	R2.7	G5.7	B8.7
Y.E.6	M5.0 (LSB)	G2.0 (LSB)	B5.0 (LSB)	R9.0 (LSB)
Y.E.7	M5.1	G2.1	B5.1	R9.1
Y.E.8	M5.2	G2.2	B5.2	R9.2
Y.E.9	M5.3	G2.3	B5.3	R9.3
Y.E.10	M5.4	G2.4	B5.4	R9.4
Y.E.11	M5.5	G2.5	B5.5	R9.5
Y.E.12	M5.6	G2.6	B5.6	R9.6
Y.E.13	M5.7	G2.7	B5.7	R9.7
Y.F.14	M6.0 (LSB)	B2.0 (LSB)	R6.0 (LSB)	G9.0 (LSB)
Y.F.15	M6.1	B2.1	R6.1	G9.1
Y.F.16	M6.2	B2.2	R6.2	G9.2
Y.F.17	M6.3	B2.3	R6.3	G9.3
Y.F.18	M6.4	B2.4	R6.4	G9.4
Y.F.19	M6.5	B2.5	R6.5	G9.5
Y.F.20	M6.6	B2.6	R6.6	G9.6
Y.F.21	M6.7	B2.7	R6.7	G9.7
Y.G.22	M7.0 (LSB)	R3.0 (LSB)	G6.0 (LSB)	B9.0 (LSB)
Y.G.23	M7.1	R3.1	G6.1	B9.1
Y.G.24	M7.2	R3.2	G6.2	B9.2
Y.G.25	M7.3	R3.3	G6.3	B9.3
Y.G.26	M7.4	R3.4	G6.4	B9.4
Z.G.0	M7.5	R3.5	G6.5	B9.5
Z.G.1	M7.6	R3.6	G6.6	B9.6
Z.G.2	M7.7	R3.7	G6.7	B9.7
Z.H.3	M8.0 (LSB)	G3.0 (LSB)	B6.0 (LSB)	R10.0 (LSB)
Z.H.4	M8.1	G3.1	B6.1	R10.1
Z.H.5	M8.2	G3.2	B6.2	R10.2
Z.H.6	M8.3	G3.3	B6.3	R10.3
Z.H.7	M8.4	G3.4	B6.4	R10.4
Z.H.8	M8.5	G3.5	B6.5	R10.5
Z.H.9	M8.6	G3.6	B6.6	R10.6
Z.H.10	M8.7	G3.7	B6.7	R10.7
Z.I.11	M9.0 (LSB)	B3.0 (LSB)	R7.0 (LSB)	G10.0 (LSB)
Z.I.12	M9.1	B3.1	R7.1	G10.1
Z.I.13	M9.2	B3.2	R7.2	G10.2
Z.I.14	M9.3	B3.3	R7.3	G10.3
Z.I.15	M9.4	B3.4	R7.4	G10.4
Z.I.16	M9.5	B3.5	R7.5	G10.5
Z.I.17	M9.6	B3.6	R7.6	G10.6
Z.I.18	M9.7	B3.7	R7.7	G10.7
Z.J.19	M10.0 (LSB)	R4.0 (LSB)	G7.0 (LSB)	B10.0 (LSB)
Z.J.20	M10.1	R4.1	G7.1	B10.1
Z.J.21	M10.2	R4.2	G7.2	B10.2
Z.J.22	M10.3	R4.3	G7.3	B10.3
Z.J.23	M10.4	R4.4	G7.4	B10.4
Z.J.24	M10.5	R4.5	G7.5	B10.5
Z.J.25	M10.6	R4.6	G7.6	B10.6
Z.J.26	M10.7	R4.7	G7.7	B10.7

4.5 10-Bit Modes, Base/Medium/Full

Table 4-3: 10-Bit Modes, Base/Medium/Full

Chip.Port.Signal	Mono Base 1,2 taps	Mono Medium 3,4 taps	Mono Full 5,6 taps	RGB Medium 1 tap	RGB Full 2 taps	RGBI Medium 1 tap
X.V.24	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
X.V.25	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
X.V.26	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
X.V.23	Spare	Spare	Spare	Spare	Spare	Spare
Y.V.24	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
Y.V.25	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
Y.V.26	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
Y.V.23	Spare	Spare	Spare	Spare	Spare	Spare
Z.V.24			LVAL		LVAL	
Z.V.25			FVAL		FVAL	
Z.V.26			DVAL		DVAL	
Z.V.23			Spare		Spare	
X.A.0	M1.0 (LSB)	M1.0 (LSB)	M1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)
X.A.1	M1.1	M1.1	M1.1	R1.1	R1.1	R1.1
X.A.2	M1.2	M1.2	M1.2	R1.2	R1.2	R1.2
X.A.3	M1.3	M1.3	M1.3	R1.3	R1.3	R1.3
X.A.4	M1.4	M1.4	M1.4	R1.4	R1.4	R1.4
X.A.6	M1.5	M1.5	M1.5	R1.5	R1.5	R1.5
X.A.27	M1.6	M1.6	M1.6	R1.6	R1.6	R1.6
X.A.5	M1.7	M1.7	M1.7	R1.7	R1.7	R1.7
X.B.7	M1.8	M1.8	M1.8	R1.8	R1.8	R1.8
X.B.8	M1.9	M1.9	M1.9	R1.9	R1.9	R1.9
X.B.9						
X.B.12						
X.B.13	M2.8	M2.8	M2.8	B1.8	B1.8	B1.8
X.B.14	M2.9	M2.9	M2.9	B1.9	B1.9	B1.9
X.B.10						
X.B.11						
X.C.15	M2.0 (LSB)	M2.0 (LSB)	M2.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)
X.C.18	M2.1	M2.1	M2.1	B1.1	B1.1	B1.1
X.C.19	M2.2	M2.2	M2.2	B1.2	B1.2	B1.2
X.C.20	M2.3	M2.3	M2.3	B1.3	B1.3	B1.3
X.C.21	M2.4	M2.4	M2.4	B1.4	B1.4	B1.4
X.C.22	M2.5	M2.5	M2.5	B1.5	B1.5	B1.5
X.C.16	M2.6	M2.6	M2.6	B1.6	B1.6	B1.6
X.C.17	M2.7	M2.7	M2.7	B1.7	B1.7	B1.7
Y.D.0		M4.0 (LSB)	M4.0 (LSB)		R2.0 (LSB)	I1.0 (LSB)
Y.D.1		M4.1	M4.1		R2.1	I1.1
Y.D.2		M4.2	M4.2		R2.2	I1.2
Y.D.3		M4.3	M4.3		R2.3	I1.3
Y.D.4		M4.4	M4.4		R2.4	I1.4
Y.D.6		M4.5	M4.5		R2.5	I1.5
Y.D.27		M4.6	M4.6		R2.6	I1.6
Y.D.5		M4.7	M4.7		R2.7	I1.7
Y.E.7		M3.0 (LSB)	M3.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)
Y.E.8		M3.1	M3.1	G1.1	G1.1	G1.1
Y.E.9		M3.2	M3.2	G1.2	G1.2	G1.2
Y.E.12		M3.3	M3.3	G1.3	G1.3	G1.3
Y.E.13		M3.4	M3.4	G1.4	G1.4	G1.4
Y.E.14		M3.5	M3.5	G1.5	G1.5	G1.5
Y.E.10		M3.6	M3.6	G1.6	G1.6	G1.6
Y.E.11		M3.7	M3.7	G1.7	G1.7	G1.7
Y.F.15		M3.8	M3.8	G1.8	G1.8	G1.8
Y.F.18		M3.9	M3.9	G1.9	G1.9	G1.9
Y.F.19						
Y.F.20						
Y.F.21		M4.8	M4.8		R2.8	I1.8
Y.F.22		M4.9	M4.9		R2.9	I1.9
Y.F.16						
Y.F.17						
Z.G.0			M5.0 (LSB)		B2.0 (LSB)	
Z.G.1			M5.1		B2.1	
Z.G.2			M5.2		B2.2	
Z.G.3			M5.3		B2.3	
Z.G.4			M5.4		B2.4	
Z.G.6			M5.5		B2.5	
Z.G.27			M5.6		B2.6	
Z.G.5			M5.7		B2.7	
Z.H.7			M5.8		B2.8	
Z.H.8			M5.9		B2.9	
Z.H.9						
Z.H.12						
Z.H.13			M6.8		G2.8	
Z.H.14			M6.9		G2.9	
Z.H.10						
Z.H.11						
Z.I.15			M6.0 (LSB)		G2.0 (LSB)	
Z.I.18			M6.1		G2.1	
Z.I.19			M6.2		G2.2	
Z.I.20			M6.3		G2.3	
Z.I.21			M6.4		G2.4	
Z.I.22			M6.5		G2.5	
Z.I.16			M6.6		G2.6	
Z.I.17			M6.7		G2.7	

4.6 10-Bit Modes, 80-bit

Table 4-4: 10-Bit Modes, 80-bit

Chip.Port.Signal	Mono 7,8 taps	RGBI 2 taps	RGB 8-tap		
			time slice t1	time slice t2	time slice t3
X.V.24	LVAL	LVAL	LVAL	LVAL	LVAL
X.V.25	FVAL	FVAL	FVAL	FVAL	FVAL
Y.V.24	LVAL	LVAL	LVAL	LVAL	LVAL
Z.V.24	LVAL	LVAL	LVAL	LVAL	LVAL
X.A.0	M1.2	R1.2	R1.2	B3.2	G6.2
X.A.1	M1.3	R1.3	R1.3	B3.3	G6.3
X.A.2	M1.4	R1.4	R1.4	B3.4	G6.4
X.A.3	M1.5	R1.5	R1.5	B3.5	G6.5
X.A.4	M1.6	R1.6	R1.6	B3.6	G6.6
X.A.6	M1.7	R1.7	R1.7	B3.7	G6.7
X.A.27	M1.8	R1.8	R1.8	B3.8	G6.8
X.A.5	M1.9	R1.9	R1.9	B3.9	G6.9
X.B.7	M2.2	G1.2	G1.2	R4.2	B6.2
X.B.8	M2.3	G1.3	G1.3	R4.3	B6.3
X.B.9	M2.4	G1.4	G1.4	R4.4	B6.4
X.B.12	M2.5	G1.5	G1.5	R4.5	B6.5
X.B.13	M2.6	G1.6	G1.6	R4.6	B6.6
X.B.14	M2.7	G1.7	G1.7	R4.7	B6.7
X.B.10	M2.8	G1.8	G1.8	R4.8	B6.8
X.B.11	M2.9	G1.9	G1.9	R4.9	B6.9
X.C.15	M3.2	B1.2	B1.2	G4.2	R7.2
X.C.18	M3.3	B1.3	B1.3	G4.3	R7.3
X.C.19	M3.4	B1.4	B1.4	G4.4	R7.4
X.C.20	M3.5	B1.5	B1.5	G4.5	R7.5
X.C.21	M3.6	B1.6	B1.6	G4.6	R7.6
X.C.22	M3.7	B1.7	B1.7	G4.7	R7.7
X.C.16	M3.8	B1.8	B1.8	G4.8	R7.8
X.C.17	M3.9	B1.9	B1.9	G4.9	R7.9
Y.D.0	M4.2	I1.2	R2.2	B4.2	G7.2
Y.D.1	M4.3	I1.3	R2.3	B4.3	G7.3
Y.D.2	M4.4	I1.4	R2.4	B4.4	G7.4
Y.D.3	M4.5	I1.5	R2.5	B4.5	G7.5
Y.D.4	M4.6	I1.6	R2.6	B4.6	G7.6
Y.D.6	M4.7	I1.7	R2.7	B4.7	G7.7
Y.D.27	M4.8	I1.8	R2.8	B4.8	G7.8
Y.D.5	M4.9	I1.9	R2.9	B4.9	G7.9
Y.E.7	M5.2	R2.2	G2.2	R5.2	B7.2
Y.E.8	M5.3	R2.3	G2.3	R5.3	B7.3
Y.E.9	M5.4	R2.4	G2.4	R5.4	B7.4
Y.E.12	M5.5	R2.5	G2.5	R5.5	B7.5
Y.E.13	M5.6	R2.6	G2.6	R5.6	B7.6
Y.E.14	M5.7	R2.7	G2.7	R5.7	B7.7
Y.E.10	M5.8	R2.8	G2.8	R5.8	B7.8
Y.E.11	M5.9	R2.9	G2.9	R5.9	B7.9
Y.F.15	M6.2	G2.2	B2.2	G5.2	R8.2
Y.F.18	M6.3	G2.3	B2.3	G5.3	R8.3
Y.F.19	M6.4	G2.4	B2.4	G5.4	R8.4
Y.F.20	M6.5	G2.5	B2.5	G5.5	R8.5
Y.F.21	M6.6	G2.6	B2.6	G5.6	R8.6
Y.F.22	M6.7	G2.7	B2.7	G5.7	R8.7
Y.F.16	M6.8	G2.8	B2.8	G5.8	R8.8
Y.F.17	M6.9	G2.9	B2.9	G5.9	R8.9
Z.G.0	M7.2	B2.2	R3.2	B5.2	G8.2
Z.G.1	M7.3	B2.3	R3.3	B5.3	G8.3
Z.G.2	M7.4	B2.4	R3.4	B5.4	G8.4
Z.G.3	M7.5	B2.5	R3.5	B5.5	G8.5
Z.G.4	M7.6	B2.6	R3.6	B5.6	G8.6
Z.G.6	M7.7	B2.7	R3.7	B5.7	G8.7
Z.G.27	M7.8	B2.8	R3.8	B5.8	G8.8
Z.G.5	M7.9	B2.9	R3.9	B5.9	G8.9
Z.H.7	M8.2	I2.2	G3.2	R6.2	B8.2
Z.H.8	M8.3	I2.3	G3.3	R6.3	B8.3
Z.H.9	M8.4	I2.4	G3.4	R6.4	B8.4
Z.H.12	M8.5	I2.5	G3.5	R6.5	B8.5
Z.H.13	M8.6	I2.6	G3.6	R6.6	B8.6
Z.H.14	M8.7	I2.7	G3.7	R6.7	B8.7
Z.H.10	M8.8	I2.8	G3.8	R6.8	B8.8
Z.H.11	M8.9	I2.9	G3.9	R6.9	B8.9
X.I.26	M1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)	B3.0 (LSB)	G6.0 (LSB)
X.I.23	M1.1	R1.1	R1.1	B3.1	G6.1
Y.I.25	M2.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)	R4.0 (LSB)	B6.0 (LSB)
Y.I.26	M2.1	G1.1	G1.1	R4.1	B6.1
Y.I.23	M3.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)	G4.0 (LSB)	R7.0 (LSB)
Z.I.15	M3.1	B1.1	B1.1	G4.1	R7.1
Z.I.18	M4.0 (LSB)	I1.0 (LSB)	R2.0 (LSB)	B4.0 (LSB)	G7.0 (LSB)
Z.I.19	M4.1	I1.1	R2.1	B4.1	G7.1
Z.J.20	M5.0 (LSB)	R2.0 (LSB)	G2.0 (LSB)	R5.0 (LSB)	B7.0 (LSB)
Z.J.21	M5.1	R2.1	G2.1	R5.1	B7.1
Z.J.22	M6.0 (LSB)	G2.0 (LSB)	B2.0 (LSB)	G5.0 (LSB)	R8.0 (LSB)
Z.J.16	M6.1	G2.1	B2.1	G5.1	R8.1
Z.J.17	M7.0 (LSB)	B2.0 (LSB)	R3.0 (LSB)	B5.0 (LSB)	G8.0 (LSB)
Z.J.25	M7.1	B2.1	R3.1	B5.1	G8.1
Z.J.26	M8.0 (LSB)	I2.0 (LSB)	G3.0 (LSB)	R6.0 (LSB)	B8.0 (LSB)
Z.J.23	M8.1	I2.1	G3.1	R6.1	B8.1

4.7 12-Bit Modes, Base/Medium/Full

Table 4-5: 12-Bit Modes, Base/Medium/Full

Chip.Port.Signal	Mono Base 1,2 taps	Mono Medium 3,4 taps	Mono Full 5,6 taps	RGB Medium 1 tap	RGB Full 2 taps	RGBI Medium 1 tap
X.V.24	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
X.V.25	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
X.V.26	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
X.V.23	Spare	Spare	Spare	Spare	Spare	Spare
Y.V.24		LVAL	LVAL	LVAL	LVAL	LVAL
Y.V.25		FVAL	FVAL	FVAL	FVAL	FVAL
Y.V.26		DVAL	DVAL	DVAL	DVAL	DVAL
Y.V.23		Spare	Spare	Spare	Spare	Spare
Z.V.24			LVAL		LVAL	
Z.V.25			FVAL		FVAL	
Z.V.26			DVAL		DVAL	
Z.V.23			Spare		Spare	
X.A.0	M1.0 (LSB)	M1.0 (LSB)	M1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)
X.A.1	M1.1	M1.1	M1.1	R1.1	R1.1	R1.1
X.A.2	M1.2	M1.2	M1.2	R1.2	R1.2	R1.2
X.A.3	M1.3	M1.3	M1.3	R1.3	R1.3	R1.3
X.A.4	M1.4	M1.4	M1.4	R1.4	R1.4	R1.4
X.A.6	M1.5	M1.5	M1.5	R1.5	R1.5	R1.5
X.A.27	M1.6	M1.6	M1.6	R1.6	R1.6	R1.6
X.A.5	M1.7	M1.7	M1.7	R1.7	R1.7	R1.7
X.B.7	M1.8	M1.8	M1.8	R1.8	R1.8	R1.8
X.B.8	M1.9	M1.9	M1.9	R1.9	R1.9	R1.9
X.B.9	M1.10	M1.10	M1.10	R1.10	R1.10	R1.10
X.B.12	M1.11	M1.11	M1.11	R1.11	R1.11	R1.11
X.B.13	M2.8	M2.8	M2.8	B1.8	B1.8	B1.8
X.B.14	M2.9	M2.9	M2.9	B1.9	B1.9	B1.9
X.B.10	M2.10	M2.10	M2.10	B1.10	B1.10	B1.10
X.B.11	M2.11	M2.11	M2.11	B1.11	B1.11	B1.11
X.C.15	M2.0 (LSB)	M2.0 (LSB)	M2.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)
X.C.18	M2.1	M2.1	M2.1	B1.1	B1.1	B1.1
X.C.19	M2.2	M2.2	M2.2	B1.2	B1.2	B1.2
X.C.20	M2.3	M2.3	M2.3	B1.3	B1.3	B1.3
X.C.21	M2.4	M2.4	M2.4	B1.4	B1.4	B1.4
X.C.22	M2.5	M2.5	M2.5	B1.5	B1.5	B1.5
X.C.16	M2.6	M2.6	M2.6	B1.6	B1.6	B1.6
X.C.17	M2.7	M2.7	M2.7	B1.7	B1.7	B1.7
Y.D.0		M4.0 (LSB)	M4.0 (LSB)		R2.0 (LSB)	I1.0 (LSB)
Y.D.1		M4.1	M4.1		R2.1	I1.1
Y.D.2		M4.2	M4.2		R2.2	I1.2
Y.D.3		M4.3	M4.3		R2.3	I1.3
Y.D.4		M4.4	M4.4		R2.4	I1.4
Y.D.6		M4.5	M4.5		R2.5	I1.5
Y.D.27		M4.6	M4.6		R2.6	I1.6
Y.D.5		M4.7	M4.7		R2.7	I1.7
Y.E.7		M3.0 (LSB)	M3.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)
Y.E.8		M3.1	M3.1	G1.1	G1.1	G1.1
Y.E.9		M3.2	M3.2	G1.2	G1.2	G1.2
Y.E.12		M3.3	M3.3	G1.3	G1.3	G1.3
Y.E.13		M3.4	M3.4	G1.4	G1.4	G1.4
Y.E.14		M3.5	M3.5	G1.5	G1.5	G1.5
Y.E.10		M3.6	M3.6	G1.6	G1.6	G1.6
Y.E.11		M3.7	M3.7	G1.7	G1.7	G1.7
Y.F.15		M3.8	M3.8	G1.8	G1.8	G1.8
Y.F.18		M3.9	M3.9	G1.9	G1.9	G1.9
Y.F.19		M3.10	M3.10	G1.10	G1.10	G1.10
Y.F.20		M3.11	M3.11	G1.11	G1.11	G1.11
Y.F.21		M4.8	M4.8		R2.8	I1.8
Y.F.22		M4.9	M4.9		R2.9	I1.9
Y.F.16		M4.10	M4.10		R2.10	I1.10
Y.F.17		M4.11	M4.11		R2.11	I1.11
Z.G.0			M5.0 (LSB)		B2.0 (LSB)	
Z.G.1			M5.1		B2.1	
Z.G.2			M5.2		B2.2	
Z.G.3			M5.3		B2.3	
Z.G.4			M5.4		B2.4	
Z.G.6			M5.5		B2.5	
Z.G.27			M5.6		B2.6	
Z.G.5			M5.7		B2.7	
Z.H.7			M5.8		B2.8	
Z.H.8			M5.9		B2.9	
Z.H.9			M5.10		B2.10	
Z.H.12			M5.11		B2.11	
Z.H.13			M6.8		G2.8	
Z.H.14			M6.9		G2.9	
Z.H.10			M6.10		G2.10	
Z.H.11			M6.11		G2.11	
Z.I.15			M6.0 (LSB)		G2.0 (LSB)	
Z.I.18			M6.1		G2.1	
Z.I.19			M6.2		G2.2	
Z.I.20			M6.3		G2.3	
Z.I.21			M6.4		G2.4	
Z.I.22			M6.5		G2.5	
Z.I.16			M6.6		G2.6	
Z.I.17			M6.7		G2.7	

4.8 14-Bit Modes, Base/Medium/Full/72-Bit

Table 4-6: 14-Bit Modes, Base/Medium/Full/72 Bit

Chip.Port.Signal	Mono Base 1 tap	Mono Medium 2,3 taps	Mono Full 4 taps	Mono 72-Bit 5 taps	RGB Medium 1 tap	RGBI Full 1 tap
X.V.24	LVAL	LVAL	LVAL	LVAL	LVAL	LVAL
X.V.25	FVAL	FVAL	FVAL	FVAL	FVAL	FVAL
X.V.26	DVAL	DVAL	DVAL	DVAL	DVAL	DVAL
X.V.23	Spare	Spare	Spare	Spare	Spare	Spare
Y.V.24		LVAL	LVAL	LVAL	LVAL	LVAL
Y.V.25		FVAL	FVAL	FVAL	FVAL	FVAL
Y.V.26		DVAL	DVAL	DVAL	DVAL	DVAL
Y.V.23		Spare	Spare	Spare	Spare	Spare
Z.V.24			LVAL	LVAL		LVAL
Z.V.25			FVAL	FVAL		FVAL
Z.V.26			DVAL	DVAL		DVAL
Z.V.23			Spare	Spare		Spare
X.A.0	M1.0 (LSB)	M1.0 (LSB)	M1.0 (LSB)	M1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)
X.A.1	M1.1	M1.1	M1.1	M1.1	R1.1	R1.1
X.A.2	M1.2	M1.2	M1.2	M1.2	R1.2	R1.2
X.A.3	M1.3	M1.3	M1.3	M1.3	R1.3	R1.3
X.A.4	M1.4	M1.4	M1.4	M1.4	R1.4	R1.4
X.A.6	M1.5	M1.5	M1.5	M1.5	R1.5	R1.5
X.A.27	M1.6	M1.6	M1.6	M1.6	R1.6	R1.6
X.A.5	M1.7	M1.7	M1.7	M1.7	R1.7	R1.7
X.B.7	M1.8	M1.8	M1.8	M1.8	R1.8	R1.8
X.B.8	M1.9	M1.9	M1.9	M1.9	R1.9	R1.9
X.B.9	M1.10	M1.10	M1.10	M1.10	R1.10	R1.10
X.B.12	M1.11	M1.11	M1.11	M1.11	R1.11	R1.11
X.B.13	M1.12	M1.12	M1.12	M1.12	R1.12	R1.12
X.B.14	M1.13	M1.13	M1.13	M1.13	R1.13	R1.13
X.B.10				M5.8		
X.B.11				M5.9		
X.C.15	M2.0 (LSB)	M2.0 (LSB)	M2.0 (LSB)	M2.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)
X.C.18	M2.1	M2.1	M2.1	M2.1	B1.1	B1.1
X.C.19	M2.2	M2.2	M2.2	M2.2	B1.2	B1.2
X.C.20	M2.3	M2.3	M2.3	M2.3	B1.3	B1.3
X.C.21	M2.4	M2.4	M2.4	M2.4	B1.4	B1.4
X.C.22	M2.5	M2.5	M2.5	M2.5	B1.5	B1.5
X.C.16	M2.6	M2.6	M2.6	M2.6	B1.6	B1.6
X.C.17	M2.7	M2.7	M2.7	M2.7	B1.7	B1.7
Y.D.0	M2.8	M2.8	M2.8	M2.8	B1.8	B1.8
Y.D.1	M2.9	M2.9	M2.9	M2.9	B1.9	B1.9
Y.D.2	M2.10	M2.10	M2.10	M2.10	B1.10	B1.10
Y.D.3	M2.11	M2.11	M2.11	M2.11	B1.11	B1.11
Y.D.4	M2.12	M2.12	M2.12	M2.12	B1.12	B1.12
Y.D.6	M2.13	M2.13	M2.13	M2.13	B1.13	B1.13
Y.D.27				M5.10		
Y.D.5				M5.11		
Y.E.7	M3.0 (LSB)	M3.0 (LSB)	M3.0 (LSB)	M3.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)
Y.E.8	M3.1	M3.1	M3.1	M3.1	G1.1	G1.1
Y.E.9	M3.2	M3.2	M3.2	M3.2	G1.2	G1.2
Y.E.12	M3.3	M3.3	M3.3	M3.3	G1.3	G1.3
Y.E.13	M3.4	M3.4	M3.4	M3.4	G1.4	G1.4
Y.E.14	M3.5	M3.5	M3.5	M3.5	G1.5	G1.5
Y.E.10	M3.6	M3.6	M3.6	M3.6	G1.6	G1.6
Y.E.11	M3.7	M3.7	M3.7	M3.7	G1.7	G1.7
Y.F.15	M3.8	M3.8	M3.8	M3.8	G1.8	G1.8
Y.F.18	M3.9	M3.9	M3.9	M3.9	G1.9	G1.9
Y.F.19	M3.10	M3.10	M3.10	M3.10	G1.10	G1.10
Y.F.20	M3.11	M3.11	M3.11	M3.11	G1.11	G1.11
Y.F.21	M3.12	M3.12	M3.12	M3.12	G1.12	G1.12
Y.F.22	M3.13	M3.13	M3.13	M3.13	G1.13	G1.13
Y.F.16				M5.12		
Y.F.17				M5.13		
Z.G.0			M4.0 (LSB)	M4.0 (LSB)		I1.0 (LSB)
Z.G.1			M4.1	M4.1		I1.1
Z.G.2			M4.2	M4.2		I1.2
Z.G.3			M4.3	M4.3		I1.3
Z.G.4			M4.4	M4.4		I1.4
Z.G.6			M4.5	M4.5		I1.5
Z.G.27			M4.6	M4.6		I1.6
Z.G.5			M4.7	M4.7		I1.7
Z.H.7			M4.8	M4.8		I1.8
Z.H.8			M4.9	M4.9		I1.9
Z.H.9			M4.10	M4.10		I1.10
Z.H.12			M4.11	M4.11		I1.11
Z.H.13			M4.12	M4.12		I1.12
Z.H.14			M4.13	M4.13		I1.13
Z.H.10						
Z.H.11						
Z.I.15				M5.0 (LSB)		
Z.I.18				M5.1		
Z.I.19				M5.2		
Z.I.20				M5.3		
Z.I.21				M5.4		
Z.I.22				M5.5		
Z.I.16				M5.6		
Z.I.17				M5.7		

4.9 16-Bit Modes, Base/Medium/Full

Table 4-7: 16-Bit Modes, Base/Medium/Full

Chip.Port.Signal	Mono Base 1 tap	Mono Medium 2,3 taps	Mono Full 4 taps	RGB Medium 1 tap	RGBI Full 1 tap
X.V.24	LVAL	LVAL	LVAL	LVAL	LVAL
X.V.25	FVAL	FVAL	FVAL	FVAL	FVAL
X.V.26	DVAL	DVAL	DVAL	DVAL	DVAL
X.V.23	Spare	Spare	Spare	Spare	Spare
Y.V.24		LVAL	LVAL	LVAL	LVAL
Y.V.25		FVAL	FVAL	FVAL	FVAL
Y.V.26		DVAL	DVAL	DVAL	DVAL
Y.V.23		Spare	Spare	Spare	Spare
Z.V.24			LVAL		LVAL
Z.V.25			FVAL		FVAL
Z.V.26			DVAL		DVAL
Z.V.23			Spare		Spare
X.A.0	M1.0 (LSB)	M1.0 (LSB)	M1.0 (LSB)	R1.0 (LSB)	R1.0 (LSB)
X.A.1	M1.1	M1.1	M1.1	R1.1	R1.1
X.A.2	M1.2	M1.2	M1.2	R1.2	R1.2
X.A.3	M1.3	M1.3	M1.3	R1.3	R1.3
X.A.4	M1.4	M1.4	M1.4	R1.4	R1.4
X.A.6	M1.5	M1.5	M1.5	R1.5	R1.5
X.A.27	M1.6	M1.6	M1.6	R1.6	R1.6
X.A.5	M1.7	M1.7	M1.7	R1.7	R1.7
X.B.7	M1.8	M1.8	M1.8	R1.8	R1.8
X.B.8	M1.9	M1.9	M1.9	R1.9	R1.9
X.B.9	M1.10	M1.10	M1.10	R1.10	R1.10
X.B.12	M1.11	M1.11	M1.11	R1.11	R1.11
X.B.13	M1.12	M1.12	M1.12	R1.12	R1.12
X.B.14	M1.13	M1.13	M1.13	R1.13	R1.13
X.B.10	M1.14	M1.14	M1.14	R1.14	R1.14
X.B.11	M1.15	M1.15	M1.15	R1.15	R1.15
X.C.15		M2.0 (LSB)	M2.0 (LSB)	B1.0 (LSB)	B1.0 (LSB)
X.C.18		M2.1	M2.1	B1.1	B1.1
X.C.19		M2.2	M2.2	B1.2	B1.2
X.C.20		M2.3	M2.3	B1.3	B1.3
X.C.21		M2.4	M2.4	B1.4	B1.4
X.C.22		M2.5	M2.5	B1.5	B1.5
X.C.16		M2.6	M2.6	B1.6	B1.6
X.C.17		M2.7	M2.7	B1.7	B1.7
Y.D.0		M2.8	M2.8	B1.8	B1.8
Y.D.1		M2.9	M2.9	B1.9	B1.9
Y.D.2		M2.10	M2.10	B1.10	B1.10
Y.D.3		M2.11	M2.11	B1.11	B1.11
Y.D.4		M2.12	M2.12	B1.12	B1.12
Y.D.6		M2.13	M2.13	B1.13	B1.13
Y.D.27		M2.14	M2.14	B1.14	B1.14
Y.D.5		M2.15	M2.15	B1.15	B1.15
Y.E.7		M3.0 (LSB)	M3.0 (LSB)	G1.0 (LSB)	G1.0 (LSB)
Y.E.8		M3.1	M3.1	G1.1	G1.1
Y.E.9		M3.2	M3.2	G1.2	G1.2
Y.E.12		M3.3	M3.3	G1.3	G1.3
Y.E.13		M3.4	M3.4	G1.4	G1.4
Y.E.14		M3.5	M3.5	G1.5	G1.5
Y.E.10		M3.6	M3.6	G1.6	G1.6
Y.E.11		M3.7	M3.7	G1.7	G1.7
Y.F.15		M3.8	M3.8	G1.8	G1.8
Y.F.18		M3.9	M3.9	G1.9	G1.9
Y.F.19		M3.10	M3.10	G1.10	G1.10
Y.F.20		M3.11	M3.11	G1.11	G1.11
Y.F.21		M3.12	M3.12	G1.12	G1.12
Y.F.22		M3.13	M3.13	G1.13	G1.13
Y.F.16		M3.14	M3.14	G1.14	G1.14
Y.F.17		M3.15	M3.15	G1.15	G1.15
Z.G.0			M4.0 (LSB)		I1.0 (LSB)
Z.G.1			M4.1		I1.1
Z.G.2			M4.2		I1.2
Z.G.3			M4.3		I1.3
Z.G.4			M4.4		I1.4
Z.G.6			M4.5		I1.5
Z.G.27			M4.6		I1.6
Z.G.5			M4.7		I1.7
Z.H.7			M4.8		I1.8
Z.H.8			M4.9		I1.9
Z.H.9			M4.10		I1.10
Z.H.12			M4.11		I1.11
Z.H.13			M4.12		I1.12
Z.H.14			M4.13		I1.13
Z.H.10			M4.14		I1.14
Z.H.11			M4.15		I1.15
Z.I.15					
Z.I.18					
Z.I.19					
Z.I.20					
Z.I.21					
Z.I.22					
Z.I.16					
Z.I.17					

4.10 16-Bit Mode, 80-bit

Table 4-8: 16-Bit Mode, 80-bit

Chip.Port.Signal	Mono 16-bit, 5-tap
X.V.24	LVAL
X.V.25	FVAL
Y.V.27	LVAL
Z.V.27	LVAL
X.A.0	M1.0 (LSB)
X.A.1	M1.1
X.A.2	M1.2
X.A.3	M1.3
X.A.4	M1.4
X.A.5	M1.5
X.A.6	M1.6
X.A.7	M1.7
X.B.8	M1.8
X.B.9	M1.9
X.B.10	M1.10
X.B.11	M1.11
X.B.12	M1.12
X.B.13	M1.13
X.B.14	M1.14
X.B.15	M1.15
X.C.16	M2.0 (LSB)
X.C.17	M2.1
X.C.18	M2.2
X.C.19	M2.3
X.C.20	M2.4
X.C.21	M2.5
X.C.22	M2.6
X.C.23	M2.7
X.D.26	M2.8
X.D.27	M2.9
Y.D.0	M2.10
Y.D.1	M2.11
Y.D.2	M2.12
Y.D.3	M2.13
Y.D.4	M2.14
Y.D.5	M2.15
Y.E.6	M3.0 (LSB)
Y.E.7	M3.1
Y.E.8	M3.2
Y.E.9	M3.3
Y.E.10	M3.4
Y.E.11	M3.5
Y.E.12	M3.6
Y.E.13	M3.7
Y.F.14	M3.8
Y.F.15	M3.9
Y.F.16	M3.10
Y.F.17	M3.11
Y.F.18	M3.12
Y.F.19	M3.13
Y.F.20	M3.14
Y.F.21	M3.15
Y.G.22	M4.0 (LSB)
Y.G.23	M4.1
Y.G.24	M4.2
Y.G.25	M4.3
Y.G.26	M4.4
Z.G.0	M4.5
Z.G.1	M4.6
Z.G.2	M4.7
Z.H.3	M4.8
Z.H.4	M4.9
Z.H.5	M4.10
Z.H.6	M4.11
Z.H.7	M4.12
Z.H.8	M4.13
Z.H.9	M4.14
Z.H.10	M4.15
Z.I.11	M5.0 (LSB)
Z.I.12	M5.1
Z.I.13	M5.2
Z.I.14	M5.3
Z.I.15	M5.4
Z.I.16	M5.5
Z.I.17	M5.6
Z.I.18	M5.7
Z.J.19	M5.8
Z.J.20	M5.9
Z.J.21	M5.10
Z.J.22	M5.11
Z.J.23	M5.12
Z.J.24	M5.13
Z.J.25	M5.14
Z.J.26	M5.15

4.11 Lite Modes

Table 4-9: Lite Modes

Chip.Port.Signal	8-bit	10-bit
X.V.24	LVAL	LVAL
X.V.25	FVAL	FVAL
X.V.26	DVAL	DVAL
X.V.22	SerTFG	SerTFG
X.A.0	M1.0 (LSB)	M1.0 (LSB)
X.A.1	M1.1	M1.1
X.A.2	M1.2	M1.2
X.A.3	M1.3	M1.3
X.A.4	M1.4	M1.4
X.A.6	M1.5	M1.5
X.A.20	M1.6	M1.6
X.A.21	M1.7	M1.7
X.B.7		M1.8
X.B.19		M1.9

5.0 Camera Link Connections

5.1 Camera Link Cable Pinout For Base, Medium, Full, 72 bit and 80 bit Configurations

Table 5-1 show the assignment of signals to pins for the different Camera Link configurations.

Table 5-1: MDR-26, HDR-26 and SDR-26 Connector Assignments

Cable Name	Base Configuration (with Camera Control and Serial Communications)			Medium, Full, 72 bit and 80 Bit Configurations		
	Camera Connector	Frame Grabber Connector	Channel Link Signal	Camera Connector	Frame Grabber Connector	Channel Link Signal
Inner Shield	1	1	inner shield	1	1	inner shield
Inner Shield	14	14	inner shield	14	14	inner shield
PAIR1-	2	25	X0-	2	25	Y0-
PAIR1+	15	12	X0+	15	12	Y0+
PAIR2-	3	24	X1-	3	24	Y1-
PAIR2+	16	11	X1+	16	11	Y1+
PAIR3-	4	23	X2-	4	23	Y2-
PAIR3+	17	10	X2+	17	10	Y2+
PAIR4-	5	22	Xclk-	5	22	Yclk-
PAIR4+	18	9	Xclk+	18	9	Yclk+
PAIR5-	6	21	X3-	6	21	Y3-
PAIR5+	19	8	X3+	19	8	Y3+
PAIR6+	7	20	SerTC+	7	20	100 Ω
PAIR6-	20	7	SerTC-	20	7	terminated
PAIR7-	8	19	SerTFG-	8	19	Z0-
PAIR7+	21	6	SerTFG+	21	6	Z0+
PAIR8-	9	18	CC1-	9	18	Z1-
PAIR8+	22	5	CC1+	22	5	Z1+
PAIR9+	10	17	CC2+	10	17	Z2-
PAIR9-	23	4	CC2-	23	4	Z2+
PAIR10-	11	16	CC3-	11	16	Zclk-
PAIR10+	24	3	CC3+	24	3	Zclk+
PAIR11+	12	15	CC4+	12	15	Z3-
PAIR11-	25	2	CC4-	25	2	Z3+
Inner Shield	13	13	inner shield	13	13	inner shield
Inner Shield	26	26	inner shield	26	26	inner shield

5.2 Shielding Recommendations

The outer shield of the cable is tied to the connector shell. It is recommended that the inner shell be tied to digital ground in cameras and tied through a resister to digital ground in the frame grabbers. It is recommended that a 0 Ω resistor be installed in the factory. If necessary, that

resistor can be removed in the field and replaced with a high-value resistor and parallel capacitor. Unused pairs should be terminated to 100 Ω at their respective ends of the cable.

Note: All pairs are individually shielded with aluminum foil. Pair shields are wrapped aluminum out and are in contact with four internal drains (digital ground). Outer braid and foil (chassis ground) are isolated from inner drains (digital ground).

6.0 Electrical Criteria

6.1 Chipset Criteria

Camera Link uses 28-bit Channel Link chips manufactured by Texas Instruments (formerly National Semiconductor). Because of potential interface issues, chips that use a similar technology, such as Flatlink by Texas Instruments and Panel Link by Silicon Image, may not be compatible with the Camera Link interface. Receivers and drivers with different operating frequencies will interoperate over the frequency range that both support. Table 6-1 lists some compatible Texas Instruments (formerly National Semiconductor) parts.

Table 6-1: Compatible Texas Instruments (formerly National Semiconductor) Parts

Product	Supply Voltage	Speed	Status
DS90CR285	3.3 V	66 MHz	Current Product
DS90CR286A	3.3 V	66 MHz	Current Product
DS90CR287	3.3 V	85 MHz	Current Product
DS90CR288A	3.3 V	85 MHz	Current Product
DS90CR281	5 V	40 MHz	Legacy
DS90CR282	5 V	40 MHz	Legacy
DS90CR283	5 V	66 MHz	Legacy
DS90CR284	5 V	66 MHz	Legacy
DS90CR286	3.3 V	66 MHz	Legacy
DS90CR288	3.3 V	75 MHz	Legacy

The pinout of the MDR 26 connector was chosen for optimal PWB trace routing using an LVDS driver/receiver pair for camera control signals. The following are the recommended Texas Instruments (formerly National Semiconductor) parts for the pair:

- Transmitter: DS90LV047, 3.3 V
- Receiver: DS90LV048, 3.3 V

6.2 Skew Budget for Channel Link Signals

The within-pair skew value on Channel Link data and clock pairs shall not exceed 50ps for both cameras and frame grabbers.

Additionally the pair-to-pair skew within each Channel Link data and clock group shall not exceed 50ps for both cameras and frame grabbers.

Note: Most Camera Link PCB-mount connectors are not skew-matched internally. Therefore, the individual trace lengths on the PCB may need to be adjusted so that the within-pair and/or pair-to-pair skew requirements are met.

Note: See sections 9.2.1.7 and 9.2.1.8 for skew requirements for Camera Link cables.

6.3 FPGA Channel Link Chip Emulation

The 1.0 to 2.0 versions of the specification required that all manufacturers of Camera Link devices shall use the Channel Link chip in order to be declared Camera Link compatible and use the CL logo and receive other benefits. The main reason for this restriction was to enforce interoperability between Camera Link devices. However, technology has moved rapidly ahead, and with advances in FPGAs, it has become possible to fully emulate the Channel Link chip inside of an FPGA. For this reason, starting with v2.1 of this specification, the requirement that a Camera Link device must use the Channel Link chip has been relaxed. Camera link devices that use a Channel Link emulation inside their FPGA will also be considered Camera Link compliant. However, in order to not weaken the specification by opening the door to custom emulations, v2.1 adds the requirement for all devices to pass an interoperability test at a AIA sponsored Plugfest.

7.0 Serial Communications API

A consistent, known API for asynchronous serial reading and writing allows camera vendors to write a frame grabber-independent, camera-specific configuration utility. The following API offers a solution for camera vendors that is easy for frame grabber manufacturers to implement, regardless of the actual implementation methods used for asynchronous serial communication.

This specification defines two APIs. Camera manufacturers use one API to create frame-grabber-independent camera configuration utilities. The other API provides the manufacturer-specific implementation of the serial communication functionality. Frame grabber manufacturers must provide this API.

7.1 Functionality

All camera control applications call into a single middleware DLL. The name of the DLL is always “clallserial.dll” no matter whether the DLL is built for Win32 or Win64 applications.

For 32-bit Windows "clallserial.dll" must be installed in %ProgramFiles%\CameraLink\Serial. This directory must be added to the PATH environment variable.

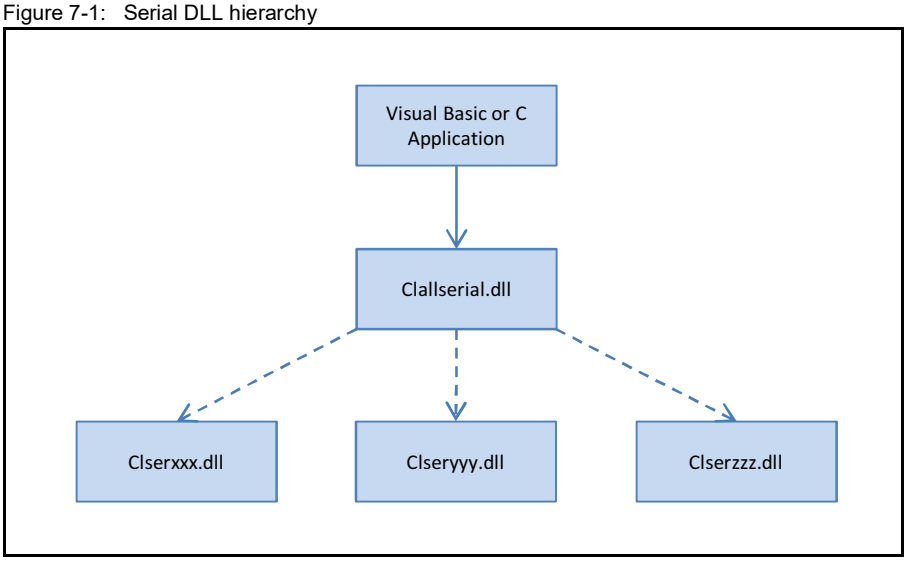
NOTE: Make sure that the directory is only added to the PATH once.

For 64-bit Windows the Win64 version of "clallserial.dll" should be in %ProgramFiles%\CameraLink\Serial, whereas the Win32 version should be in %ProgramFiles(x86)%\CameraLink\Serial. Both directories must be added to the PATH environment variable. This allows a 32 bit application to run on a 64 bit OS.

NOTE: Windows will make sure to load either the Win32 or the Win64 version of the DLL depending on the application being built for Win32 or Win64.

This DLL dynamically loads the DLL file(s) specific to the frame grabber(s) the application references. It then routes all calls to that DLL file. Figure 7-1 shows the hierarchy.

Figure 7-1: Serial DLL hierarchy



In order to simplify interfacing between applications and the serial DLLs, an import library is available for C/C++, and type library resource information is available in the DLL file for Visual Basic.

When “clallserial.dll” loads, it will search for the “clserxxx.dll” in a directory found via the following registry entries:

For 32-bit Windows the "clserxxx.dll" should be in the directory defined in the registry key: HKEY_LOCAL_MACHINE\software\cameralink. This key contains a value named “CLSERIALPATH” with type string (REG_SZ) which contains the actual path to the directory. The path should be: %ProgramFiles%\CameraLink\Serial. If the key/value already exist and point to a different location this location must be used.

For 64-bit Windows the Win64 version of "clserxxx.dll" should be in the directory defined in the registry key: HKEY_LOCAL_MACHINE\software\cameralink. This key contains a value named “CLSERIALPATH” with type string (REG_SZ) which contains the actual path to the directory. The path should be %ProgramFiles%\CameraLink\Serial. If the key/value already exist and point to a different location this location must be used. You must not change any existing value.

For 64-bit Windows the Win32 version of "clserxxx.dll" should be in the directory defined in the registry key: HKEY_LOCAL_MACHINE\software\Wow6432Node\cameralink.

NOTE: “clallserial.dll” always uses HKEY_LOCAL_MACHINE\software\cameralink to retrieve the “clserxxx.dll”. The Windows Registry Redirector makes sure that the application sees only one of the two registry entries depending on the application being built for Win32 or Win64.

This key contains a value named “CLSERIALPATH” with type string (REG_SZ) which contains the actual path to the directory. The path should be %ProgramFiles(x86)%\CameraLink\Serial. If the key/value already exist and point to a different location this location must be used. You must not change any existing value.

If the keys/values/directories do not exist they must be created. See Section 7.1.2 for details.

After locating the files, “clallserial.dll” dynamically loads and queries each one for the manufacturer name and port names. It returns a complete system-wide list of Camera Link serial ports to the application. The required manufacturer-specific DLL files are loaded, and “clallserial.dll” manages passing the application calls to the appropriate DLL for the port specified by the application.

All camera and frame grabber manufacturers are free to distribute “clallserial.dll”.

7.1.1 Features

The following are features of the current Camera Link standard for serial communication:

- Simultaneous, multi-port (including cross vendor) access
- Support for binary or text-based data transfers
- Common API across vendors
- Common error codes across vendors
- Common error text across vendors
- Strict, well-defined behavior of all functions in specification

- Openness to vendor-specific error codes and text
- Ability to enumerate ports on system
- Inquireable/adjustable baud rate for ports
- Win32 and Win64 support (open source for port to other platforms)
- C/C++ support through import library
- VisualBasic support through type library
- Backward compatibility with October 2000 Camera Link specification
- Standard default communication settings for serial port
- Thread safety

7.1.2 Requirements and Recommendations

This section outlines requirements and recommendations for frame grabber companies and camera companies.

7.1.2.1 Frame Grabber Companies

In order to comply with the Camera Link standard, frame grabbers companies must fulfill the following requirements:

- Provide “clserxxx.dll” to implement all functions listed in Table 7-4.
- Ensure that “clserxxx.dll” is thread safe.
- Frame grabber driver installer should install to the directory specified by the keys specified in Section 7.1.
- On 32 bit operating systems only install "clserxxx.dll".
- On 64 bit operating systems install the Win64 version of the "clserxxx.dll". If the underlying frame grabber hardware supports running a 32 bit application on a 64 bit operating system, then also install the Win32 version of the "clserxxx.dll".

The following are recommendations for frame grabber companies:

- Serial port should be accessible by one process while another process controls the acquisition portion of the frame grabber.
- Any configuration capture utility developed for a Camera Link board should leave the serial port available for a camera control utility to access.

7.1.2.2 Camera Companies

The following are recommendations for camera companies:

- Camera control utilities should be refactored to take advantage of the API defined in Table 7-3 and Table 7-4.
- Camera control utility should release the port by calling `clSerialClose` when the port is not in use.

7.2 C Interface to “clallserial.dll”

An import library, “clallserial.lib”, and header file, “clallserial.h”, for “clallserial.dll” provides the functions shown in Table 7-1 and Table 7-2 which can be called from a C/C++ program.

Table 7-1: Serial interface specification

Name	Prototype
clFlushPort	INT32 __stdcall clFlushPort (hSerRef serialRef)
clGetErrorText	INT32 __stdcall clGetErrorText (const INT8* manuName, INT32 errorCode, INT8* errorText, UINT32* errorTextSize)
clGetNumPorts	INT32 __stdcall clGetNumPorts (UINT32* numPorts)
clGetNumBytesAvail	INT32 __stdcall clGetNumBytesAvail (hSerRef serialRef, UINT32* numBytes)
clGetPortInfo	INT32 __stdcall clGetPortInfo (UINT32 serialIndex, INT8* manufacturerName, UINT32* nameBytes, INT8* portID, UINT32* IDBytes, UINT32* version)
clGetSupportedBaudRates	INT32 __stdcall clGetSupportedBaudRates (hSerRef serialRef, UINT32* baudRates)
clSerialClose	void __stdcall clSerialClose (hSerRef serialRef)
clSerialInit	INT32 __stdcall clSerialInit (UINT32 serialIndex, hSerRef* serialRefPtr)
clSerialRead	INT32 __stdcall clSerialRead (hSerRef serialRef, INT8* buffer, UINT32* numBytes, UINT32 serialTimeout)
clSerialWrite	INT32 __stdcall clSerialWrite (hSerRef serialRef, INT8* buffer, UINT32* bufferSize, UINT32 serialTimeout)
clSetBaudRate	INT32 __stdcall clSetBaudRate (hSerRef serialRef, UINT32 baudRate)

Datatype definitions on Windows operating systems are shown in Figure 7-2

Table 7-2: Type definitions

Defined Data Type	Win 32 Type
hSerRef	void*
INT32	Int
UINT32	unsigned int
INT8	Char

7.3 Visual Basic Interface to “clallserial.dll”

A Visual Basic type library provides the functions in Table 7-3 for Visual Basic applications.

Table 7-3: Visual Basic Interface

Name	Prototype
clFlushPort	clFlushPort (serialReference As Long) As Long
clGetErrorText	clGetErrorText (manuName As String, errorCode As Long, errorText As String, errorTextSize As Long) As Long
clGetNumBytesAvail	clGetNumBytesAvail (serialReference As Long, numBytes As Long) As Long
clGetNumPorts	clGetNumPorts (numPorts As Long) As Long
clGetPortInfo	clGetPortInfo (serialIndex As Long, manufacturerName As String, nameBytes As Long, portID As String, IDBytes As Long, version As Long) As Long
clGetSupportedBaudRates	clGetSupportedBaudRates(serialRef As Long, baudRates As Long) As Long
clSerialClose	clSerialClose(serialReference As Long) As Any
clSerialInit	clSerialInit(serialIndex As Long, serialReference As Long) As Long
clSerialRead - Deprecated	clSerialRead(serialReference As Long, readBuffer As String, numBytes As Long, serialTimeout As Long) As Long
clSerialReadEx	clSerialReadEx(hSerRef serialRef, INT8* buffer, UINT32* numBytes UINT32 serialTimeout)
clSerialWrite	clSerialWrite(serialReference As Long, writeBuffer As String, bufferSize As Long, serialTimeout As Long) As Long
clSetBaudRate	clSetBaudRate(serialRef As Long, baudRate As Long) As Long

7.4 The Manufacturer DLL “clserxxx.dll”

Table 7-4 outlines the functions a frame-grabber-specific manufacturer DLL should provide according to the listed prototypes and calling conventions.

Table 7-4: “clserxxx.dll”

Name	Prototype
clFlushPort	INT32 __cdecl clFlushPort (hSerRef serialRef)
clGetErrorText	INT32 __cdecl clGetErrorText (INT32 errorCode, INT8* errorText, UINT32* errorTextSize)
clGetManufacturerInfo	INT32 __cdecl clGetManufacturerInfo INT8* ManufacturerName, UINT32* bufferSize, UINT32* version)
clGetNumBytesAvail	INT32 __cdecl clGetNumBytesAvail (hSerRef serialRef, UINT32* numBytes)
clGetNumSerialPorts	INT32 __cdecl clGetNumSerialPorts (UINT32* numSerialPorts)
clGetSerialPortIdentifier	INT32 __cdecl clGetSerialPortIdentifier (UINT32 serialIndex, INT8* portID, UINT32* bufferSize)
clGetSupportedBaudRates	INT32 __cdecl clGetSupportedBaudRates (hSerRef serialRef, UINT32* baudRates)
clSerialClose	void __cdecl clSerialClose (hSerRef serialRef)
clSerialInit	INT32 __cdecl clSerialInit (UINT32 serialIndex, hSerRef* serialRefPtr)

Table 7-4: “clserxxx.dll” (Continued)

Name	Prototype
clSerialRead - Depreciated	INT32 __cdecl clSerialRead (hSerRef serialRef, INT8* buffer, UINT32* numBytes, UINT32 serialTimeout)
clSerialReadEx	clSerialReadEx(hSerRef serialRef, INT8* buffer, UINT32* numBytes UINT32 serialTimeout)
clSerialWrite	INT32 __cdecl clSerialWrite (hSerRef serialRef, INT8* buffer, UINT32* bufferSize, UINT32 serialTimeout)
clSetBaudRate	INT32 __cdecl clSetBaudRate (hSerRef serialRef, UINT32 baudRate)

8.0 Serial Communication API Function Reference

This chapter is a provides a detailed listing of each serial API function and its associated parameters and return values.

8.1 clFlushPort

Format

```
INT32 clFlushPort (hSerRef serialRef)
```

Purpose

This function discards any bytes that are available in the input buffer. This function is required for `clserxxx.dll` and is available from `clallserial.dll`.

Parameters

Name	Direction	Description
serialRef	input	The value obtained by the `clSerialInit` function that describes the port to be flushed.

Return Value

At completion, this function returns one of the following status codes:

CL_ERR_NO_ERR
CL_ERR_INVALID_REFERENCE

Refer to Table 8-1 for more information on status codes.

8.2 clGetErrorText

Format

```
INT32 clGetErrorText (const INT8* manuName, INT32 errorCode, INT8* errorText, UINT32*
                      errorTextSize)
```

Purpose

This function converts an error code to error text for display in a dialog box or in a standard I/O window. This function is required for `clserxxx.dll` and is available from `clallserial.dll`.

`NOTE: clGetErrorText` first looks for the error code in `clallserial.dll`. If the error code is not found in `clallserial.dll`, it is not a standard Camera Link error. `clGetErrorText` then passes the error code to the manufacturer-specific DLL, which returns the manufacturer-specific error text.

Parameters

Name	Direction	Description
manufacturerName	input	The manufacturer name in a NULL-terminated buffer. Manufacturer name is returned from `clGetPortInfo`.
errorCode	input	The error code used to find the appropriate error text. An error code is returned by every function in this library.
errorText	output	A caller-allocated buffer which contains the NULL-terminated error text on function return.
errorTextSize	input/output	On success, contains the number of bytes written into the buffer, including the NULL-termination character. This value should be the size in bytes of the error text buffer passed in. On CL_ERR_BUFFER_TOO_SMALL, contains the size of the buffer needed to write the error text.

Return Value

On completion, this function returns one of the following status codes:

CL_ERR_NO_ERR
CL_ERR_MANU_DOES_NOT_EXIST
CL_ERR_BUFFER_TOO_SMALL
CL_ERR_ERROR_NOT_FOUND

Refer to Table 8-1 for more information on status codes.

8.3 clGetManufacturerInfo

Format

```
INT32 clGetManufacturerInfo (INT8* manufacturerName; UINT32* bufferSize UINT32*
                             version);
```

Purpose

This function returns the name of the frame grabber manufacturer who created the DLL and the version of the Camera Link specifications with which the DLL complies. This function is required for `clser`*`xxx`*`.dll`.

Parameters

Name	Direction	Description
manufacturerName	output	A pointer to a user-allocated buffer into which the function copies the manufacturer name. The returned name is NULL-terminated.
bufferSize	input/output	As an input, this value should be the size of the buffer that is passed. On successful return, this parameter contains the number of bytes written into the buffer, including the NULL termination character. On CL_ERR_BUFFER_TOO_SMALL, this parameter contains the size of the buffer needed to write the data text.
version	output	A constant stating the version of the Camera Link specifications with which this DLL complies. See Table B-4

Return Value

At completion, this function returns one of the following status codes:

CL_ERR_NO_ERR
CL_ERR_FUNCTION_NOT_FOUND
CL_ERR_BUFFER_TOO_SMALL

Refer to Table 8-1 for more information on status codes.

8.4 clGetNumBytesAvail

Format

```
INT32 clGetNumBytesAvail (hSerRef serialRef, UINT32* numBytes)
```

Purpose

This function outputs the number of bytes that are received at the port specified by serialRef but are not yet read out. This function is required for `clserxxx.dll` and is available from `clallserial.dll`.

Parameters

Name	Direction	Description
serialRef	input	The value obtained by the `clSerialInit` function.
numBytes	output	The number of bytes currently available to be read from the port.

Return Value

At completion, this function returns one of the following status codes:

CL_ERR_NO_ERR
CL_ERR_INVALID_REFERENCE

Refer to Table 8-1 for more information on status codes.

8.5 clGetNumSerialPorts

Format

```
INT32 clGetNumSerialPorts (UINT32* numSerialPorts)
```

Purpose

This function returns the number of serial ports in your system from a specific manufacturer. This function is required for `clser`*`xxx`*`.dll`.

Parameters

Name	Direction	Description
numSerialPorts	output	The number of serial ports in your system that you can access with the current DLL.

Return Value

At completion, this function returns the following status code:

CL_ERR_NO_ERR

Refer to Table 8-1 for more information on status codes.

8.6 clGetNumPorts

Format

```
INT32 clGetNumPorts (UINT32* numPorts)
```

Purpose

This function returns the total number of Camera Link serial ports in your system. This function is available from `clallserial.dll`.

Parameters

Name	Direction	Description
numPorts	output	The number of Camera Link serial ports in your system.

Return Value

On completion, this function returns the following status code:

CL_ERR_NO_ERR

Refer to Table 8-1 for more information on status codes.

8.7 clGetPortInfo

Format

```
INT32 clGetPortInfo (UINT32 serialIndex, INT8* manufacturerName, UINT32* nameBytes,
                     INT8* portID, UINT32* IDBytes, UINT32* version)
```

Purpose

This function provides information about the port specified by the index. This function is available from `clallserial.dll`.

Parameters

Name	Direction	Description
index	input	The index of the port for which you want information. The valid range for this index is 0 to (n–1) where n is the value of numPorts returned by `clGetNumPorts`.
manufacturerName	output	Pointer to a user-allocated buffer into which the function copies the manufacturer name. The returned name is NULL-terminated. In the case that the DLL conforms to the October 2000 specification, this parameter will contain the file name of the DLL rather than the manufacturer name.
nameBytes	input/output	As an input, this value should be the size of the buffer that is passed. On successful return, this parameter contains the number of bytes written into the buffer, including the NULL termination character. On CL_ERR_BUFFER_TOO_SMALL, this parameter contains the size of the buffer needed to write the data text.
portID	output	A manufacturer-specific identifier for the serial port. In the case that the manufacturer DLL conforms to the October 2000 specification, on return this parameter will be Port *n*, where *n* is a unique index for the port.
IDBytes	input/output	As an input, this value should be the size of the buffer that is passed. On successful return, this parameter contains the number of bytes written into the buffer, including the NULL-termination character. On CL_ERR_BUFFER_TOO_SMALL, this parameter contains the size of the buffer needed to write the data text.
version	output	The version of the Camera Link specifications with which this frame grabber software complies.

Return Value

On completion, this function returns the following status codes:

CL_ERR_NO_ERR
CL_ERR_BUFFER_TOO_SMALL
CL_ERR_INVALID_INDEX

Refer to Table 8-1 for more information on status codes.

8.8 clGetSerialPortIdentifier

Format

```
INT32 clGetSerialPortIdentifier (UINT32 serialIndex, INT8* portID,
                          UINT32* bufferSize) ;
```

Purpose

This function returns a manufacturer-specific identifier for each serial port in your system. This function is required for `clser`*`xxx`*`.dll`.

Parameters

Name	Direction	Description
serialIndex	input	A zero-based index value. The valid range for serialIndex is 0 to (n–1), where n is the value of numSerialPorts, as returned by `clGetNumSerialPorts`.
portID	output	Manufacturer-specific identifier for the serial port
bufferSize	input/output	As an input, this value should be the size of the buffer that is passed. On successful return, this parameter contains the number of bytes written into the buffer, including the NULL termination character. On CL_ERR_BUFFER_TOO_SMALL, this parameter contains the size of the buffer needed to write the data text.

Return Value

At completion, this function returns one of the following status codes:

CL_ERR_NO_ERR
CL_ERR_BUFFER_TOO_SMALL
CL_ERR_INVALID_INDEX

Refer to Table 8-1 for more information on status codes.

8.9 clGetSupportedBaudRates

Format

```
INT32 clGetSupportedBaudRates (hSerRef serialRef, UINT32* baudRates) ;
```

Purpose

This function returns the valid baud rates of the current interface. This function is required for `clserxxx.dll` and is available from `clallserial.dll`.

Parameters

Name	Direction	Description
serialRefPtr	input	The value obtained from the `clSerialInit` function, which describes the port being queried for baud rates.
baudRates	output	Bitfield that describes all supported baud rates of the serial port as described by serialRefPtr. Refer to Table 8-2

Return Value

At completion, this function returns one of the following status codes:

CL_ERR_NO_ERR
CL_ERR_INVALID_REFERENCE
CL_ERR_FUNCTION_NOT_FOUND

Refer to Table 8-1 for more information on status codes.

8.10 clSerialClose

Format

```
void clSerialClose (hSerRef serialRef)
```

Purpose

This function closes the serial device and cleans up the resources associated with **serialRef**. Upon return, **serialRef** is no longer usable. This function is required for `clserxxx.dll` and is available from `clallserial.dll`.

Parameters

Name	Direction	Description
serialRef	input	The value obtained from the `clSerialInit` function for clean-up.

8.11 clSerialInit

Format

```
INT32 clSerialInit(UINT32 serialIndex, hSerRef* serialRefPtr)
```

Purpose

This function initializes the device referred to by **serialIndex** and returns a pointer to an internal serial reference structure. This function is required for `clserxxx.dll` and is available from `clallserial.dll`.

Parameters

Name	Direction	Description
serialIndex	input	A zero-based index value. For *n* serial devices in the system supported by this library, serialIndex has a range of 0 to (*n*–1).
serialRefPtr	output	On a successful call, points to a value that contains a pointer to the vendor-specific reference to the current session.

Return Value

On completion, this function returns one of the following status codes:

CL_ERR_NO_ERR
CL_ERR_PORT_IN_USE
CL_ERR_INVALID_INDEX

Refer to Table 8-1 for more information on status codes.

8.12 clSerialRead - *Deprecated*

Note: this function has been deprecated and will not be available in Camera Link v3.0. Use the new function clSerialReadEx instead.

Format

```
INT32 clSerialRead(hSerRef serialRef, INT8* buffer, UINT32* numBytes
                           UINT32 serialTimeout)
```

Purpose

This function reads **numBytes** from the serial device referred to by **serialRef**. This function is required for `clserxxx.dll` and is available from `clallserial.dll`.

clSerialRead will return when **numBytes** are available at the serial port or when the **serialTimeout** period has passed. Upon success, **numBytes** are copied into **buffer**. In the case of any error, including CL_ERR_TIMEOUT, no data is copied into **buffer**.

Note: the parameter numBytes represent the number of byte the caller wants to read from the camera. It does not represent the size of the incoming buffer. If numBytes is bigger than the expect message from the camera, this function till time out. If the size of the message being returned from the camera is unknown, then the best solution is to call this function repeatedly until the message is completely read.

Parameters

Name	Direction	Description
serialRef	input	The value obtained from the `clSerialInit` function.
buffer	output	Points to a user-allocated buffer. Upon a successful call, buffer contains the data read from the serial device. Upon failure, this buffer is not affected. Caller should ensure that buffer is at least numBytes in size.
numBytes	input	The number of bytes requested by the caller.
serialTimeout	input	Indicates the timeout in milliseconds.

Return Value

On completion, this function returns one of the following status codes:

CL_ERR_NO_ERR
CL_ERR_TIMEOUT
CL_ERR_INVALID_REFERENCE

Refer to Table 8-1 for more information on status codes.

8.13 clSerialReadEx

Format

```
INT32 clSerialReadEx(hSerRef serialRef, INT8* buffer, UINT32* numBytes
                          UINT32 serialTimeout)
```

Purpose

This function reads **numBytes** from the serial device referred to by **serialRef**. This function is required for `clserxxx.dll` and is available from `clallserial.dll`.

This function will return when either of the following occur:

numBytes bytes have been received from the device (function returns CL_ERR_NO_ERR)

serialTimeout milliseconds has expired, this is not considered an error condition (function returns CL_ERR_TIMEOUT, which is not an error condition).

When either of these conditions occur, all the bytes received (up to **numBytes)** are copied into **buffer** and **numBytes** will contain the number of bytes read.

In the case of CL_ERR_INVALID_REFERENCE error, no data is copied into **buffer**.

NOTE: this function replaces `clSerialRead`

`clSerialReadEx` differs from `clSerialRead` in the following ways:

1. A timeout in `clSerialReadEx` is not considered an error condition. When a timeout occurs, the function simply returns as many bytes as have been received thus far. A timeout in `clSerialRead` is considered an error, and the **buffer** is returned empty.

2. Both functions return CL_ERR_TIMEOUT when a timeout occurs. However, when it occurs in `clSerialReadEx`, the value does not denote an error condition. With `clSerialRead`, this is considered an error condition.

3.The parameter **numBytes** of `clSerialReadEx` is both an input and an output. As an input it is the size of the **buffer** in bytes, as an output it returns the number of bytes actually read. In `clSerialRead`, **numBytes** is only an input and it contains the number of bytes the function should read before returning.

NOTE: Users of `clSerialReadEx` must first test to see if the serial DLL is version 2.1 compliant. This is done by calling `clGetManufacturerInfo` from `clserxxx.dll` or `clGetPortInfo` from `clallserial.dll` and checking the **version** parameter. If the **version** parameter is not 2.1 or later, then this function cannot be used, and `clSerialRead` must be used.

NOTE: A common way to use this function is to set **serialTimeout** equal to zero. In this case, the function will return immediately with any bytes that have already been received. If no bytes have been received, the function will simply return CL_ERR_TIMEOUT right away with **numBytes** equal to 0.

NOTE: If a timeout condition occurs before all of the received bytes can be copied into the buffer, the function should return CL_ERR_TIMEOUT and **buffer** should contain all the bytes that have been copied before the timeout occurred. A subsequent call should not return any bytes returned in the previously returned, it should only return bytes that have not yet been copied into the buffer.

Parameters

Name	Direction	Description
serialRef	input	The value obtained from the `clSerialInit` function.
buffer	output	Points to a user-allocated buffer. Upon a successful call, buffer contains the data read from the serial device.
numBytes	input/output	The size of the buffer in bytes. Upon a successful call contains the number of bytes read from the device.
serialTimeout	input	Indicates the timeout in milliseconds.This parameter can be set to 0.

Return Value

On completion, this function returns one of the following status codes:

CL_ERR_NO_ERR
CL_ERR_TIMEOUT
CL_ERR_INVALID_REFERENCE

Refer to Table 8-1 for more information on status codes.

8.14 clSerialWrite

Format

```
INT32 clSerialWrite(hSerRef serialRef, INT8* buffer, UINT32* bufferSize
                          UINT32 serialTimeout)
```

Purpose

This function writes the data in the buffer to the serial device referenced by **serialRef**. This function is required for `clser`*`xxx`*`.dll` and is available from `clallserial.dll`.

Note: This function is blocking, it will not return until bufferSize bytes have been successfully written to the device, or if the timeout has expired.

Parameters

Name	Direction	Description
serialRef	input	The value obtained from the `clSerialInit` function.
buffer	input	Contains data to write to the serial port.
bufferSize	input/output	Contains the buffer size indicating the maximum number of bytes to be written. Upon a successful call, bufferSize contains the number of bytes written to the serial device.
serialTimeout	input	Indicates the timeout in milliseconds.

Return Value

On completion, this function returns one of the following status codes

CL_ERR_NO_ERR
CL_ERR_INVALID_REFERENCE
CL_ERR_TIMEOUT

Refer to Table 8-1 for more information on status codes.

8.15 clSetBaudRate

Format

```
INT32 clSetBaudRate (hSerRef serialRef, UINT32 baudRate)
```

Purpose

This function sets the baud rate for the serial port of the selected device. Use `clGetSupportedBaudRate` to determine supported baud rates. This function is required for `clser`*`xxx`*`.dll` and is available from `clallserial.dll`.

Parameters

Name	Direction	Description
serialRefPtr	input	The value obtained from the `clSerialInit` function.
baudRate	input	The baud rate you want to use. This parameter expects the values represented by the CL_BAUDRATE constants in Table B-4

Return Value

On completion, this function returns one of the following status codes:

CL_ERR_NO_ERR
CL_ERR_INVALID_REFERENCE
CL_ERR_BAUD_RATE_NOT_SUPPORTED

Refer to Table 8-1 for more information on status codes.

8.16 Status Codes

Each Camera Link function returns a status code that indicates whether the function was performed successfully. Table 8-1 summarizes the Camera Link error codes.

Table 8-1: Camera Link Error Codes

Error Code	Error Constant	Error Text
0	CL_ERR_NO_ERR	Function returned successfully.
-10001	CL_ERR_BUFFER_TOO_SMALL	User buffer not large enough to hold data.
-10002	CL_ERR_MANU_DOES_NOT_EXIST	The requested manufacturer's DLL does not exist on your system.
-10003	CL_ERR_PORT_IN_USE	Port is valid but cannot be opened because it is in use.
-10004	CL_ERR_TIMEOUT	Operation not completed within specified timeout period.
-10005	CL_ERR_INVALID_INDEX	Not a valid index.
-10006	CL_ERR_INVALID_REFERENCE	The serial reference is not valid.
-10007	CL_ERR_ERROR_NOT_FOUND	Could not find the error description for this error code.
-10008	CL_ERR_BAUD_RATE_NOT_SUPPORTED	Requested baud rate not supported by this interface.
-10009	CL_ERR_OUT_OF_MEMORY	System is out of memory and could not perform required actions.
-10098	CL_ERR_UNABLE_TO_LOAD_DLL	The DLL was unable to load due to a lack of memory or because it does not export all required functions.
-10099	CL_ERR_FUNCTION_NOT_FOUND	Function does not exist in the manufacturer's library.

8.17 Constants

Constants help clearly define specific function parameter values. These constants are included in your `clallserial.h` header file. Table 8-2 defines the Camera Link constants.

Table 8-2: Camera Link Constants

Constant	Definition
CL_DLL_VERSION_NO_VERSION	This library is not a valid Camera Link library; value = 1
CL_DLL_VERSION_1_0	This Camera Link library conforms to the October 2000 version of the Camera Link Specifications; value = 2
CL_DLL_VERSION_1_1	This Camera Link library conforms to the November 2002 version of the Camera Link Specifications; value = 3
CL_DLL_VERSION_2_0	This Camera Link library conforms to the February 2012 version of the Camera Link Specifications; value = 4
CL_DLL_VERSION_2_1	This Camera Link library conforms to the April 2018 version of the Camera Link Specifications; value = 5
CL_BAUDRATE_9600	Baud Rate = 9600; value = 1
CL_BAUDRATE_19200	Baud Rate = 19200; value = 2
CL_BAUDRATE_38400	Baud Rate = 38400; value = 4
CL_BAUDRATE_57600	Baud Rate = 57600; value = 8
CL_BAUDRATE_115200	Baud Rate = 115200; value = 16
CL_BAUDRATE_230400	Baud Rate = 230400; value = 32
CL_BAUDRATE_460800	Baud Rate = 460800; value = 64
CL_BAUDRATE_921600	Baud Rate = 921600; value = 128

9.0 Mechanical Interface and Cable Requirements

9.1 Mechanical Interface

9.1.1 Overview

This section describes the Camera Link connector and cable interface required on the camera and frame grabber. General dimensions, tolerances and descriptions of those features which affect the intermateability of the receptacle and plug connectors are described in this section. The pin outs for the receptacle connector are also described in this section.

9.1.2 Camera Link Connectors

Three connectors have been approved for use in Camera Link. The first two are the standard 1.27 mm (.050") pitch Camera Link connector and the smaller 0.80 mm (.031") pitch miniature Camera Link (MiniCL) connector. Both of these connectors have 360 degree "delta" shaped metal shells that enclose the plug and receptacle contacts to provide shielding and proper polarity when mated. The third connector is the PoCL-Lite connector. The contacts are designed to handle limited power, ground and signals. The connectors are as described in the following paragraphs.

9.1.2.1 Contact Finish

The contacts of the connector receptacles of the camera and cable assembly shall be plated with a noble metal or noble metal alloy that meets the following minimum requirements: 0.76 μm gold over 2.0 μm nickel.

9.1.2.2 Camera Link (CL) Connector

The Camera Link connector shall be a 26-position two-row shielded mini-delta ribbon connector with contacts on 1.27 mm (.050") spacing. The approved Camera Link connector is the 3M™ Mini Delta Ribbon (MDR) connector available from 3M Company. Table 9-1 shows the applicable part numbers.

Table 9-1: Part numbers for compatible Camera Link connectors.

Part Number	Description
3M™ MDR 10126 Series	26-Position Plugs
3M™ MDR 10226 Series	26-Position Receptacles
3M™ MDR 10326 Series	26-Position Junction Shells

9.1.2.3 Miniature Camera Link (MiniCL) Connector

The miniature Camera Link (MiniCL) connector shall be a 26-position two row shielded subminiature delta ribbon connector with contacts on 0.80 mm (.031") spacing. The approved MiniCL connectors are the 3M™ Shrunk Delta Ribbon (SDR) connector available from 3M

Company and the HDR Series connector available from Honda Connectors, Inc. Table 9-2 shows the applicable part numbers.

Table 9-2: Part numbers for compatible Miniature Camera Link connectors.

Part Number	Description
3M™ SDR 12126 Series	26-Position Plugs
3M™ SDR 12226 Series	26-Position Receptacles
Honda Connectors, Inc. HDR-E26M Series	26-Position Plugs
Honda Connectors, Inc. HDR-Ex26xF Series	26-Position Receptacles
Honda Connectors, Inc. HDR-E26 Series	26-Position Junction Shells

9.1.2.4 Power over Camera Link Lite (PoCL-Lite) Connector

The PoCL-Lite connector shall be a 14-position two row shielded subminiature delta ribbon connector with contacts on 0.80 mm (.031”) spacing. In addition, PoCL-Lite configurations may use a 26-position Miniature Camera Link connector listed in paragraph 1.2.3. PoCL-Lite configurations shall use a14-position SDR Connector on the camera side or frame grabber side when using a 26-position Miniature Camera Link connector. The approved PoCL-Lite configuration connectors are the SDR Shrunk Delta Ribbon connector available from 3M Company and the HDR Series connector available from Honda Connectors. Table 9-3 shows the applicable part numbers.

Table 9-3: Part numbers for compatible Camera Link Lite connectors.

Part Number	Description
3M™ SDR 12114 Series	14-Position Plugs
3M™ SDR 12214 Series	14-Position Receptacles
Honda Connectors, Inc. HDR-E14M Series	14-Position Plugs
Honda Connectors, Inc. HDR-Ex14xF Series	14-Position Receptacles
Honda Connectors, Inc. HDR-E14 Series	14-Position Junction Shells

9.1.2.5 Connector Pin Assignment for Base, Medium, Full, 72 Bit and 80 Bit Configuration Camera Link

The assignment of signals to the connector pins shall be as shown in Table 9-4. There is no difference between the camera end of the cable and that of the frame grabber. Thus, either end of the cable may be connected to the camera or frame grabber.

Table 9-4: Camera Link Cable Assembly Wiring Diagram - MDR-26, HDR-26 and SDR-26

Connector Pin Assignment		Conductor Description	
P1	**P2**	**Standard**	**PoCL**
1	1	Bare wire (Inner shield)	Insulated Wire (Power)
14	14	Bare wire (Inner shield)	Bare wire (Power return)
2	25	Pair 1-	Pair 1-
15	12	Pair 1+	Pair 1+
3	24	Pair 2-	Pair 2-
16	11	Pair 2+	Pair 2+
4	23	Pair 3-	Pair 3-
17	10	Pair 3+	Pair 3+
5	22	Pair 4-	Pair 4-
18	9	Pair 4+	Pair 4+
6	21	Pair 5-	Pair 5-
19	8	Pair 5+	Pair 5+
7	20	Pair 6+	Pair 6+
20	7	Pair 6-	Pair 6-
8	19	Pair 7-	Pair 7-
21	6	Pair 7+	Pair 7+
9	18	Pair 8-	Pair 8-
22	5	Pair 8+	Pair 8+
10	17	Pair 9+	Pair 9+
23	4	Pair 9-	Pair 9-
11	16	Pair 10-	Pair 10-
24	3	Pair 10+	Pair 10+
12	15	Pair 11+	Pair 11+
25	2	Pair 11-	Pair 11-
13	13	Bare wire (Inner shield)	Bare wire (Power return)
26	26	Bare wire (Inner shield)	Insulated Wire (Power)

NOTE: Pin Assignment is for Shielded Twisted Pair Cabling.

NOTE: The function of each of these conductors is given in Table 5-1 on page 27.

9.1.2.6 Connector Pin Assignment for PoCL-Lite Configuration

The assignment of signals to the connector pins shall be as shown in Table 9-5 through Table 9-7. There is no difference between the camera end of the cable and that of the frame grabber. Thus, either end of the cable may be connected to the camera or frame grabber. PoCL-Lite configurations shall use a 14-position SDR Connector on at least one end of the cable.

NOTE: Pin Assignments are for Shielded Twisted Pair Cabling in Table 9-5 through Table 9-7

Table 9-5: **PoCL-Lite Cable Assembly Wiring Diagram (14p to 14p configuration)**

Connector Pin Assignment		**Conductor Description**	
Camera Connector	**Frame Grabber Connector**	**Channel Link Signal**	**Cable Name**
1	1	Power	Power
8	8	Inner Shield	Inner Shield
2	9	SerTC+	Pair1+
9	2	SerTC-	Pair1-
3	12	X0-	Pair2-
10	5	X0+	Pair2+
4	11	X2-	Pair3-
11	4	X2+	Pair3+
5	10	Xclk-	Pair4-
12	3	Xclk+	Pair4+
6	13	CC-	Pair5-
13	6	CC+	Pair5+
7	7	Inner Shield	Inner Shield
14	14	Power	Power

Table 9-6: **PoCL-Lite Cable Assembly Wiring Diagram (14p to 26p configuration)**

Connector Pin Assignment		**Conductor Description**	
Camera Connector (14p)	**Frame Grabber Connector (26p)**	**Channel Link Signal**	**Cable Name**
1	1	Power	Power
8	14	Inner Shield	Inner Shield
2	20	SerTC+	Pair1+
9	7	SerTC-	Pair1-
3	25	X0-	Pair2-
10	12	X0+	Pair2+
4	23	X2-	Pair3-
11	10	X2+	Pair3+
5	22	Xclk-	Pair4-
12	9	Xclk+	Pair4+
6	18	CC-	Pair5-
13	5	CC+	Pair5+
7	13	Inner Shield	Inner Shield
14	26	Power	Power

Table 9-7: PoCL-Lite Cable Assembly Wiring Diagram (26p to 14p configuration)

Connector Pin Assignment		**Conductor Description**	
Camera Connector (26p)	**Frame Grabber Connector (14p)**	**Channel Link Signal**	**Cable Name**
1	1	Power	Power
14	8	Inner Shield	Inner Shield
7	9	SerTC+	Pair1+
20	2	SerTC-	Pair1-
2	12	X0-	Pair2-
15	5	X0+	Pair2+
4	11	X2-	Pair3-
17	4	X2+	Pair3+
5	10	Xclk-	Pair4-
18	3	Xclk+	Pair4+
9	13	CC-	Pair5-
22	6	CC+	Pair5+
13	7	Inner Shield	Inner Shield
26	14	Power	Power

9.1.2.7 Mechanical Drawings

This section depicts the dimensions and mechanical outline of the cable assembly and connector receptacles on the camera and frame grabber. Typical cable assemblies are shown in Figure 9-1 through Figure 9-6. Typical board mount receptacles and panel cutouts for the camera and frame grabber are shown in Figure 9-7 through Figure 9-9. These figures are for illustrative purposes only.

Figure 9-1: Camera Link Cable Assembly

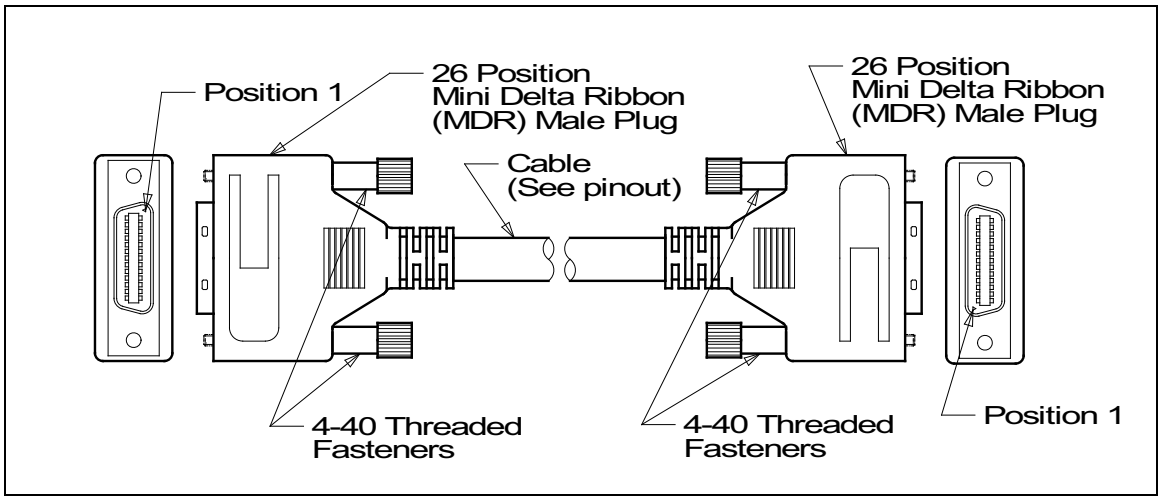


Figure 9-2: Mini Camera Link (MiniCL) Cable Assembly

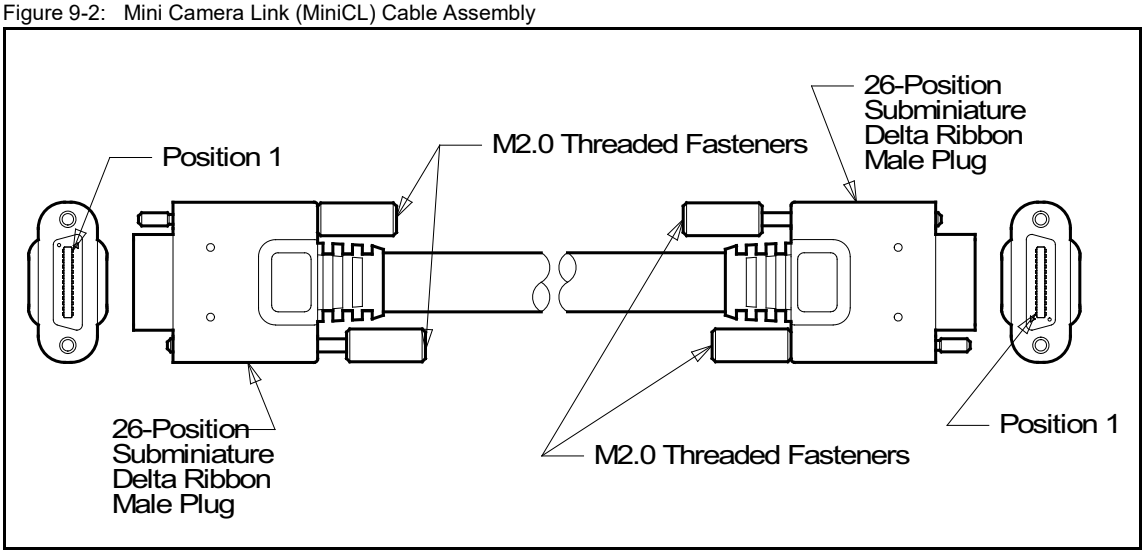


Figure 9-3: Cable assembly with combination of MiniCL and CL connectors

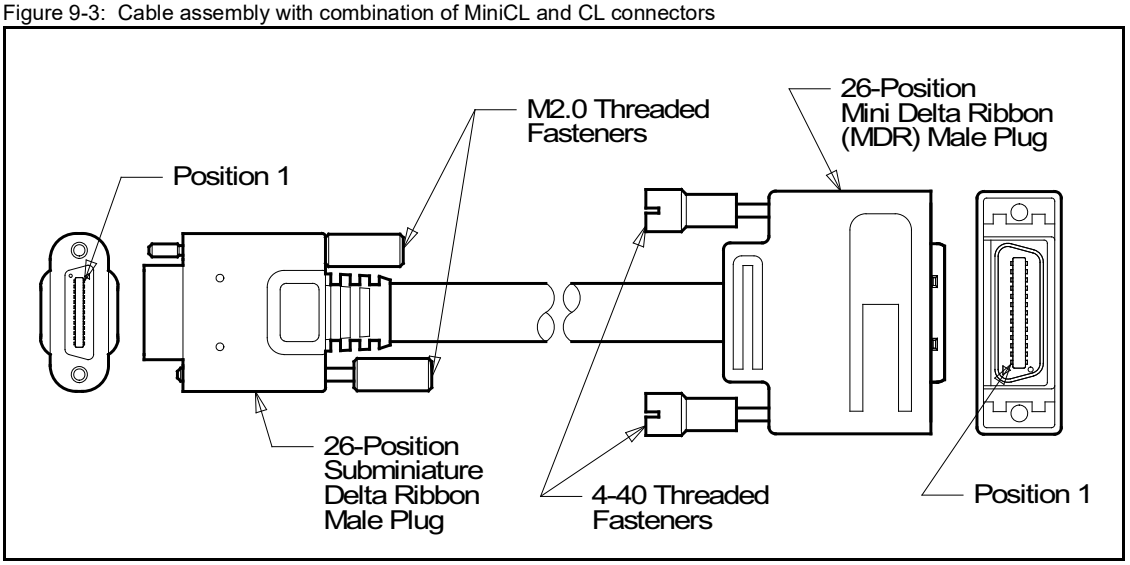


Figure 9-4: PoCL-Lite Configuration Cable Assembly (14pin-14pin)

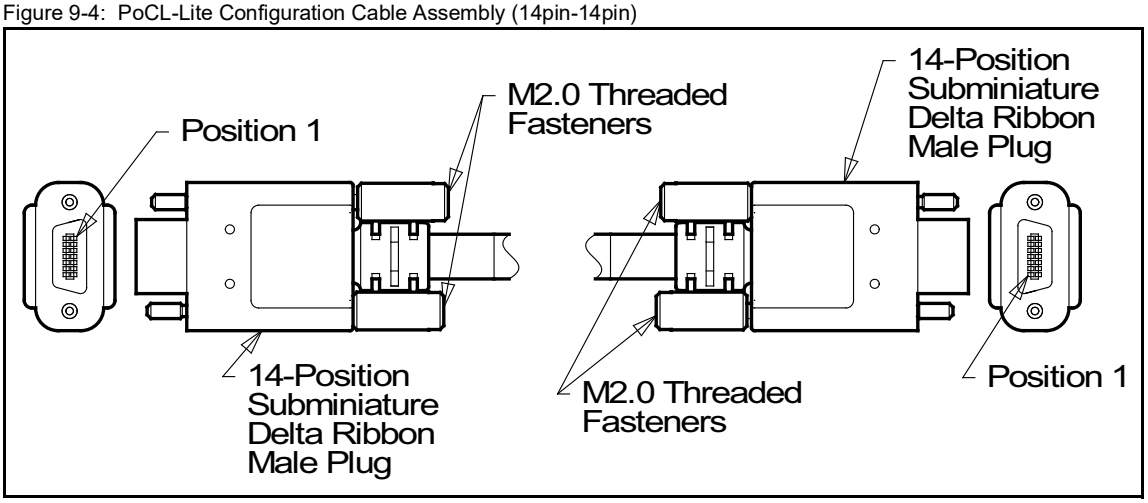


Figure 9-5: PoCL-Lite Configuration Cable Assembly (14pin-26pin)

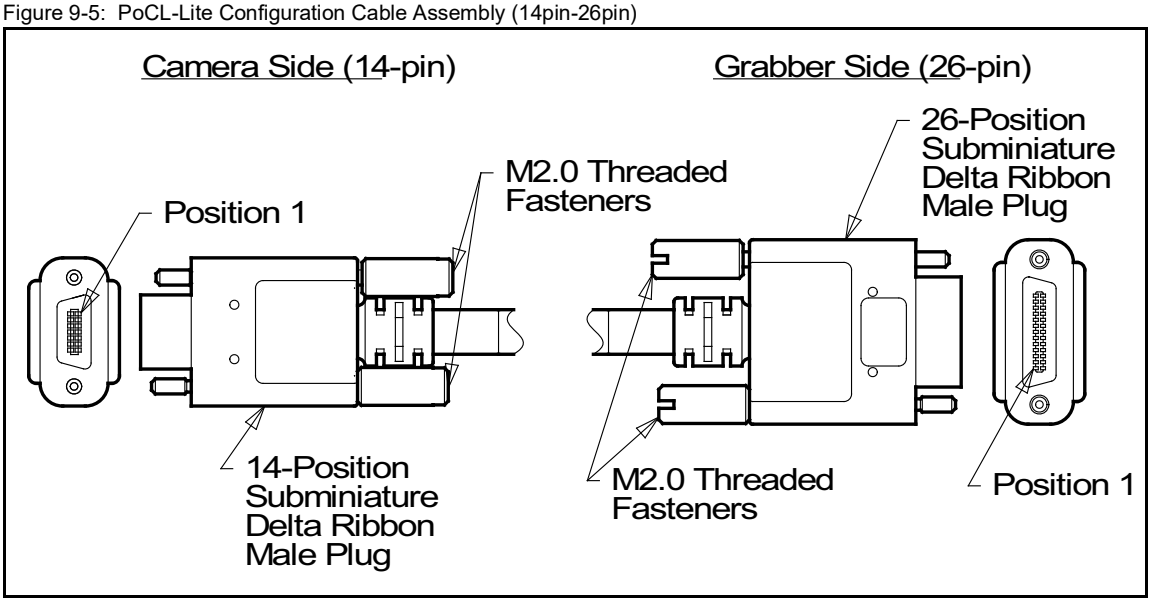


Figure 9-6: PoCL-Lite Configuration Cable Assembly (26pin-14pin)

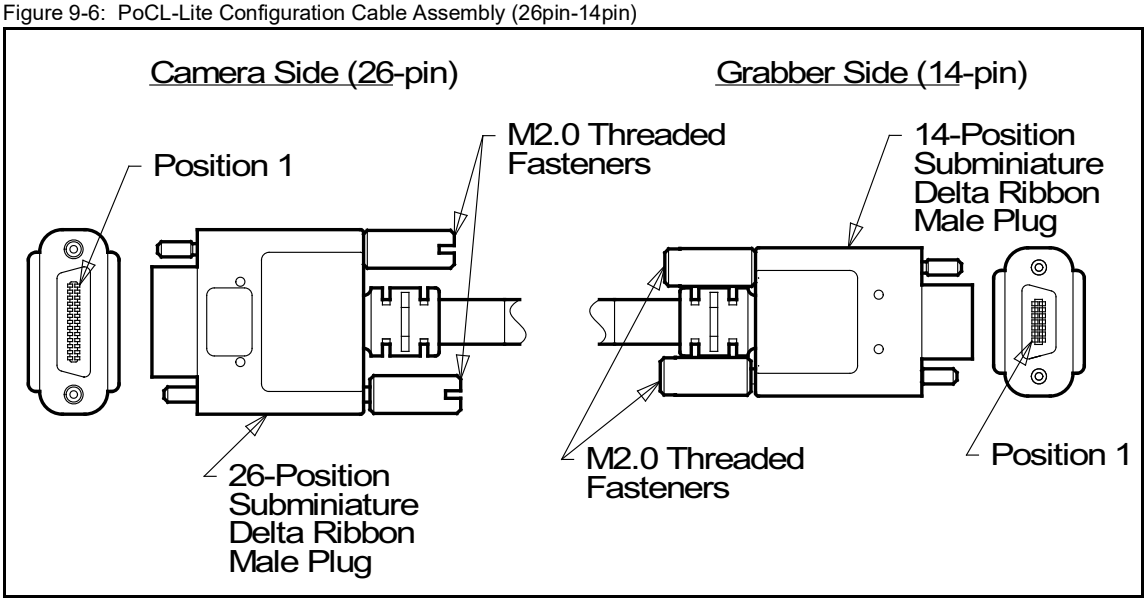


Figure 9-7: Camera Link: 26p Mini Delta Ribbon Receptacle, Thru-hole Type

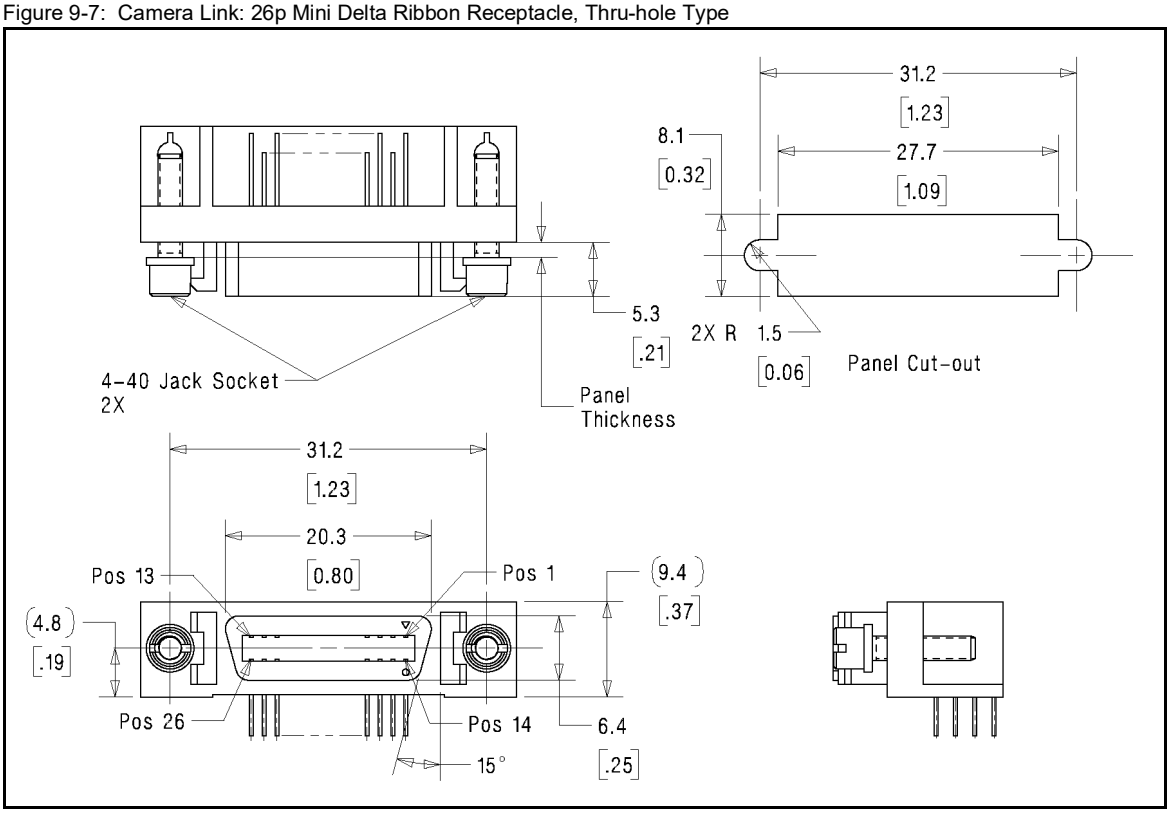


Figure 9-8: MiniCL: 26p Subminiature Delta Ribbon Receptacle, Thru-hole Type

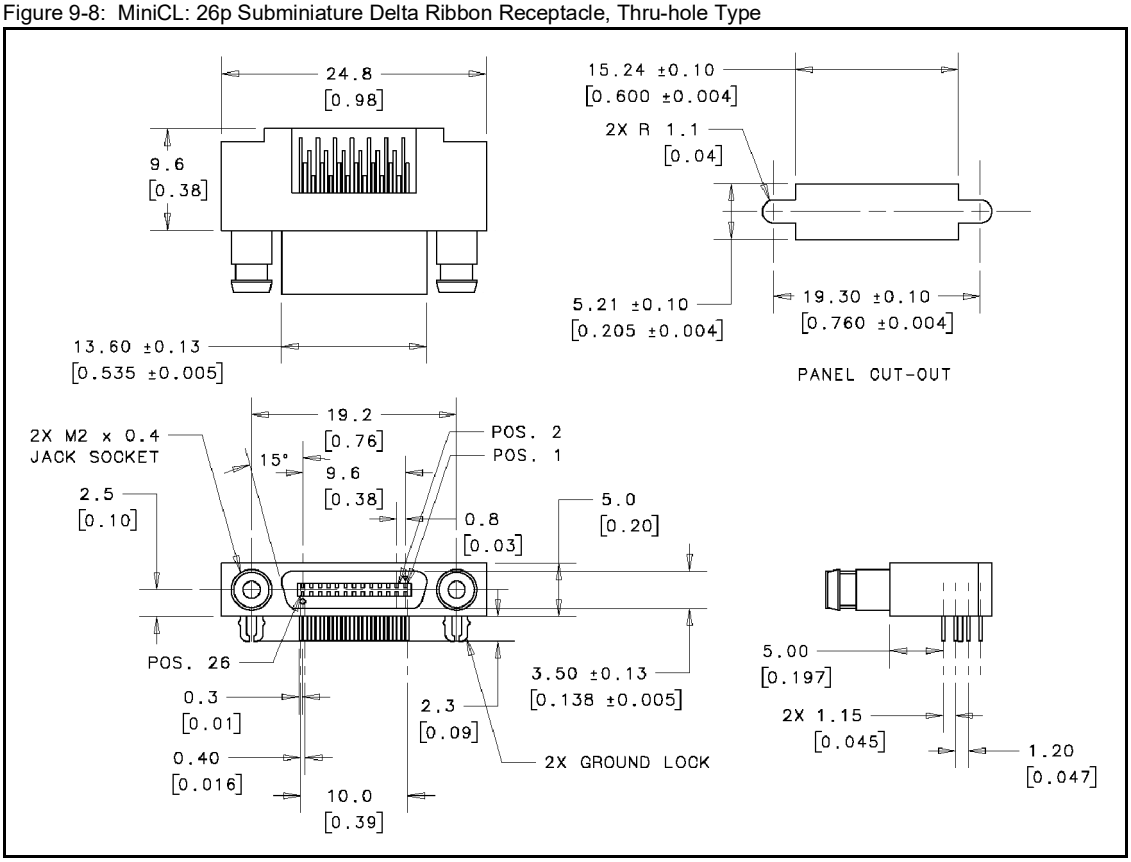
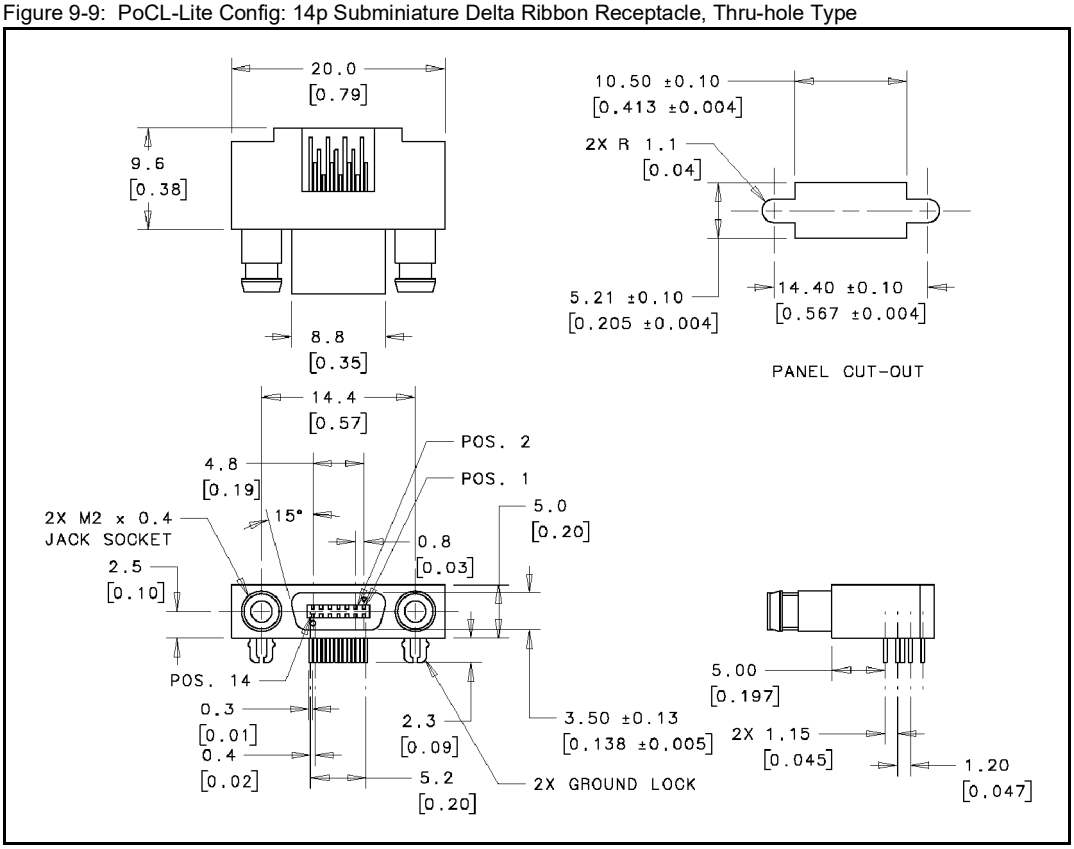


Figure 9-9: PoCL-Lite Config: 14p Subminiature Delta Ribbon Receptacle, Thru-hole Type



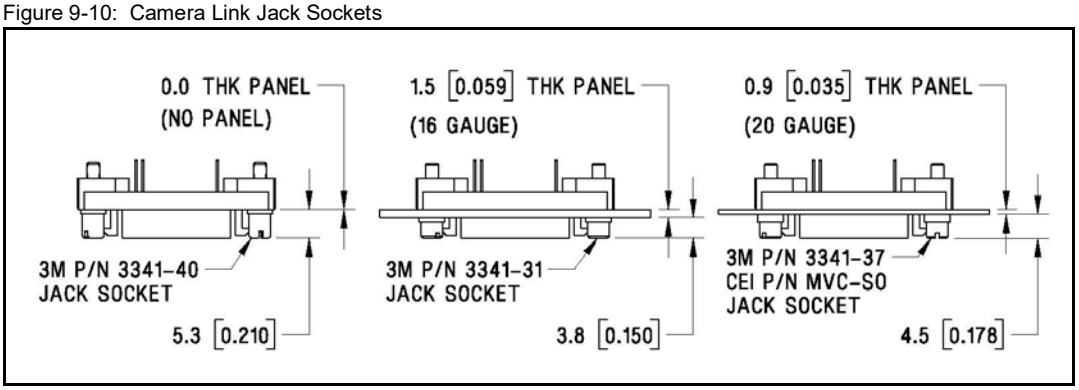
9.1.2.8 Connector Retention

The plug on the cable assembly shall use two threaded fasteners to mount to the receptacle jack sockets and ensure the proper mating of the connector. Proper mating is critical to minimizing radiated emissions and electromagnetic interference.

9.1.2.9 Camera Link Connector Jack Socket Requirements

The jack sockets of the Camera Link receptacle shall be aligned with the end of the receptacle shroud. The proper jack socket should be selected as shown in Figure 9-10 below.

Figure 9-10: Camera Link Jack Sockets

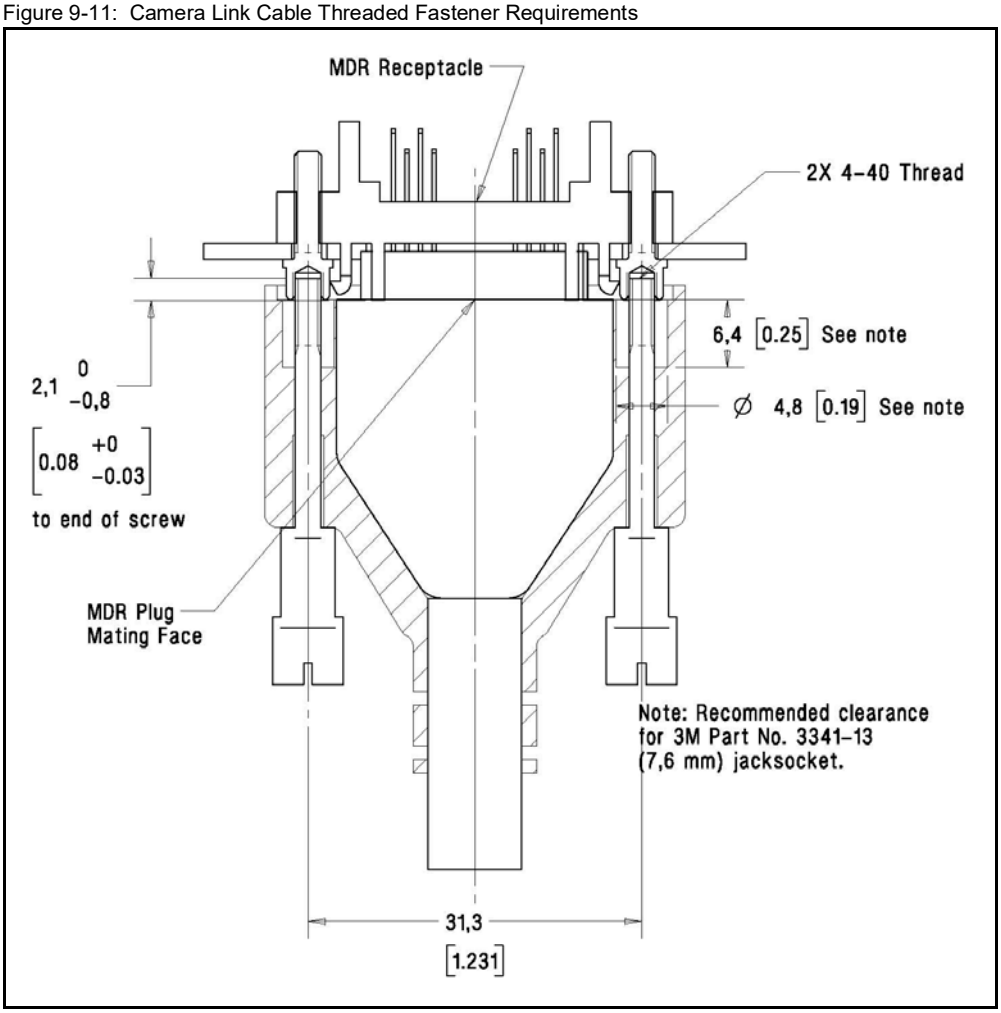


9.1.2.10 Camera Link Cable Threaded Fastener Requirements

The junction shells on both ends of the cable assembly must have threaded fasteners for attachment to the jack sockets on the receptacle connector. The threaded fasteners shall be positioned as shown in Figure 9-11. The threaded fasteners may be thumbscrews, machine screws or other type of threaded fastener that will properly fix the cable assembly to the receptacle.

NOTE: Previous revisions of this specification included the 3M Part No. 3341-13 jack socket. The use of the 3341-13 jack socket was recommended with MDR connectors that are not panel mounted. To insure backward compatibility, Figure 9-7 shows clearance dimensions for the 3341-13 jack socket.

Figure 9-11: Camera Link Cable Threaded Fastener Requirements



9.1.2.11 MiniCL/PoCL-Lite Connector Jack Socket Requirements

To ensure reliable mating of MiniCL and PoCL-Lite connectors, the following requirements are mandatory:

The receptacle connector shall be fitted with jack sockets.

The jack sockets shall have an M2x0.4 female thread.

In addition, the following requirements are recommended:

The jack sockets may be discrete parts screwed into the connector body, or they may be an integral part of the product housing. If discrete parts are used, the vendor should select ones to meet the requirements listed below, based on the panel thickness. A selection of jack sockets known to comply with this specification are listed in Table 9-8 below.

The top of the jack socket should be dimension H above the outer face of the connector as shown in Figure 9-12, with a minimum thread depth of dimension D.

There should not be any counterbore that would reduce the usable thread depth with shorter threaded fasteners on cables.

Table 9-8: Jack Socket Part Numbers

Manufacturer	Part Number	Panel Thickness
3M	12600-S1-10	0.9 .. 1.0
Alysium	A79-4657	0.9 .. 1.0
Components Express	C0460	0.9 .. 1.0
Honda	TBA	0.9 .. 1.0
Intercon 1	90679-001	0.9 .. 1.0

NOTE: Products based around previous versions of this specification (see Appendix A) are still Camera Link compliant. However it is preferable to follow the above recommendations to improve the fit between the jack sockets and the threaded fasteners on the cable.

Figure 9-12: Mating Dimension Definitions

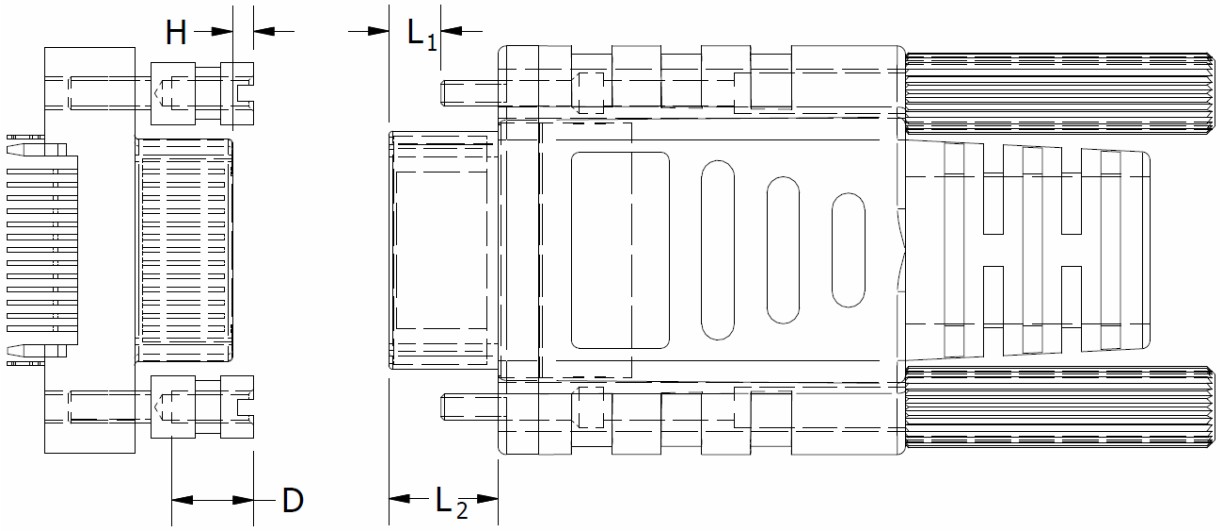
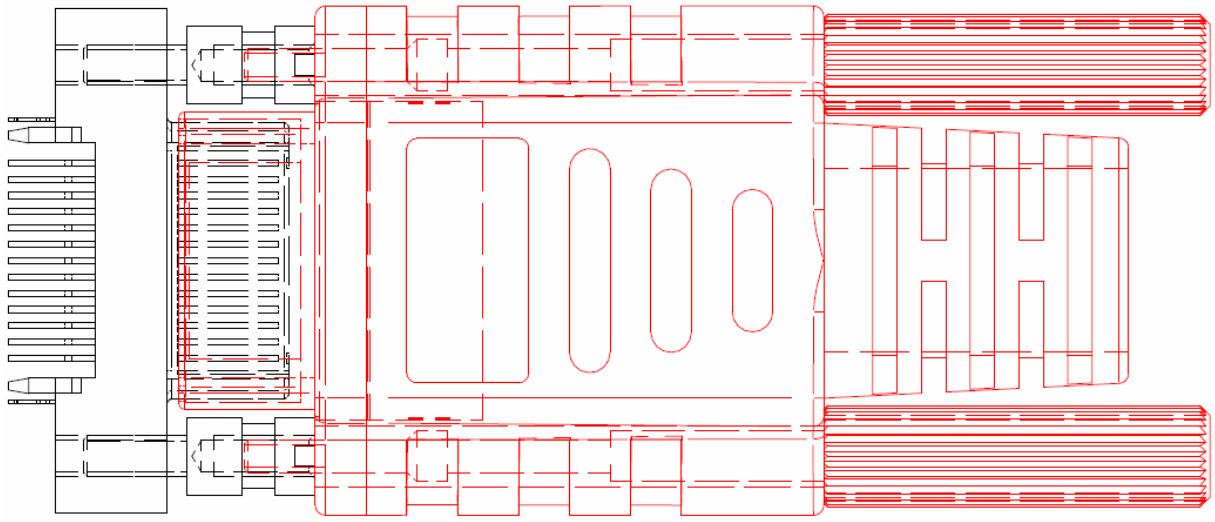


Table 9-9: Dimensions of Figure 9-12

Symbol	Definition	Min (mm)	Max (mm)
H	Top of jack socket above outer face of connector	1.2	1.4
D	Depth of thread in jack socket	5.0	-
L_1	End of fastener below the outer face of connector when the fastener is fully pushed into the connector hood	2.2	2.7
L_2	Outer face of connector above face of connector hood	6.5	6.9

Figure 9-13: Reference View Showing Mated Connectors



9.1.2.12 MiniCL/PoCL-Lite Cable Threaded Fastener Requirements

To ensure reliable mating of MiniCL and PoCL-Lite connectors, the following requirements are mandatory:

The junction shells on both ends of the cable assembly shall have threaded fasteners for attachment to the jack sockets on the receptacle connector.

The threaded fasteners shall have an M2x0.4 male thread.

In addition, the following requirements are recommended:

The end of the threaded fastener should be dimension L_1 below the outer face of the connector as shown in fig 9-12, when the fastener is fully pushed into the hood.

The minimum value of dimension L_1 should apply when the threaded fastener is tightened to a torque of 0.1Nm.

Note: This is hand-tight.

The outer face of the connector should be dimension L_2 above the face of the connector hood.

The threaded fasteners may be thumbscrews, machine screws or any other type of threaded fastener that will properly fix the cable assembly to the receptacle.

NOTE: Products based around previous versions of this specification (see Appendix A) are still Camera Link compliant. However it is preferable to follow the above recommendations to improve the fit between the jack sockets and the threaded fasteners on the cable.

9.1.3 Camera Link Cabling

A Camera Link cable assembly shall consist of a cable meeting the requirements of Section 9.0 Mechanical Interface and Cable Requirements with an approved Camera Link plug on each end. It is the responsibility of the manufacturer of the Camera Link equipment to use the type of cable required to meet applicable regulatory requirements, and the specifications of Section 9.0 Mechanical Interface and Cable Requirements. Adherence to this standard does not guarantee regulatory compliance.

NOTE: While this standard does not require compliance with certain UL, CSA, RoHS or NEC requirements for cabling, it is the responsibility of the cable manufacturer to obtain such compliance when required.

9.1.3.1 Camera Link Cable Certification

Manufactures are required to register their products with AIA to be able to use the Camera Link logos. Failure to maintain current registration or a determination that the products are not compliant will be grounds for removal from the list of registered products and revocation of the right to use the trademarked logos.

The cable assembly manufacturers are required to submit a completed Camera Link Cable Product Compliance Checklist declaring the maximum cable length for the clock speeds to which the manufacturer wishes the cable to be certified.

Once a cable assembly has been certified, it remains certified for the life of the product.

The manufacturer is responsible to submit a new assembly sample for recertification if any changes are made that alter the physical and electrical performance of the cable assembly as defined by the standard.

Examples of cable changes are:

- Cable supplier is changed.
- Any conductors or dielectric materials are changed.
- Cable shields are changed.

9.1.3.2 Cable Jacket

It shall be the responsibility of the manufacturer of the Camera Link cable to use appropriate materials and construction to meet applicable regulatory requirements.

9.1.3.3 Shield Requirement

The Camera Link cable shall be encompassed with an overall braided shield, a foil shield or a combination of foil and braided shields. The foil shield is under the braided shield and both shields surround all conductors in the cable. The minimum braid coverage shall be 80% if no foil shield is used or 65% if used in conjunction with an overall foil shield. Use shield Coverage calculation as specified in ANSI/NEMA WC 27500 paragraph 4.3.5. The foil shield shall provide 100% coverage. There shall be electrical continuity from the outer cable shield through the connector back shells to the connector front shells or shrouds.

The differential pairs or quads, shall be encompassed with a foil shield, a braided shield or a combination of foil and braided shields. These shields and the 4 drain wires (2 drain wires for PoCL® applications) shall be electrically isolated from the overall cable shield.

9.1.3.4 Cable Length

It shall be the responsibility of the end user to evaluate the suitability of a cable for an intended application. The maximum cable length shall be limited by the electrical requirements outlined in Section 9.2.1 Electrical Requirements of this specification.

NOTE: Pair to Pair skew and signal attenuation are critical to system performance. Maximum values for skew and attenuation are a function of the pixel clock rate. The cable assembly manufacturer should include on a label, the maximum pixel clock rate that will function for the length of the cable assembly.

9.1.3.5 Types of Camera Link Cabling

There are three types of cable assemblies: Camera Link, Power over Camera Link (PoCL) and Power over Camera Link Lite (PoCL-Lite). The Camera Link cabling is designed to carry signal data but not power. PoCL cabling is designed to carry power to PoCL compatible devices in addition to signal data. A cable suitable for PoCL use is designed to be backward-compatible – that is, to also be suitable for conventional Camera Link use. Section 9.1.3.6 through Section 9.1.3.8 define the requirements that are unique to each type.

9.1.3.6 Cable Requirements – Camera Link

9.1.3.6.1 Number of Signal Conductors

The Camera Link cable shall comprise 11 differential pairs or 6 differential quads and 4 individual drain conductors. The pin assignment and function of each of these conductors are given in Table 5-1 on page 27 and Table 9-4 on page 59.

9.1.3.6.2 Insulation

Each differential pair conductor in the cable shall be separately insulated. The drain wires shall not be insulated.

9.1.3.6.3 Wire Gauge

Each conductor in a Camera Link cable shall be suitably constructed to meet or exceed the performance requirements as outlined in this document. Use of 28AWG stranded copper wire is recommended for the drain wires.

NOTE: Cable and assembly manufacturer should verify that the conductor size is compatible with the termination method of the connector.

9.1.3.7 Cable Requirements – Power over Camera Link (PoCL)

NOTE: A cable suitable for PoCL use is also suitable for standard Camera Link.

9.1.3.7.1 Number of Signal Conductors

The PoCL cable shall comprise 11 differential pairs or 6 differential quads, two individual power conductors and two drain wires.

9.1.3.7.2 Insulation – Differential Pairs

Each differential pair conductor in the cable shall be separately insulated.

9.1.3.7.3 Insulation – Power and Drain Conductors

The power wire insulation must meet the insulation resistance values specified in paragraph 2.1.1. The drain wires shall not be insulated.

9.1.3.7.4 Wire Gauge

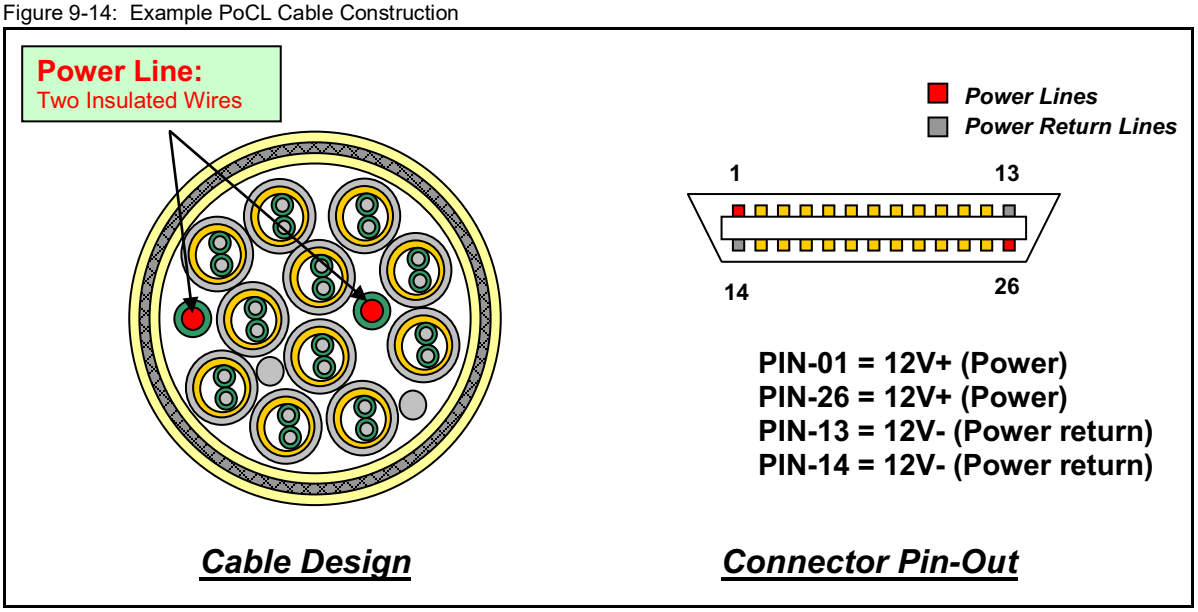
Each conductor in a PoCL cable shall be suitably constructed to meet or exceed the performance requirements as outlined in this document. Both power and power return wires must be capable of handling 1A current under fault conditions. 28AWG stranded copper wire is minimum wire recommended for the power and drain wires.

NOTE: Cable and assembly manufacturer should verify that the conductor size is compatible with the termination method of the connector.

9.1.3.7.5 Labeling

The cable assembly shall be clearly marked to indicate it is a PoCL compatible cable, either with the text “PoCL”, and/or by marking with the PoCL logo. Figure 9-14 shows an example PoCL cable construction as described in the preceding sections.

Figure 9-14: Example PoCL Cable Construction



9.1.3.8 Cable Requirements - PoCL-Lite Configuration

9.1.3.8.1 Number of Signal Conductors

The PoCL-Lite cable shall comprise 5 differential signal pairs or 3 differential quads, 2 individual power conductors and 2 drain wires. The 5 differential signal pairs of this cable shall be shielded. The pin assignment and function of each of these conductors are given in Table 9-5 on page 60 through Table 9-7 on page 61. Figure 9-15 shows an example PoCL-Lite cable construction.

9.1.3.8.2 Insulation - Differential Pairs

Each differential pair conductor in the cable shall be separately insulated.

9.1.3.8.3 Insulation - Power and Drain Conductors

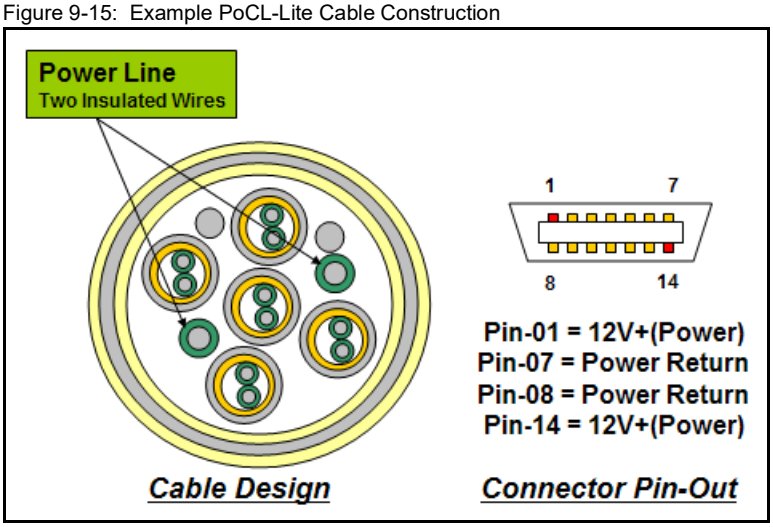
The power wire insulation must meet the insulation resistance values specified in Section 9.2.1.1. The drain wires shall not be insulated.

9.1.3.8.4 Wire Gauge

Each conductor in a Camera Link cable shall be suitably constructed to meet or exceed the performance requirements as outlined in this document. Use of 28AWG stranded copper wire is recommended for the drain wires.

NOTE: Cable and assembly manufacturer should verify that the conductor size is compatible with the termination method of the connector.

Figure 9-15: Example PoCL-Lite Cable Construction



9.2 Testing Requirements

The performance and testing requirements for the Camera Link cable assembly is described in this section. Test procedures and requirements from ANSI/NEMA WC 27500 and EIA/TIA 364-90 as well as EIA-364-107 are used, where applicable. All rise times (transition times) are from 10% to 90% of amplitude as shown in EIA-364-90, Figure 1. Test equipment used for the certification process must be capable of accurately producing and measuring the described signals outlined in the following requirements. The test equipment must be current in its calibration. Records of compliance tests must be maintained for a minimum of 3 years and be available for review if requested by the AIA.

9.2.1 Electrical Requirements

9.2.1.1 Dielectric Withstanding Voltage of PoCL and PoCL-Lite power wires

This test is conducted on cable, not assemblies. The cable manufacturer shall supply a certificate of compliance of the test results with the assembly submitted for certification.

The power wires in PoCL cable shall be tested for a minimum dielectric withstanding voltage of 500 volts measured in accordance to ANSI/NEMA WC 27500 paragraph 4.3.3. Testing shall be conducted by applying voltage to the power wires and monitoring all other conductors and shields for leakage current.

9.2.1.2 Shield Isolation

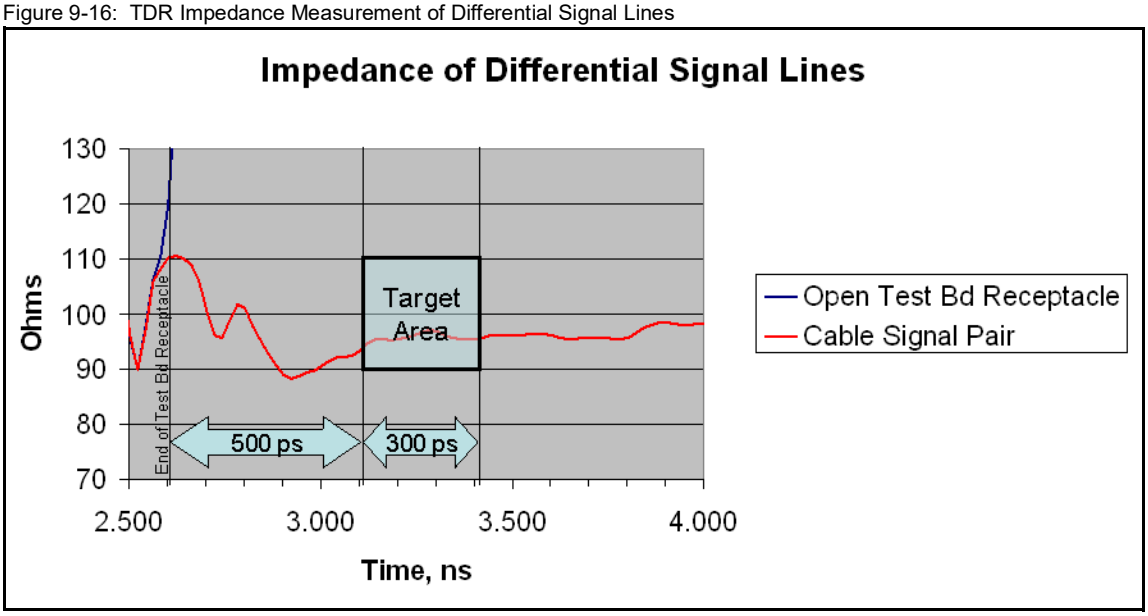
This test is conducted on cable, not assemblies. The cable manufacturer shall supply a certificate of compliance of the test results with the assembly submitted for certification.

The inner and outer shielding of Camera Link, PoCL and PoCL-Lite cable shall be isolated from each other by a minimum dielectric withstanding voltage of 500 volts measured in accordance to ANSI/NEMA WC 27500 paragraph 4.3.3. Testing shall be conducted by applying voltage to the drain wires and monitoring the overall shield for leakage current.

9.2.1.3 Impedance of Differential Signal Lines

The cable assembly shall be tested using a time domain reflectometry method using a differential pulse with a 500ps rise time. Pins 1, 13, 14 and 26 shall be grounded. The balanced impedance of each differential pair shall be 100 Ohms +/-10 Ohms. The impedance shall be measured between 500 and 800 picoseconds after the end of the open test board receptacle as shown in Figure 9-16 below.

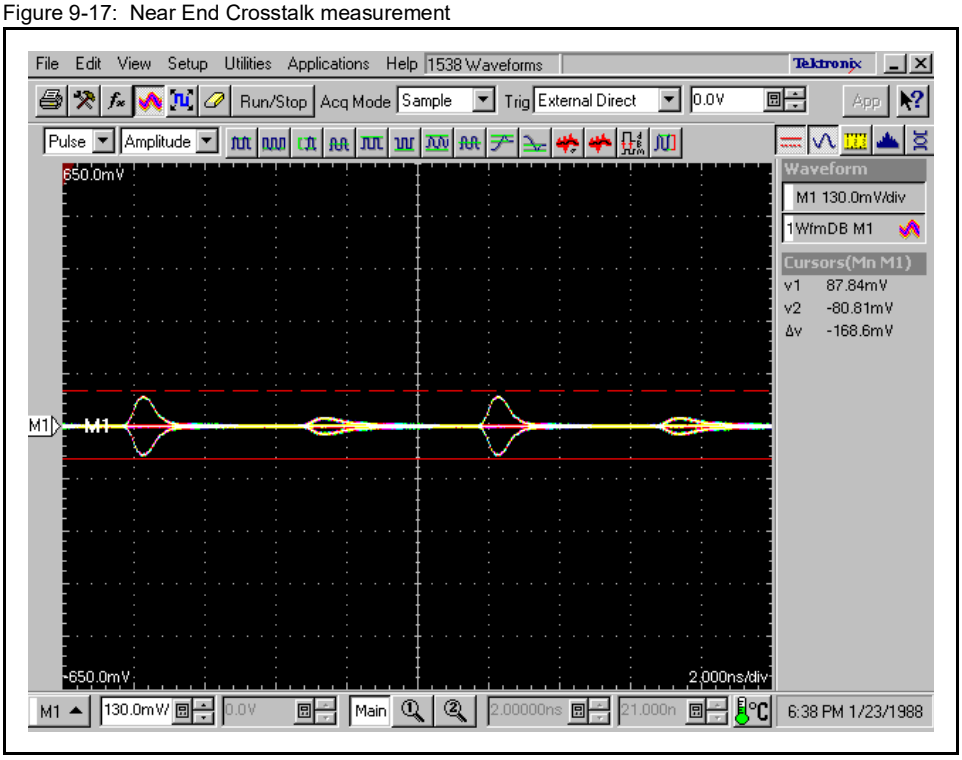
Figure 9-16: TDR Impedance Measurement of Differential Signal Lines



9.2.1.4 Near End Crosstalk of Differential Signal Lines

The cable assembly shall be tested according to EIA/TIA 364-90, using a 700 mV peak to peak differential signal with 500ps rise time, 595 Mbps bit rate. The differential signal should be transmitted on pair 3 (Table 9-4 on page 59) and cross talk measured on pair 2 and pair 4, adjacent pairs. The measured peak crosstalk shall not exceed 20% between any two pairs as shown in Figure 9-17.

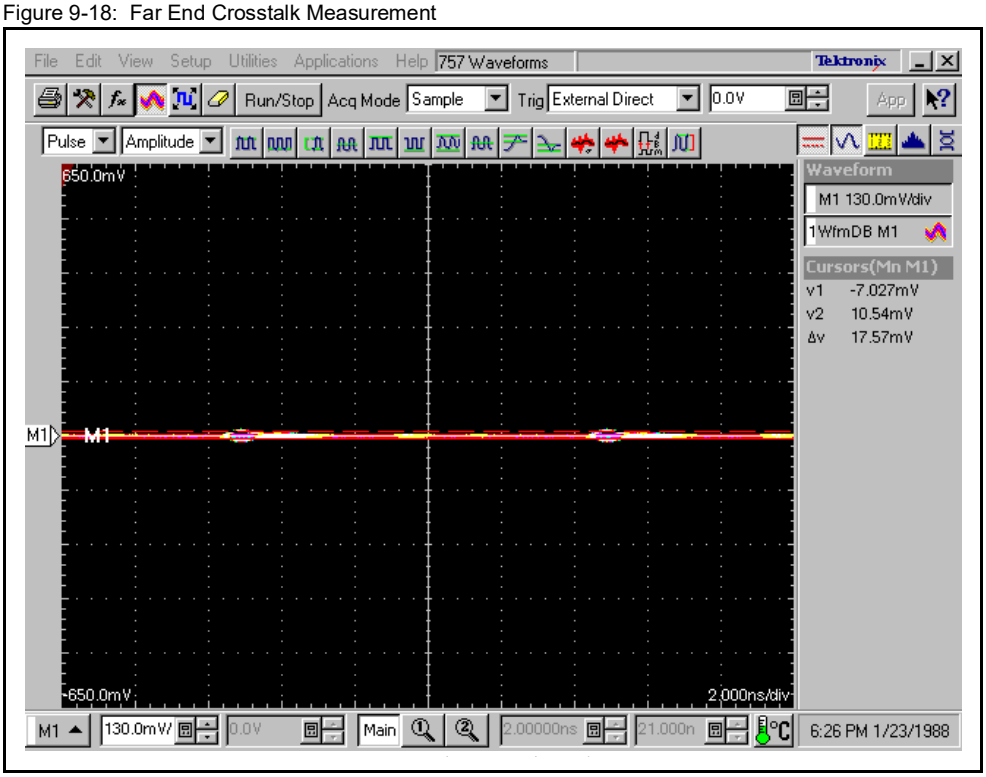
Figure 9-17: Near End Crosstalk measurement



9.2.1.5 Far End Crosstalk of Differential Signal Lines

The cable assembly shall be tested according to EIA/TIA 364-90, using a 700 mV differential signal with 500 ps rise time, 595 Mbps bit rate. The differential signal should be transmitted on pair 3 (Table 9-4 on page 59) and cross talk measured on pair 2 and pair 4, adjacent pairs. The measured peak crosstalk shall not exceed 20% between any two pairs as shown in Figure 9-18.

Figure 9-18: Far End Crosstalk Measurement



9.2.1.6 Crosstalk of Power Lines (PoCL and PoCL-Lite cabling only)

PoCL and PoCL-Lite cables shall meet the following cross-talk requirement between the power lines and signal lines. This cross-talk is defined as the induced signal between the power lines and a signal lines in differential mode. The cross-talk value shall be not more than 20% of the injected signal.

Test Conditions

The following test conditions were used:

- Input pulse: 30 ns pulse width
- Amplitude: 500 mV
- Rise Time: 500 ps (595MHz bandwidth)
- Pulse Input line: Power wire
- Measurement line: Each twisted pair, measured 1 pair at a time.

See Figure 9-19 through Figure 9-22 below for the measurement method of near end and far end crosstalk.

Figure 9-19: Measurement System for Near-End Cross-Talk

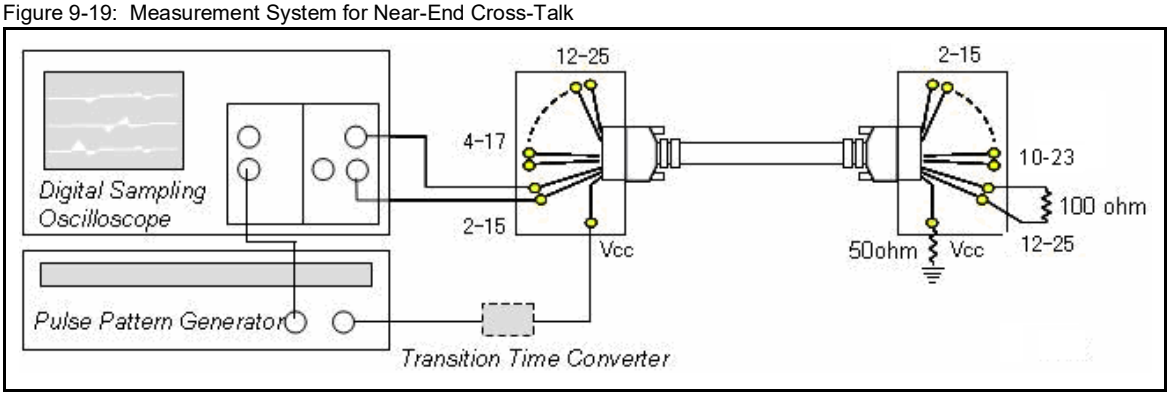


Figure 9-20: Measurement System for Far-End Cross-Talk

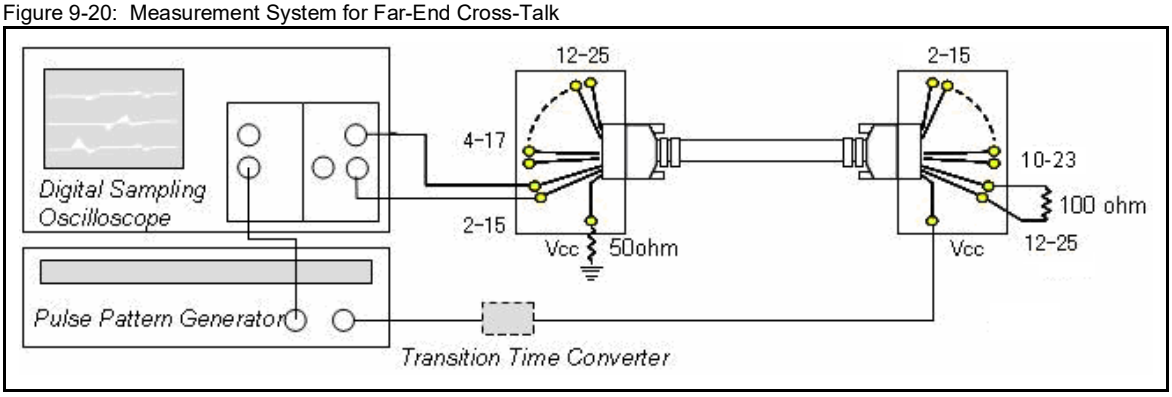


Figure 9-21: Measurement System for Near-End Cross-Talk (PoCL-Lite Configuration)

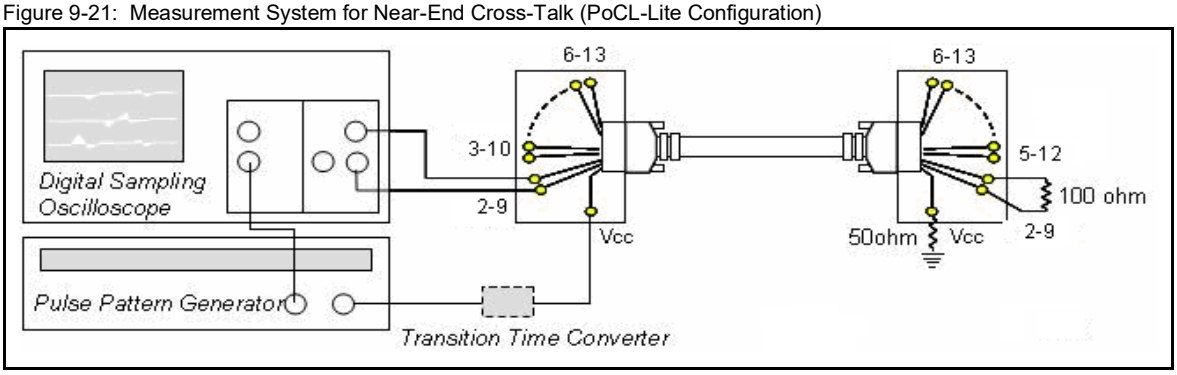
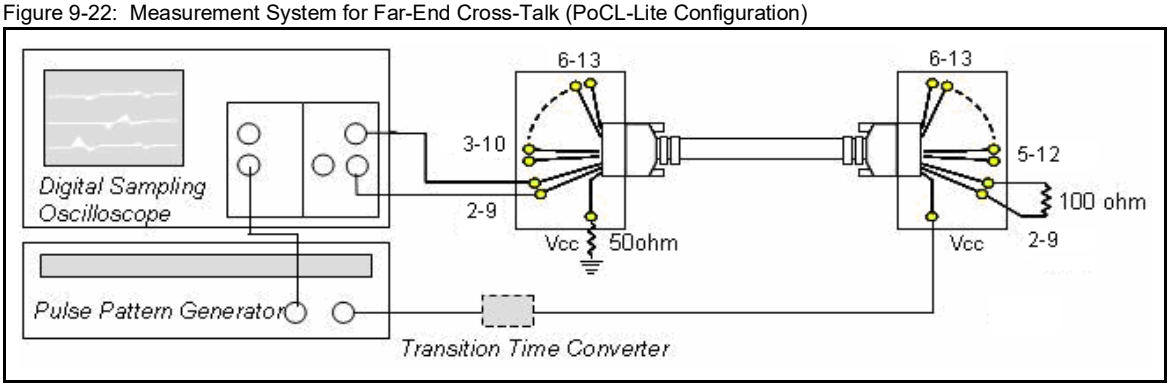


Figure 9-22: Measurement System for Far-End Cross-Talk (PoCL-Lite Configuration)



9.2.1.7 Within Pair Skew of Differential Signal Lines

Within pair skew is measured between the conductors within a signal pair using a 1V to 1.1V differential signal with 500ps rise time, 100 Mbps bit. Skew testing can also be conducted using a suitable oscilloscope equipped with a Time Domain Reflectometry (TDR) module. The within pair skew value shall not exceed the value shown in Table 9-10.

Table 9-10: CL Cable Assembly Rated Speed vs. Maximum Single Pair and Pair-to-Pair Skew

Pixel Clock Frequency	Maximum Skew (ps)
40 MHz	390
66 MHz	290
85 MHz	190

9.2.1.8 Pair to Pair Skew of Differential Signal Lines within data and clock groups

Pair to pair skew is measured between pairs using a 1V to 1.1V differential signal with 500ps rise time, 100 Mbps bit rate. Skew testing can also be conducted using a suitable oscilloscope equipped with a Time Domain Reflectometry (TDR) module.

The Channel Link chip set uses 4 pairs for data and 1 pair for clock (See “Channel Link Operation” on page 2.). This is defined as the data and clock group. Camera Link cables assign data and clock signals to pairs 1 – 5 and 7 – 11 (Table 5-1 on page 27). There are 2 data and clock groups in Camera Link and PoCL cables. The pair to pair skew value measured within each data and clock group and shall not exceed the value shown in Table 9-10.

NOTE: Connector termination methods may impact skew. It is the responsibility of the manufacturer to verify the performance of assemblies when the connector termination method or the cable exit on the backshell is changed. An assembly that meets Cameral Link skew requirements with a straight exit from the backshell, may not meet the skew requirements with a right angle exit from the backshell. Recertification of an assembly is required if the connector type change results in a performance change.

9.2.1.9 Eye Mask Definition

Eye Mask measurements shall be taken using a 700 mV peak to peak differential signal with a 500ps rise time. The data rate used during the measurement is based on the clock frequency and can be found in Table 9-11. An example of the eye mask for the 85 MHz eye pattern is shown in Figure 9-23. Upper and lower masks are located at +/- 350mV and the length varies with the period of the bit.

Figure 9-23: Eye Mask Diagram

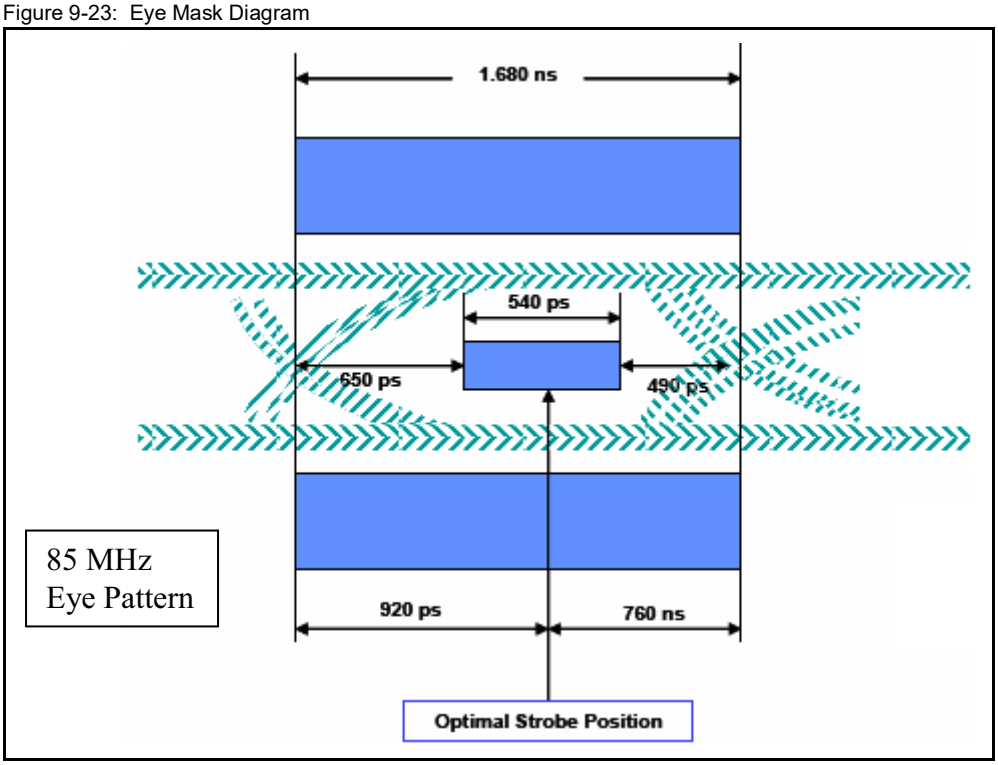


Table 9-11: Camera Link Eye Mask

Pixel Clock Frequency	Data rate	RSKM	Mask Width	Mask Height
40 MHz	280 Mbps	1685 ps	540 ps	± 100 mV
66 MHz	462 Mbps	915 ps	540 ps	± 100 mV
85 MHz	595 Mbps	650 ps	540 ps	± 100 mV

NOTE: Work instructions, including examples of eye mask code for the Agilent 86100 digital oscilloscope and other reference documents may be found at the following URL:

http://www.visiononline.org/userAssets/aiaUploads/File/Camera_Link_Assembly_Test_Plan.pdf.

9.2.1.10 Current Capacity for PoCL and PoCL-Lite

The power and drain wires within a cable assembly shall be capable of handling 1.0A camera current under fault conditions. The power and drain wires shall be at least AWG 28 or larger diameter.

9.2.1.11 Conductor Resistance for PoCL and PoCL-Lite

The DC resistance of any power wire or drain wire shall not exceed 2.5 Ω for the length of the cable assembly. Resistance of the power and drain wires shall be such that the voltage drop is less than 0.5V for the length of the cable assembly at a 400 mA operating current.

NOTE: The resistance of each of the two power lines and two power returns shall be less than 2.5

ohms. This gives a 1.25 ohm resistance when measured in parallel, giving a 0.5V drop along the cable at a current of 400mA.

10.0 Power over Camera Link (PoCL)

10.1 Introduction

10.1.1 Overview

This chapter describes an extension to the Camera Link® standard to allow the camera to be powered by the frame grabber along the Camera Link cable. This allows a single cable solution to provide power and data, useful in low cost applications.

Power is supplied to the camera by redefining the four "Inner Shield" wires in a Camera Link cable as two power lines and two power returns. This means that PoCL® continues to use the existing Camera Link connectors, allowing backwards compatibility with existing equipment.

PoCL is defined for base, medium, full,72 bit and 80 bit systems. Additionally, PoCL is the standard configuration for Lite systems.

NOTE: The power available through the Camera Link cable is limited and may not be sufficient for high performance cameras. Therefore PoCL does not replace cameras with separate power supplies, which will continue to be the best solution for many applications.

10.1.2 Backward Compatibility with non-PoCL Devices

The PoCL standard uses the existing 26 way connectors defined for Camera Link, with both the standard (MDR) and mini (HDR/SDR) connectors being supported.

All existing signals and functions available to a conventional (non-PoCL) system are still available in a PoCL system.

Cable lengths and operating speeds are unchanged from conventional Camera Link.

This standard defines the SafePower protocol to protect systems in the event of an accidental mix of PoCL and conventional Camera Link products.

There are no changes to the requirements for base configuration operation between non-PoCL devices and PoCL devices. Changes to frame grabber requirements for medium/full/72 bit/80 bit operation are minimal and are described in Section 10.4.4. PoCL and conventional cables should not be mixed in dual cable configurations. Table 10-1 summarizes the compatibility of PoCL Frame Grabbers, Cables and Cameras in the various combinations.

NOTE: Many frame grabbers designed to Camera Link v1.2 and which support dual base configuration operation may already support medium/full/72 bit/80 bit configuration PoCL cameras.

Table 10-1: Compatibility Table

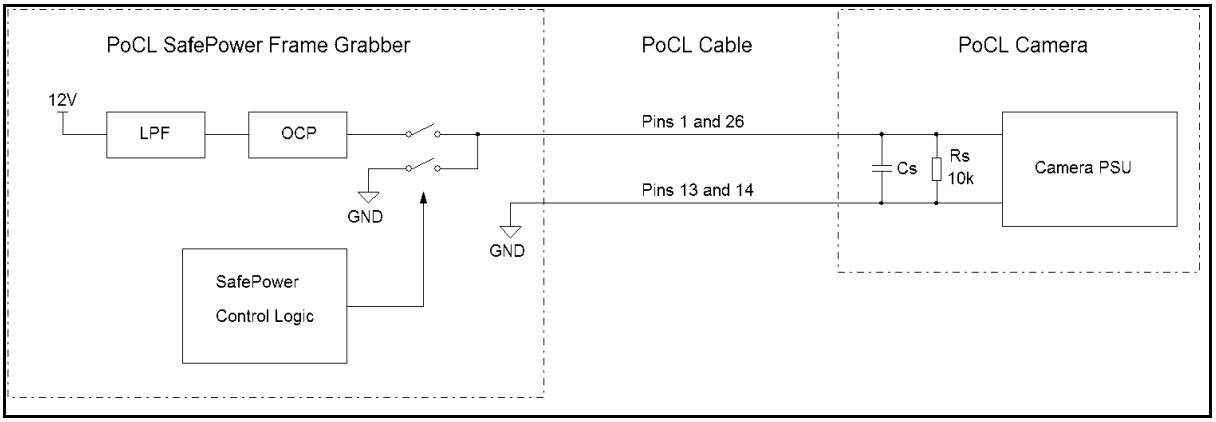
Frame Grabber	Cable	Camera	Valid Combination
Conventional	Conventional	Conventional	Yes, operates normally
		PoCL	Only if the camera has an auxiliary power connector
	PoCL	Conventional	Yes, operates normally
		PoCL	Only if the camera has an auxiliary power connector
PoCL	Conventional	Conventional	Only if the frame grabber supports SafePower
		PoCL	Only if the camera has an auxiliary power connector, and the frame grabber supports SafePower
	PoCL	Conventional	Only if the frame grabber supports SafePower
		PoCL	Yes, frame grabber powers camera

NOTE: In the Medium/Full/72 bit/80 bit configuration systems, "conventional" applies in the table when either one or both cables are conventional; however, it is recommended not to mix styles.

10.1.3 Simplified Block Diagram (Base Configuration)

Figure 10-1 shows a simplified block diagram for the Base Configuration.

Figure 10-1: PoCL Block Diagram



where:

LPF	Power supply low pass filter (see Section 10.4.5)
OCP	Over current protection circuit (see Section 10.4.3.1)
SafePower	SafePower protection protocol (see Section 10.4.3.2)
Rs	Camera sense resistor for SafePower (see Section 10.3.2.1).
Cs	Camera input capacitance for SafePower (see Section 10.3.2.2).

10.2 PoCL Pinouts for Specific Configurations

10.2.1 Camera Link Cable Pinout Changes For PoCL Configuration

The only change is the redefinition of the four “Inner Shield” wires as shown in Table 10-2

Table 10-2: Pinout assignments

Pin	Conventional Camera Link	PoCL
1	Inner Shield	Power (nominal 12V DC)
26	Inner Shield	Power (nominal 12V DC)
13	Inner Shield	Power Return
14	Inner Shield	Power Return

NOTE: All four power lines still reduce noise sensitivity of the cable.

10.2.2 Camera Link Cable Pinout For PoCL-Lite Configurations

The following tables show the cable pinout for 26P PoCL-Lite (Table 10-3), 26P PoCL-Base (Figure 10-4), 14P(Table 10-5), 14P-26P(Table 10-6), and 26P-14P(Table 10-7) confirmations.

Table 10-3: 26P Connector Assignments PoCL-Lite

PoCL-Lite Configuration			
Camera Connector	**Frame Grabber Connector**	**Channel Link Signal**	**Cable Name**
1	1	Power	Power
14	14	Inner shield	Inner shield
2	25	X0-	PAIR1-
15	12	X0+	PAIR1+
3	24	NC	
16	11	NC	
4	23	X2-	PAIR2-
17	10	X2+	PAIR2+
5	22	Xclk-	PAIR3-
18	9	Xclk+	PAIR3+
6	21	NC	
19	8	NC	
7	20	SerTC+	PAIR4+
20	7	SerTC-	PAIR4-
8	19	NC	
21	6	NC	
9	18	CC-	PAIR5-
22	5	CC+	PAIR5+
10	17	NC	
23	4	NC	
11	16	NC	
24	3	NC	
12	15	NC	

Table 10-3: 26P Connector Assignments PoCL-Lite (Continued)

PoCL-Lite Configuration			
Camera Connector	**Frame Grabber Connector**	**Channel Link Signal**	**Cable Name**
25	2	NC	
13	13	Inner shield	Inner shield
26	26	Power	Power

Table 10-4: 26P Connector Assignments PoCL Base

PoCL-Base Configuration		
Camera Connector	**Frame Grabber Connector**	**Channel Link Signal**
1	1	Power
14	14	Inner shield
2	25	X0-
15	12	X0+
3	24	X1-
16	11	X1+
4	23	X2-
17	10	X2+
5	22	Xclk-
18	9	Xclk+
6	21	X3-
19	8	X3+
7	20	SerTC+
20	7	SerTC-
8	19	SerTFG-
21	6	SerTFG+
9	18	CC1-
22	5	CC1+
10	17	CC2+
23	4	CC2-
11	16	CC3-
24	3	CC3+
12	15	CC4+
25	2	CC4-
13	13	Inner shield
26	26	Power

Table 10-5: 14P Connector Assignments

PoCL-Lite Configuration			
Camera Connector	**Frame Grabber Connector**	**Channel Link Signal**	**Cable Name**
1	1	Power	Power
8	8	Inner shield	Inner shield
2	9	SerTC+	PAIR1+
9	2	SerTC-	PAIR1-
3	12	X0-	PAIR2-
10	5	X0+	PAIR2+
4	11	X2-	PAIR3-
11	4	X2+	PAIR3+
5	10	Xclk-	PAIR4-
12	3	Xclk+	PAIR4+
6	13	CC-	PAIR5-
13	6	CC+	PAIR5+
7	7	Inner shield	Inner shield
14	14	Power	Power

Table 10-6: 14P-26P Connector Assignments

PoCL-Lite Configuration			
Camera Connector (14P)	**Frame Grabber Connector (26P)**	**Channel Link Signal**	**Cable Name**
1	1	Power	Power
8	14	Inner shield	Inner shield
2	20	SerTC+	PAIR1+
9	7	SerTC-	PAIR1-
3	25	X0-	PAIR2-
10	12	X0+	PAIR2+
4	23	X2-	PAIR3-
11	10	X2+	PAIR3+
5	22	Xclk-	PAIR4-
12	9	Xclk+	PAIR4+
6	18	CC-	PAIR5-
13	5	CC+	PAIR5+
7	13	Inner shield	Inner shield
14	26	Power	Power

Table 10-7: 26P-14P Connector Assignments

PoCL-Lite Configuration			
Camera Connector (26P)	**Frame Grabber Connector (14P)**	**Channel Link Signal**	**Cable Name**
1	1	Power	Power
14	8	Inner shield	Inner shield
7	9	SerTC+	PAIR1+
20	2	SerTC-	PAIR1-
2	12	X0-	PAIR2-
15	5	X0+	PAIR2+
4	11	X2-	PAIR3-
17	4	X2+	PAIR3+
5	10	Xclk-	PAIR4-
18	3	Xclk+	PAIR4+
9	13	CC-	PAIR5-
22	6	CC+	PAIR5+
13	7	Inner shield	Inner shield
26	14	Power	Power

10.3 Camera Requirements

10.3.1 Operating Requirements

10.3.1.1 Voltage

The camera shall operate over a range of 10V DC to 13V DC.

NOTE: This allows for a 1V round-trip drop in the cable compared to the frame grabber requirements.

10.3.1.2 Power

The camera shall draw a maximum of 4W per cable.

NOTE: 4W gives a current of 333mA at the nominal 12V, or 400mA at the minimum 10V, for base configuration cameras. Medium/full/72 bit/80 bit configuration cameras can draw a maximum of 8W, giving a current of 666mA at 12V, or 800mA at the minimum 10V.

The camera shall tie together pin 1 to pin 26, and pin 13 to pin 14, on the Camera Link connector(s).

NOTE: This helps ensure that the power is equally split between the four power lines in the cable.

See Section 10.3.4 for additional requirements for medium/full/72 bit/80 bit systems.

10.3.2 Support for SafePower

All PoCL cameras shall implement the following requirements to allow SafePower frame grabbers to operate correctly.

These requirements apply to both connectors on medium/full/72 bit/80 bit cameras.

10.3.2.1 Input Resistance

A 52µA sense current into pins 1 and 26 shall result in a voltage drop across Rs of 0.52V ± 5%.

NOTE: This is essentially specifying a 10kΩ sense resistor Rs, but worded to allow the resistor value to be increased to allow for any power drawn by the camera's power supply at the nominal 0.52V sense voltage. A 10kΩ sense resistor will result in additional 14mW of power dissipation in the camera at 12V, which should not be significant. The sense resistor is labeled "Rs" in Figure 10-1.

10.3.2.2 Input Capacitance

The camera shall have a maximum input capacitance Cs on each Camera Link connector of 57µF.

NOTE: The value of 57uF allows a 47uF 20% component to be used. This capacitor is labeled "Cs" in Figure 10-1.

10.3.2.3 Camera Link Clock

The camera shall provide a clock on the clock pair on pins 9 and 22 of its Camera Link connector(s) within 3s, however it is recommended that the camera provides this clock in the shortest time possible.

The camera shall not at any time suspend the clock pair on pins 9 and 22 of its Camera Link connector(s) for more than 100ms.

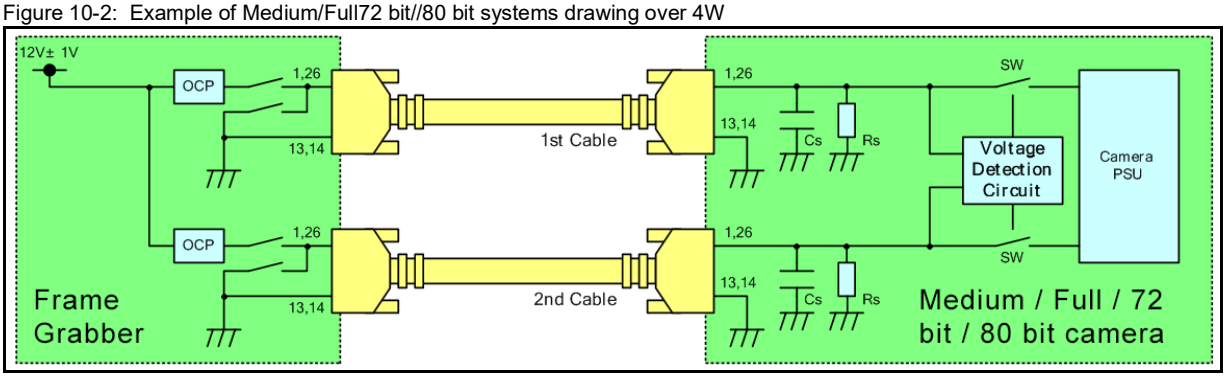
10.3.3 Labeling

The camera shall be clearly marked to indicate it is a PoCL camera, either with the text "PoCL", and/or by marking with the PoCL logo.

10.3.4 Medium, Full, 72 bit, 80 bit Cameras

Figure 10-2 shows an example of a Medium/Full/72 bit/80 bit system drawing over 4W.

Figure 10-2: Example of Medium/Full72 bit//80 bit systems drawing over 4W



Medium/full/72 bit/80 bit configuration cameras that draw more than 4W shall implement the following requirements to ensure that Section 10.3.1.2 is met:

a. The camera shall draw a maximum of 8W.

b. The camera's power supply shall be designed so that it does not draw more than 4W per cable.

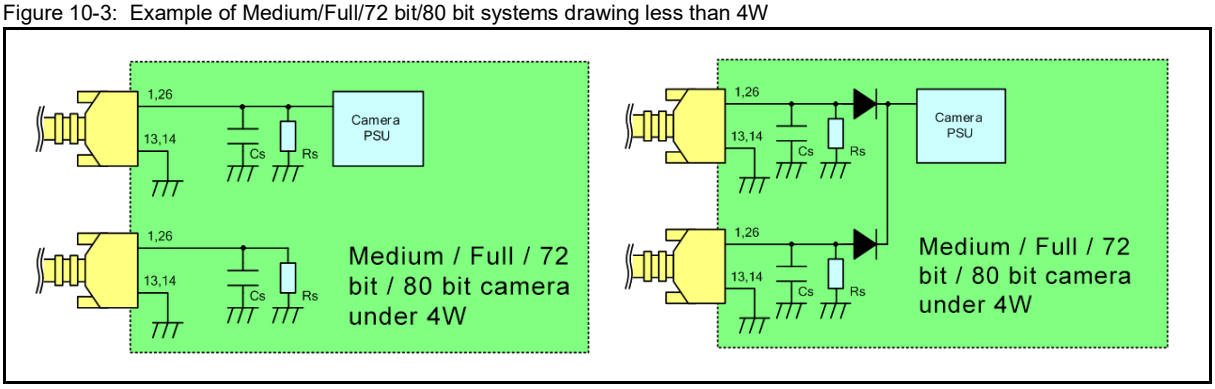
c. The camera's power supply shall be designed to isolate the two Camera Link connectors, i.e. power applied to one connector shall not be injected into the other one.

d. The camera shall implement a voltage detection circuit that only enables the camera's power supply when power is present on both Camera Link cables. The value in Section 10.3.2.3 shall apply from the time when power is present on both Camera Link cables.

Note: This allows for any time delay between the SafePower circuits on each of the frame grabber's connectors, and also allows for one cable being disconnected.

Figure 10-3 shows an example of a Medium/Full/72 bit/80 bit system drawing less than 4W.

Figure 10-3: Example of Medium/Full/72 bit/80 bit systems drawing less than 4W



Medium/full/72 bit/80 bit configuration cameras that draw less than 4W can implement a simpler system:

a. The camera can draw power from just the "base" connector, however both connectors shall comply with the SafePower requirements for components Rs and Cs.

NOTE: The requirements for Rs and Cs allow use of a non-SafePower frame grabber.

b. Alternatively the camera can draw power from both connectors. In this case the camera's power supply shall be designed to isolate the two Camera Link connector, i.e. power applied to one connector shall not be injected into the other one.

10.3.5 Additional Power Connectors

A PoCL camera can have auxiliary power connectors to allow it to be used with in a system with a separate power supply in the event that the frame grabber does not support PoCL. In this case the camera shall be designed to isolate the power sources. In particular the auxiliary connector(s) shall not inject power into the frame grabber, and the Camera Link PoCL connector(s) shall not inject power into the auxiliary connector(s).

NOTE: This prevents damage in the event that both a PoCL frame grabber and the separate power supply are used concurrently.

10.4 Frame Grabber Requirements

10.4.1 Compatibility

A frame grabber can be dedicated to PoCL operation ("Dedicated PoCL frame grabber"), so always supplying 12V. Alternatively the 12V can be switchable to ground to allow the frame

grabber to operate with both PoCL and conventional Camera Link cameras (“Switchable PoCL frame grabber”).

10.4.2 Operating Requirements

10.4.2.1 Voltage

The frame grabber shall supply 12V DC ±1V to pins and 1 and 26 on the Camera Link connector(s).

10.4.2.2 Power

The frame grabber shall be capable of supplying 4W per cable over the full voltage range defined in Section 10.4.2.1. The 4W must be available at the camera end of the cable, thus the frame grabber must provide adequate headroom to compensate for power loss in the cable.

NOTE: It therefore needs to be able to supply 8W to a medium/full/72 bit/80 bit camera.

The frame grabber shall tie together pin 1 to pin 26, and pin 13 to pin 14, on the Camera Link connector(s)

NOTE: This helps ensure that the power is equally split between the four power lines in the cable.

10.4.3 Protection Systems

In the event of a conventional Camera Link cable or camera being plugged into a PoCL frame grabber, the power output from the frame grabber would get shorted to ground. Protection systems are therefore needed.

10.4.3.1 Over-Current Protection (OCP)

All PoCL frame grabbers shall implement an over-current protection circuit to limit the transient power in the event of a power-ground short to 360mJ per cable.

The OCP shall still be implemented even if SafePower is implemented.

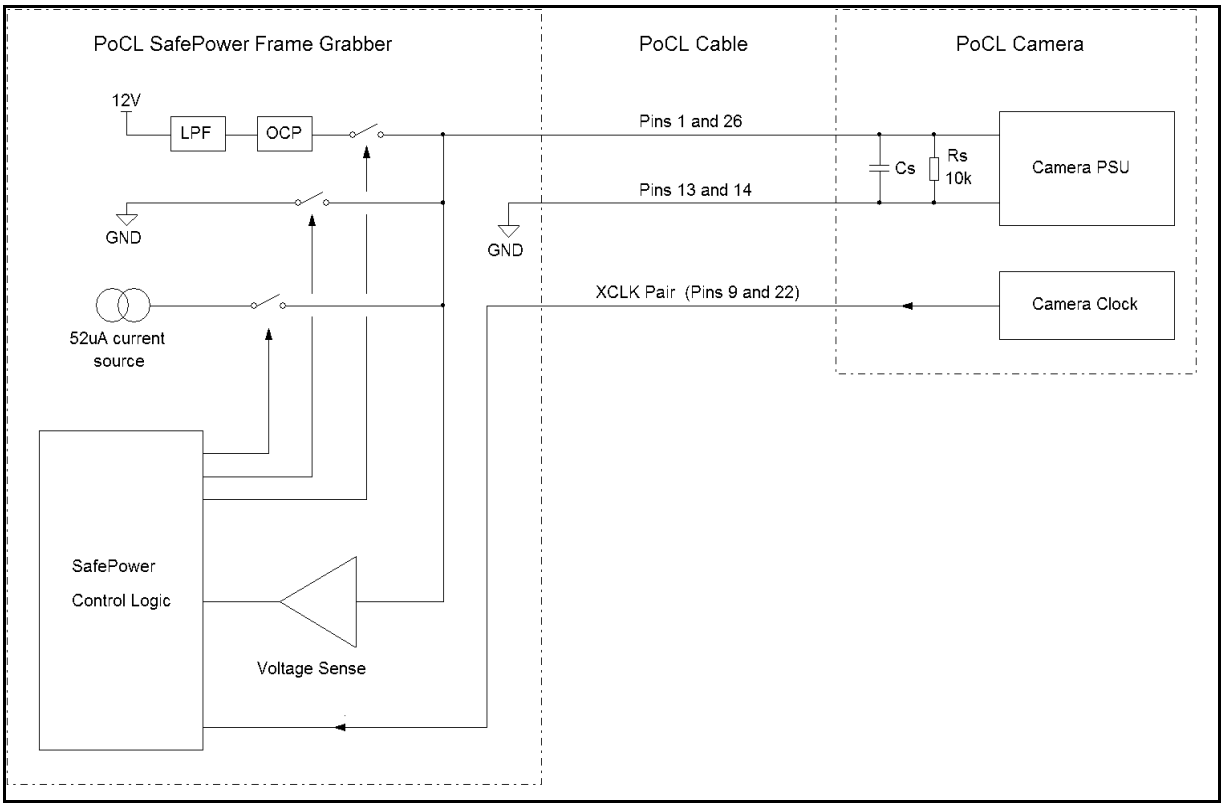
NOTE: The OCP is the minimum protection device to satisfy the standard, preventing damage or fire risk. It allows the implementation of low cost systems in applications with minimal risk of users connecting the wrong cables or cameras. A Polyswitch or similar resettable fuse should satisfy this requirement.

Caution: A resettable fuse is not intended to provide protection against continuous use with a conventional cable or camera.

10.4.3.2 SafePower

SafePower is a protocol to prevent the frame grabber from attempting to supply power to a conventional cable or camera. It is recommended that it is implemented. Figure 10-4 shows an example of a SafePower implementation.

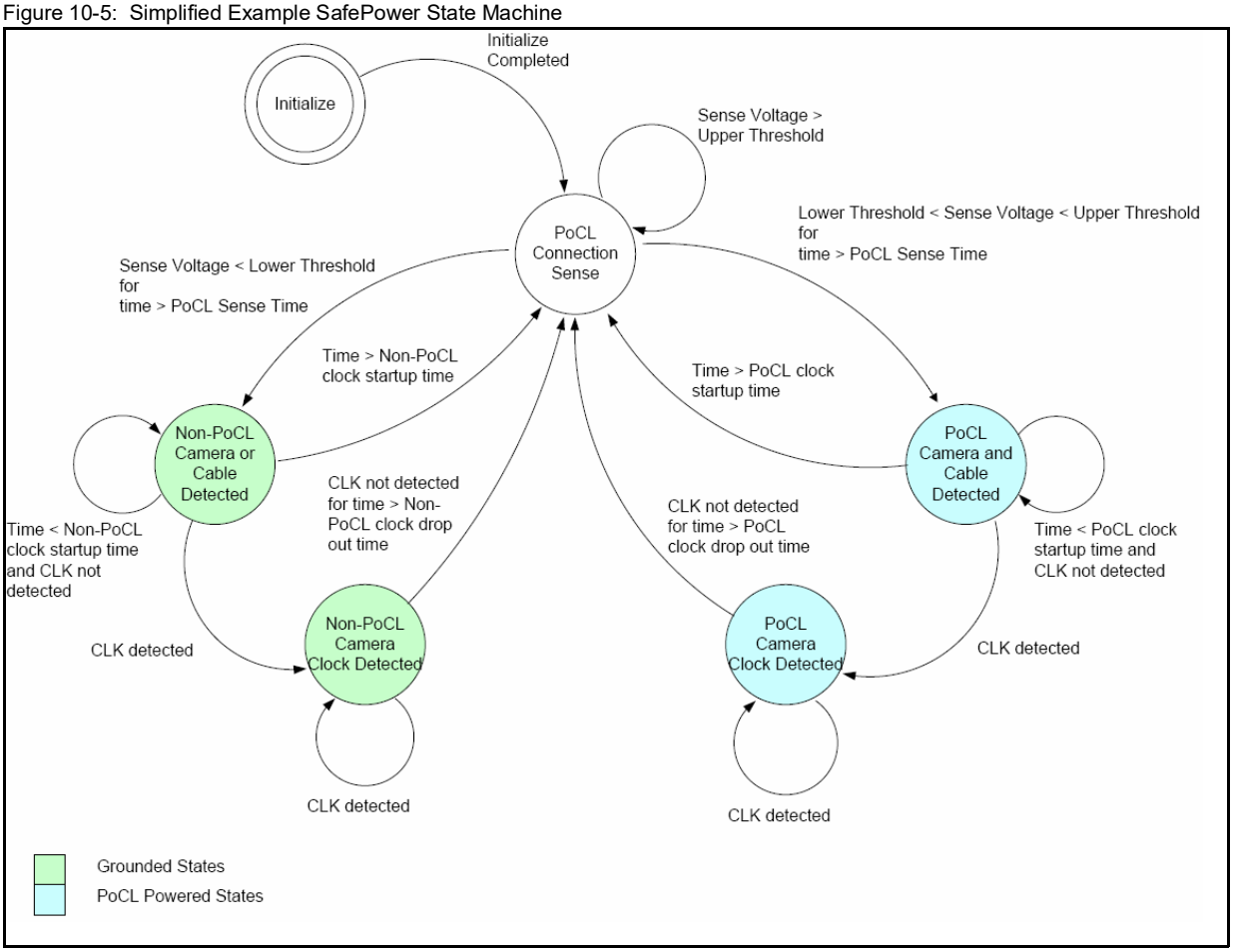
Figure 10-4: Example SafePower Implementation



NOTE: While the OCP should prevent damage in the event of a conventional cable or camera being connected, it may not be sufficient to prevent the system's power supply from being tripped. SafePower is designed to prevent any risk of the power supply being tripped.

SafePower shall be implemented for a switchable PoCL frame grabber. Figure 10-5 shows a simplified example SafePower State Machine.

Figure 10-5: Simplified Example SafePower State Machine



A SafePower frame grabber shall meet the following requirements:

a. The frame grabber shall sense that a PoCL camera and cable are connected before applying power. It can do this by sensing the camera's nominal 10kΩ input resistance "Rs", in which case it shall use a sense current of 52µA ± 10%.

NOTE: The 10kΩ / 52µA combination, with a total tolerance of 15%, gives a sensed voltage of 0.44V to 0.6V after allowing for the RC time constant of 0.57s from the 57µF maximum capacitance "Cs" with the 10kΩ input resistance. Note that if a conventional camera or cable is connected, the sensed voltage will be near zero.

b. Once power has been applied to a PoCL camera, the frame grabber shall monitor the clock pair on pins 9 and 22 of the Camera Link connector(s). If the clock is not present within the time specified in section Section 10.3.2.3 of the frame grabber supplying power, or if at any time the clock stops for more than the time specified in section Section 10.3.2.3, the frame grabber shall remove power from the camera.

NOTE: This causes power to be removed if the camera or cable is unplugged, and prevents the risk of a short should a user unplug a powered PoCL camera, and plug in a conventional camera in its place. It also allows the state machine controlling SafePower to return to its "Sense" state ready to detect a new camera. The time given in section Section 10.3.2.3 is a compromise between allowing time for the camera to start up, and the risk of a user swapping cables very soon after

power is applied.

c. Once power has been applied to a PoCL camera, the frame grabber shall monitor the voltage on pins 1 and 26 on the Camera Link connector(s). If this voltage drops to a level for more than 20ms indicating that the OCP has tripped, the frame grabber shall remove power from the camera.

d. If the frame grabber senses that a conventional Camera Link camera or cable is connected, it shall connect its PoCL power lines to ground.

NOTE: This allows them to operate as inner shield wires. It also means that a SafePower frame grabber is inherently a Switchable PoCL frame grabber.

e. Once the PoCL power lines have been connected to ground for a conventional camera, the frame grabber shall monitor the clock pair on pins 9 and 22 of the Camera Link connector(s). If the clock is not present within the time specified in section Section 10.3.2.3 of the frame grabber supplying power, or if at any time the clock stops for more than 1s, the frame grabber shall disconnect the PoCL power lines from ground.

NOTE: This allows the state machine controlling SafePower to return to its "Sense" state ready to detect a new camera. The time of 1s is longer than for a PoCL camera in section Section 10.4.3.2b. because conventional cameras do not have any clock startup or disconnection requirements; however there is no risk of damage resulting from the power lines being left grounded, and while the loss of two of the Inner Shield lines will reduce noise immunity, if there is no clock, the system isn't in use anyway.

It is recommended that a SafePower frame grabber supports a "PoCL disabled" mode where its PoCL power lines are always connected to ground. This allows for legacy conventional cameras with very long clock startup or clock disconnection times, in case any operational problems result from the action of the PoCL sense circuit.

10.4.4 Support for Medium/Full/72 Bit/80 bit Cameras

A frame grabber implementing SafePower shall operate SafePower concurrently on two Camera Link connectors which support medium/full/72 bit/80 bit operation, to minimize the time difference between the two camera connectors supplying power to the camera.

NOTE: Most of the requirements for medium/full/72 bit/80 bit configuration operation apply to the camera. The PoCL section of a frame grabber need not know the difference between for instance two independent PoCL base cameras being connected and one PoCL full camera.

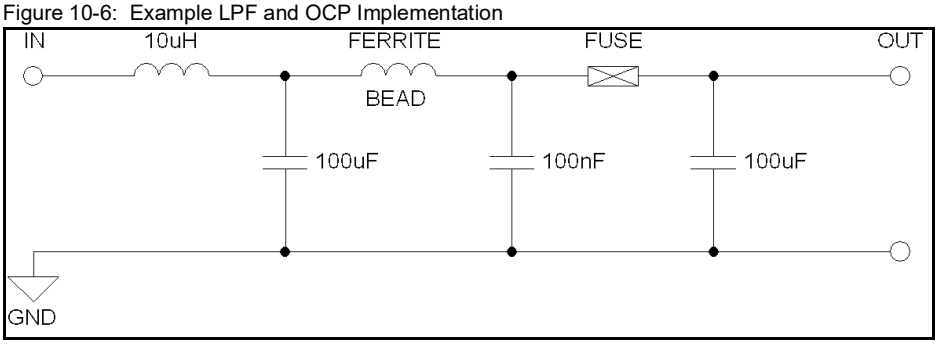
10.4.5 Power Supply Filter (LPF)

The frame grabber shall implement a low pass filter in the power supplied to each Camera Link connector with the following frequency response requirements when driving into a 27Ω test load:

- By 10kHz: At least 20dB attenuation.
- By 1MHz: At least 40dB attenuation.

NOTE: This provides clean power to the camera.

Figure 10-6: Example LPF and OCP Implementation



10.4.6 Labeling

The frame grabber shall be clearly marked to indicate it supports PoCL, either with the text "PoCL", and/or by marking with the PoCL logo.

Frame grabbers supporting medium/full/72 bit/80 bit configurations should be so labeled.

If the frame grabber also supports SafePower, it shall also be marked with the text "SafePower".

It is recommended that if space allows these labels are on the frame grabber's end panel.

If the frame grabber does not support SafePower then it shall have a clear warning in the operations manual that connecting or disconnecting the PoCL cable or camera is only allowed when the power is off.

10.4.7 Indicator Lamps

It is recommended that the frame grabber has an indicator near the Camera Link connector to show when it is supplying power to that connector.

NOTE: There may not be sufficient space on the frame grabber's end panel to allow this.

10.5 Cable Requirements

For full details of PoCL cable requirements see Section 9.1.3.

NOTE: A cable suitable for PoCL use is also suitable for conventional Camera Link.

10.6 Miscellaneous

10.6.1 Repeaters

A PoCL Camera Link cable repeater shall not pass camera power through the repeater.

NOTE: This would result in a voltage drop along multiple cables exceeding that allowable, preventing reliable operation.

A PoCL Camera Link cable repeater shall behave like a PoCL frame grabber to the camera. The repeater therefore shall support all the requirements of Section 10.4. The repeater's power supply shall power the camera.

A PoCL compatible Camera Link cable repeater can behave like a PoCL camera to the frame grabber.

NOTE: Allowing the frame grabber to think that a PoCL camera is connected would not do any

harm, but it may not be very useful either.

Appendix A - Camera Link HDR Mating Requirements For Previous Revisions

A.1 Introduction

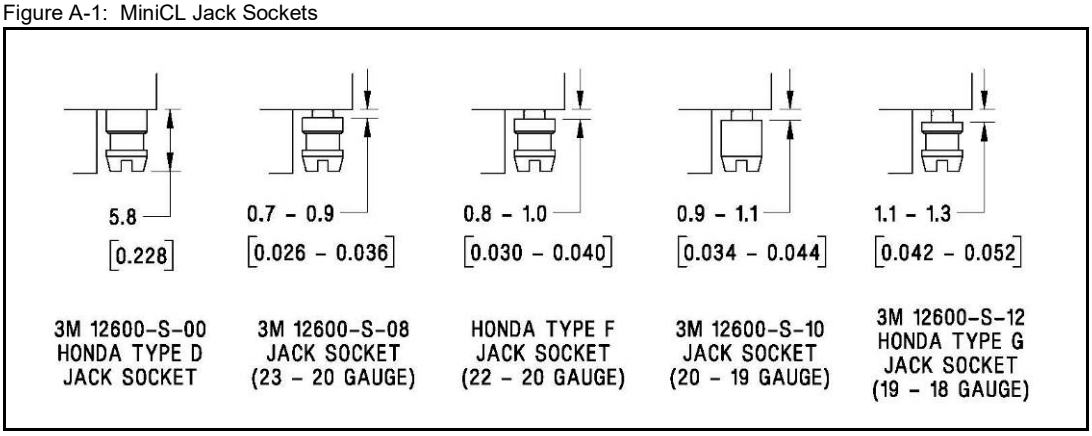
Sections 9.1.2.11 and 9.1.2.12 of this specification give requirements and recommendations for the mating requirements for MiniCL and PoCL-Lite connectors. These improve the fit between the jack sockets and the threaded fasteners on the cable.

This appendix shows the previous requirements from the v2.0 Camera Link specification. Products made to the v2.0 specification are still Camera Link compliant, but for new designs it is recommended to conform to the recommendations in sections 9.1.2.11 and 9.1.2.12 of this specification (v2.1).

CL v2.0, Section 10.1.2.11 - MiniCL/PoCL-Lite Connector Jack Socket Requirements

The dimension of the MiniCL receptacle jack socket shall be 5.8 mm. The appropriate panel lock shall be used for panel mounting as shown in Figure A-1 below. The maximum panel thickness shall be 1.5 mm. For panel thicknesses greater than 1.5 mm, the panel shall be counter-bored to reduce the thickness to 1.2 to 1.5 mm.

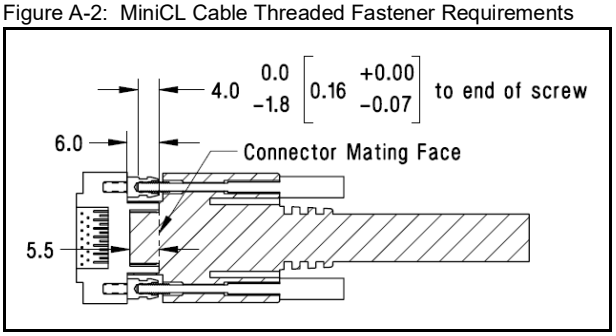
Figure A-1: MiniCL Jack Sockets



CL v2.0, Section 10.1.2.11 - MiniCL/PoCL-Lite Cable Threaded Fastener Requirements

The junction shells on both ends of the cable assembly must have threaded fasteners for attachment to the jack sockets on the receptacle connector. The threaded fasteners shall be positioned as shown in Figure A-2. The threaded fasteners may be thumbscrews, machine screws or other type of threaded fastener that will properly fix the cable assembly to the receptacle.

Figure A-2: MiniCL Cable Threaded Fastener Requirements



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