HT32F1655 / HT32F1656 EBI

D/N: HA0335E

Introduction

The parallel bus interface in the HT32F1655 / 56 microcontrollers carries the name EBI or External Bus Interface. It is able to access external asynchronous parallel interface devices such as SRAM, Flash and LCD modules. The interface is memory mapped into the internal address bus of the Cortex-M3. The data and address lines can be multiplexed in order to reduce the number of pins required to connect to external devices. The bus read/write timing can be adjusted to meet the timing specifications of external devices.

Bus Control Signals

The below table shows the control signals that are provided in the HT32F1655/56 external bus interface in addition to the address and data bus singals. Note that some devices in the HT32F1655/56 series only have a subset of functions that are described below.

Signal	Direction	Description
A[xx:0]	Output	Address Bus
AD[xx:0]	Input/Output	Address/Data Bus
CS	Output	Chip Select
OE	Output	Output Enable
WE	Output	Write Enable
ALE	Output	Address Latch Enable
BL[1:0]	Output	Byte Lane
ARDY	Input	Asynchronous Ready

Table 1 EBI Bus Control Signals

BL[1:0] is only used for some 16-bit data widths and SRAM. ARDY is only used for some NOR Flash

EBI Operating Modes

The EBI supports multiplexed and non-multiplexed addressing modes. The non-multiplexed addressing mode can be operated more efficiently and faster but it requires a higher number of pins. The multiplexed addressing modes are slower and require an external address latch device and a lower number of pins.

Non-Multiplexed Modes

- D8A8: In this mode, 8-bit address and 8-bit data is supported. The address is located on the higher 8 bits of the EBI_AD lines and the data uses the lower 8 bits.
- D16: In this non-multiplexed mode 16-bit data is provided on the 16 EBI_AD lines. The addresses are provided on the EBI_A lines.

Multiplexed Modes

- D8A24ALE: This mode allows 24-bit address with 8-bit data multiplexed on the EBI_AD[15:0] lines to reduce the pins utilisation and uses the EBI_ALE signal to decode 8-bit data and 24-bit address. The upper 8 bits of the EBI_AD lines (EBI_AD[15:8]) are consecutively used for the highest 8 bits and the lowest 8 bits of the address. The lower 8 bits of the EBI_AD lines (EBI_AD[7:0]) are used for the middle 8 address bits and 8-bit data.
- D16A16ALE: In this mode, 16-bit address and 16-bit data is supported, but the utilisation of an external latch and an extra signal EBI_ALE is required. The 16-bit address and 16-bit data bits are multiplexed on the EBI_AD pins.

Timing Configuration

In HT32F1655/56 EBI, there are several timing parameter settings for different possible access protocols.

- RDSETUP: Sets the number of cycles that the address is setup for before OE is asserted.
- RDSTRB: Sets the number of cycle that OE is held active for.
- RDHOLD: Sets the number of cycles that CS is held active for after OE is deasserted.
- WESETUP: Sets the number of cycles that the address is setup for before WE is asserted.
- WESTRB: Sets the number of cycles that WE is held active for.
- WEHOLD: Sets the number of cycles that CS is held active for after WE is deasserted.

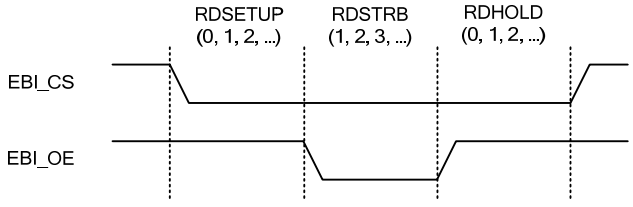

Figure 1 EBI Non-Multiplexed Read Timing

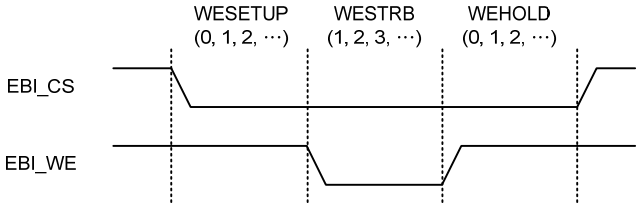

Figure 2 EBI Non-Multiplexed Write Timing

For the multiplexed mode, ADDRSETUP and ADDRHOLD are used to control the timing of the external address latch device. Refert to the reference manual for more detailed diagrams regarding the timing configuration.

- ADDRSETUP: Sets the number of cycles the address is driven onto the AD bus before ALE is asserted.
- ADDRHOLD: Sets the number if cycles the address is held on the AD bus after ALE is asserted.

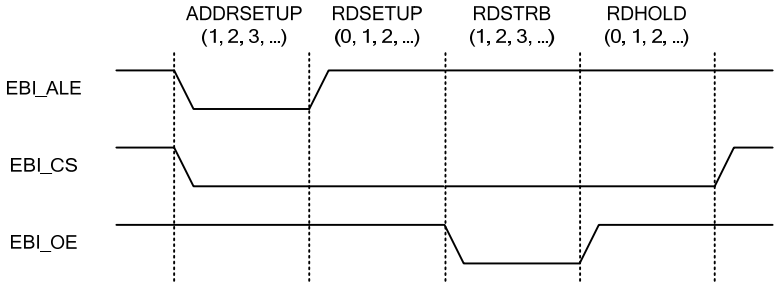

Figure 3 EBI Multiplexed Read Timing

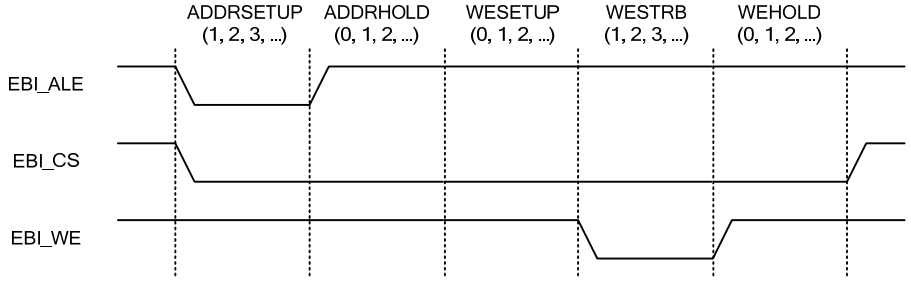

Figure 4 EBI Multiplexed Read Timing

Other Features

- Page read operation
- Write Buffer
- AHB transaction width conversion
- Read/Write cycle extension
- Polarity configuration

Interfacing with Asynchronous NOR Flash

EBI Configuration

To control a NOR Flash memory, the EBI provides the following features:

- Select the bank to be used to map the NOR Flash memory.
- Select the EBI mode to be used: D8A8, D16A16ALE, D8A24ALE, D16.
- Enable or disable the Asynchronous Ready or Asynchronous Ready timeout function.
- Configure the control signal polarity setting.
- Configure the timing parameters.
- Configure the Page Read function.

For asynchronous NOR Flash memory, there are different ac characteristics, so the first step is to know what value of timing parameter should be used with the specific memory. In this application note, the MX29GL256F memory is used as a reference. Table 2 lists the MX29GL256F memory read and write access timings.

Symbol	Description	Value	Unit
Tcs	Chip enable setup time	0	ns
Twp	WE# pulse width	35	ns
Twph	WE# pulse width high	30	ns
Twc	Write period time	100	ns
Taa	Valid data output after address	100	ns
Toe	Valid data output after OE# low	25	ns
Trc	Read period time	100	ns

Table 2 MX29GL256F NOR Flash memory timing

Using the memory timing in Table 2, the EBI can be innitialised as follows. Note that the CPU is running at 72MHz and using EBI bank 0 in D16 mode as an example.

```
EBI_StructInit(&EBI_InitStructure);

EBI_InitStructure.EBI_Bank = EBI_BANK_0;
EBI_InitStructure.EBI_Mode = EBI_MODE_D16;
EBI_InitStructure.EBI_AsynchronousReady = EBI_ASYNCHRONOUSREADY_DISABLE;
EBI_InitStructure.EBI_ARDYTimeOut = EBI_ARDYTIMEOUT_DISABLE;
EBI_InitStructure.EBI_ChipSelectPolarity = EBI_CHIPSELECTPOLARITY_LOW;
EBI_InitStructure.EBI_AddressLatchPolarity = EBI_ADDRESSLATCHPOLARITY_LOW;
EBI_InitStructure.EBI_WriteEnablePolarity = EBI_WRITEENABLEPOLARITY_LOW;
EBI_InitStructure.EBI_ReadEnablePolarity = EBI_READENABLEPOLARITY_LOW;
EBI_InitStructure.EBI_ReadySignalPolarity = EBI_READYSIGNALPOLARITY_LOW;
EBI_InitStructure.EBI_AddressSetupTime = 0;
EBI_InitStructure.EBI_AddressHoldTime = 0;
EBI_InitStructure.EBI_WriteSetupTime = 2;
EBI_InitStructure.EBI_WriteStrobeTime = 4;
EBI_InitStructure.EBI_WriteHoldTime = 3;
EBI_InitStructure.EBI_ReadSetupTime = 2;
EBI_InitStructure.EBI_ReadStrobeTime = 6;
EBI_InitStructure.EBI_ReadHoldTime = 1;
EBI_InitStructure.EBI_PageMode = EBI_PAGEMODE_ENABLE;
EBI_InitStructure.EBI_PageLength = EBI_PAGELENGTH_32;
EBI_InitStructure.EBI_PageHitMode = EBI_PAGEHITMODE_ADDINC;
EBI_InitStructure.EBI_PageAccessTime = 0x3;
EBI_InitStructure.EBI_PageOpenTime = 0xFF;
EBI_Init(&EBI_InitStructure);

EBI_Cmd(EBI_BANK_0, ENABLE);
```

Hardware Connection

The below figures show a typical connection between the MX29GL256F NOR Flash and the four EBI modes. The unused EBI pins can be used as general purpose I/O pins.

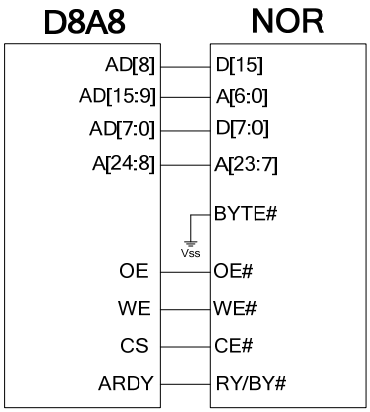

Figure 5 Connecting the EBI to the NOR Flash in the D8A8 Mode

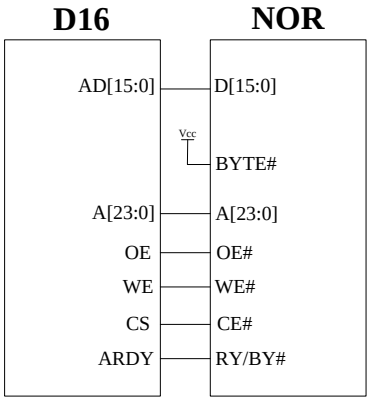

Figure 6 Connecting the EBI to the NOR Flash in the D16 Mode

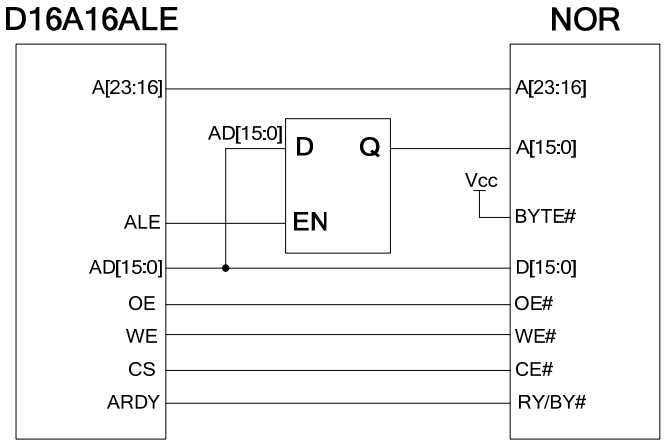

Figure 7 Connecting the EBI to the NOR Flash in the D16A16ALE Mode

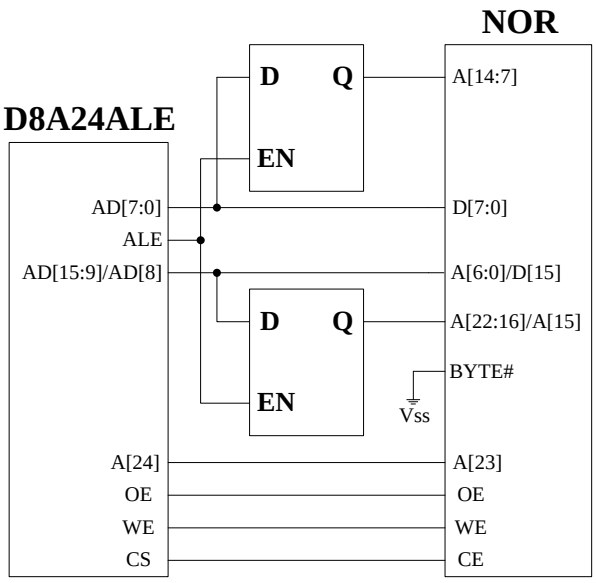

Figure 8 Connecting the EBI to the NOR Flash in the D8A24ALE Mode

Interfacing to the Asynchronous 16-bit SRAM

EBI Configuration

To control the SRAM the EBI provides the following features:

- Selects the bank to be used to map the NOR Flash memory.
- Select the EBI mode to be used: D8A8, D16A16ALE, D8A24ALE, D16.
- Enable or disable the Byte Lane function.
- Configure the control signal polarity setting.
- Configure the timing parameters.

For asynchronous SRAM memory, there are different ac characteristics, so the first step is to know what value of timing parameter should be used with the specific memory. In this application note, the IS61WV102416BLL memory is used as a reference. Table 3 lists the IS61WV102416BLL memory read and write access timings.

Symbol	Description	Value	Unit
Tsce	CE to Write End	8	ns
Taw	Address Setup Time to Write End	8	ns
Tpwe	WE Pulse Width	8	ns
Twc	Write Cycle Time	10	ns
Taa	Address Access Time	10	ns
Tdoe	OE Access Time	6.5	ns
Trc	Read Cycle Time	10	ns

Table 3 IS61WV102416BLL SRAM Memory Timing

Using the memory timing in Table 3, the EBI can be initialised as follows. Note that the CPU is running at 72MHz and using EBI bank 2 in D16 mode as an example.

```
EBI_StructInit(&EBI_InitStructure);

EBI_InitStructure.EBI_Bank = EBI_BANK_2;
EBI_InitStructure.EBI_Mode = EBI_MODE_D16;
EBI_InitStructure.EBI_ByteLane = EBI_BYTELANE_ENABLE;
EBI_InitStructure.EBI_ChipSelectPolarity = EBI_CHIPSELECTPOLARITY_LOW;
EBI_InitStructure.EBI_AddressLatchPolarity = EBI_ADDRESSLATCHPOLARITY_LOW;
EBI_InitStructure.EBI_WriteEnablePolarity = EBI_WRITEENABLEPOLARITY_LOW;
EBI_InitStructure.EBI_ReadEnablePolarity = EBI_READENABLEPOLARITY_LOW;
EBI_InitStructure.EBI_ByteLanePolarity = EBI_BYTELANEPOLARITY_LOW;
EBI_InitStructure.EBI_AddressSetupTime = 0;
EBI_InitStructure.EBI_AddressHoldTime = 0;
EBI_InitStructure.EBI_WriteSetupTime = 2;
EBI_InitStructure.EBI_WriteStrobeTime = 2;
EBI_InitStructure.EBI_WriteHoldTime = 1;
EBI_InitStructure.EBI_ReadSetupTime = 2;
EBI_InitStructure.EBI_ReadStrobeTime = 2;
EBI_InitStructure.EBI_ReadHoldTime = 1;
EBI_Init(&EBI_InitStructure);

EBI_Cmd(EBI_BANK_2, ENABLE);
```

Because of the HT32F1655/56 IO driving capability, it is appropriate to set some EBI timing parameters to 2 when the CPU is running at 72MHz.

Hardware Connection

The below figures show a typical connection between the IS61WV102416BLL SRAM and the four EBI modes. The unused EBI pins can be used as general purpose I/O pins.

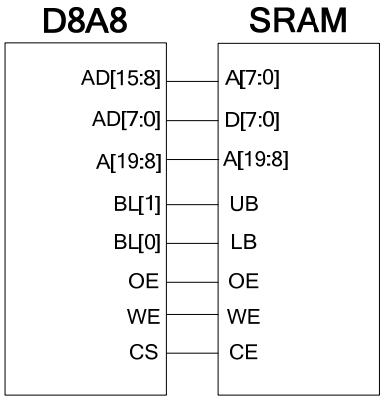

Figure 9 Connecting the EBI to the NOR Flash in the D8A8 Mode

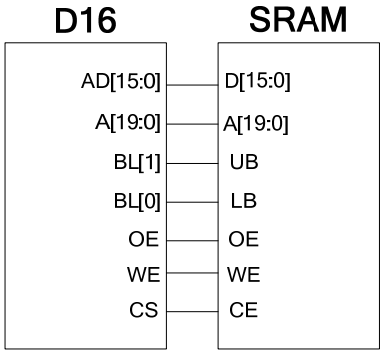

Figure 10 Connecting the EBI to the NOR Flash in the D16 Mode

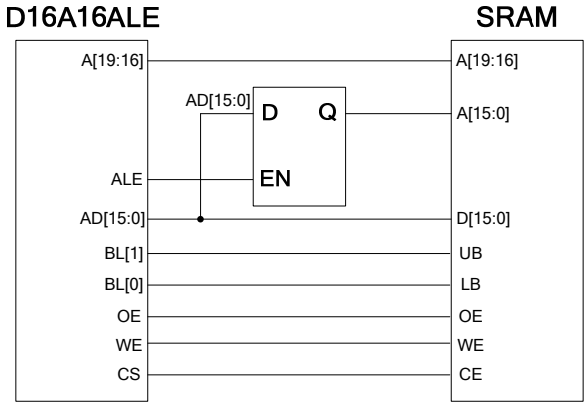

Figure 11 Connecting the EBI to the NOR Flash in the D16A16ALE Mode

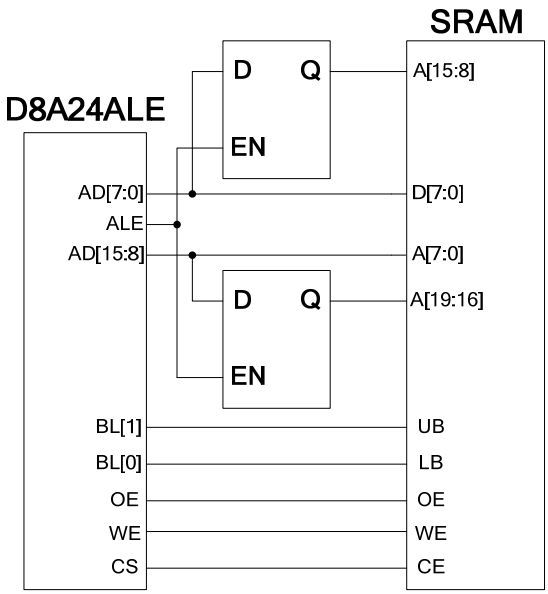

Figure 12 Connecting the EBI to the NOR Flash in the D8A24ALE Mode

Interfacing with Asynchronous NOR Flash

EBI Configuration

As described above, with regard to asynchronous NOR Flash or SRAM memories, there are different access protocols. It is first necessary to define what kind of protocol is to be used with the user LCD. The choice depends on the different control signals and on the behavior of the LCD during read and write transactions.

Hardware Connection

The below figures show a typical connection between the LCD Intel 8080 and the four EBI modes. The unused EBI pins can be used as general purpose I/O pins.

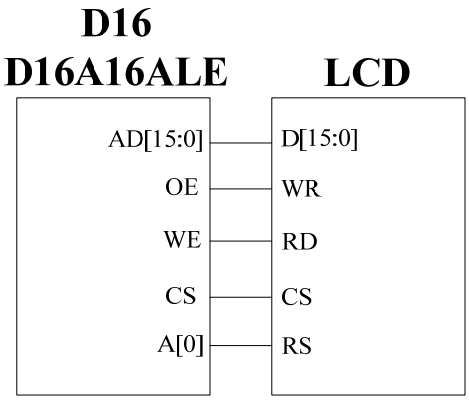

Figure 13 Connecting the EBI to the LCD 8080-like Interface in the D16/D16A16ALE Mode

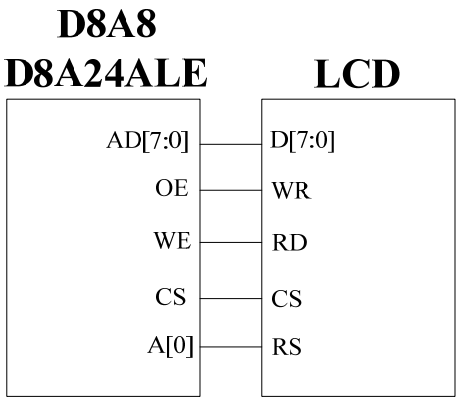

Figure 14 Connecting the EBI to the LCD 8080-like Interface in the D8A8/D8A24ALE Mode